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Quadrature oscillator based on a novel low-voltage ultra-low-power quasi-floating-gate DVCC

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Low-voltage ultra-low-power analog circuit design;
DVCC.

Abstract. In this work, a new realization topology of the low-voltage ultra-low-power quadrature oscillator is presented. This quadrature oscillator utilizes only two active elements, namely, Differential Voltage Current Conveyors (DVCCs), and five passive ones. All of the elements are grounded, which is recommended for integrated circuit implementation. The DVCC is based on quasi-floating-gate MOS transistor, which is a distinct technique from the conventional one, featuring operation at low-voltage and ultra-low-power conditions; hence, the proposed DVCC works with low supply voltage of $\pm$ 400 mV and consumes power of merely 6.6 μW. Thanks to these features, the total power dissipation of the oscillator is only 0.28 mW. The simulation results using 0.18-μm TSMC CMOS technology are included in order to prove validity of the design.

1. Introduction

Evidently, among many parameters of great interests in electronic circuits performance improvement, Low-Voltage (LV) Low-Power (LP) ones are probably the first priority when considering their contribution to prolonging battery life of portable devices. LV LP parameters are indispensable in a myriad of biomedical portable devices and wireless technology, e.g., cellular phones, laptop computers, etc. [1].

The formidable challenge in LV analog circuit design is the relatively high threshold voltage value of MOSFET transistor (MOST) in comparison with the used supply voltage. Of late, the threshold voltage value has been considered as an obstacle to the input signal that limits the input voltage range of the analog circuits. As a consequence, several design techniques have been proposed to overcome this limitation [2].

In addition to the conventional low-voltage analog circuit design techniques, the Bulk-Driven (BD), Floating-Gate (FG), and Quasi-Floating-Gate (QFG) are by far the most popular unconventional techniques. These unconventional techniques can be used to avoid complexity of the circuit and achieve attractive results under the LV domain [2]. They have the ability to operate without concern for the threshold voltage. In other words, these techniques make the transistor able to operate with the supply voltage close to its threshold voltage.

Nevertheless, the challenge often encountered in these unconventional techniques is the small transconductance value compared with the conventional gate-driven one. This issue can be translated into many undesirable traits such as poor gain-bandwidth product, low frequency response, and low speed [2]. However, a multitude of circuits can exploit these disadvantages; biomedical, telemetry, real time speech recognition,

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and other systems are utilizing signals with low frequency response [3-7].

Recently, the bulk-driven and the floating-gate techniques have successfully been employed in many LV analog circuit designs [8,9]. However, there are some limitations and drawbacks to these techniques. With regard to the bulk-driven technique, its bulk transconductance is approximately 2.5 to 5 times lower than the conventional gate transconductance, which results in a lower unity gain frequency and higher input-referred noise; besides, a latch-up may occur, which limits the maximum operating voltage [10-16]. In respect of the floating-gate technique, it mainly suffers from the increased silicon area, initial charge trapped in the floating gates, and approximately 1.6 to 2 times lower value of the equivalent transconductance than the conventional gate transconductance, resulting in gain-bandwidth product degradation. It is interesting that these limitations and drawbacks could be eliminated by using the alternative QFG technique [17-26].

The QFG principle is similar to the FG one with some variations; in case of FG, unlike in QFG, the DC biasing point for the transistor is floating [27-32]. The non-floating DC biasing point in case of QFG is achieved by connecting the gate of the transistor to a suitable bias voltage via a large-value resistor (R_{LARGE}), as illustrated in Figure 1(a). The value of the bias voltage should be chosen so that the MOST is placed in the saturation region.

Obviously, applying the large-value resistor is not easy from the viewpoint of fabrication, since it increases the chip area of the system. However, to avoid the difficulty in design, stemming from the large resistor size, a MOST in the cut-off region (diode connected transistor) is used instead of the resistor, as shown in Figure 1(b) [33-35]. This very large voltage dependent resistor (diode connected transistor) can take values in the range of hundreds of Giga Ohms.

The equivalent circuit of QFG MOST is given in Figure 1(c). As shown in [35], the voltage transfer can be represented by:

$$V_G = \frac{sR_{\mathrm{larg}}}{1 + sR_{\mathrm{larg}}\, C_{\,\mathrm{total}}}(C_{in}V_{in} + C_{GD}V_D + C_{GS}V_S + C_{GB}V_B), \quad (1)$$

where C_{total} is the total capacitance, and is given by:

$$C_{\,\mathrm{total}} = C_{in} + C_{\mathrm{GD}} + C_{\mathrm{GS}} + C_{\mathrm{GB}} + C'_{\mathrm{GD}}, \quad (2)$$

where C_{GD}, C_{GS}, and C_{GB} denote the capacitances from gate to drain, to source, and to bulk, respectively. C'_{GD} denotes the capacitances from gate to drain of the M_R transistor.

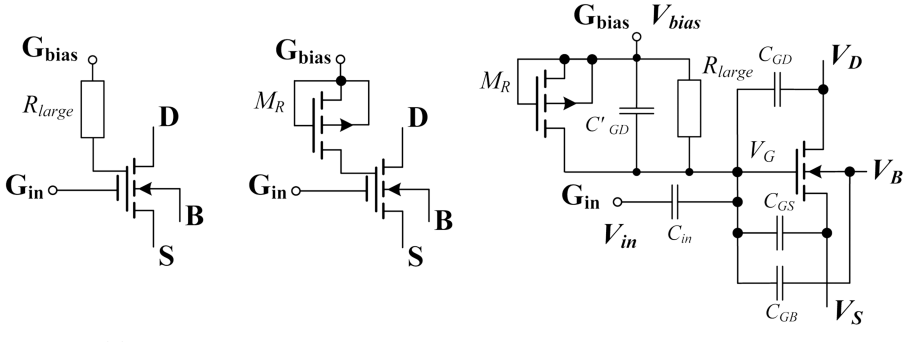
The signal at the QFG of the MOST depends on the inputs signal V_{in} with the ratio of $C_{in}/C_{\mathrm{total}}$. Hence, the input signal is attenuated, which potentially enables rail-to-rail input swing [35,36].

Based on the above mentioned advantages of the QFG MOST, this paper introduces a new design of DVCC utilizing the QFG technique. The low-voltage supply of ±400 mV, ultra-low-power consumption of 6.6 μW, acceptable current, and voltage bandwidths of 19 MHz are the major attractive characteristics of the circuit proposed. Furthermore, with the flexibility in design trade-offs between LV LP and an acceptable bandwidth, the performance of the proposed DVCC is suitable for many applications, e.g., implantable biomedical devices, where the processing signal possesses low amplitude and frequency in the ranges of millivolt and kilohertz, respectively [3-7].

The paper is organized as follows: to comprehend the DVCC principle and its non-ideal model, Sections 2 and 3 are presented. The QFG DVCC is employed in the design of a high-performance quadrature oscillator, which is given in Sections 4 and 5. At the end of the paper, the conclusion is provided.

2. The proposed QFG-DVCC realization

The Differential Voltage Current Conveyor (DVCC) is a powerful current-mode building block with the benefit of providing a multitude of interesting applications, e.g., in filters, oscillators, current-mode integrators, current-mode differentiators, instrumentation



(a) (b) (c)

Figure 1. Single-input QFG MOST: (a) Symbolic with R_{LARGE}, (b) symbolic with M_R, and (c) equivalent circuit of (b).

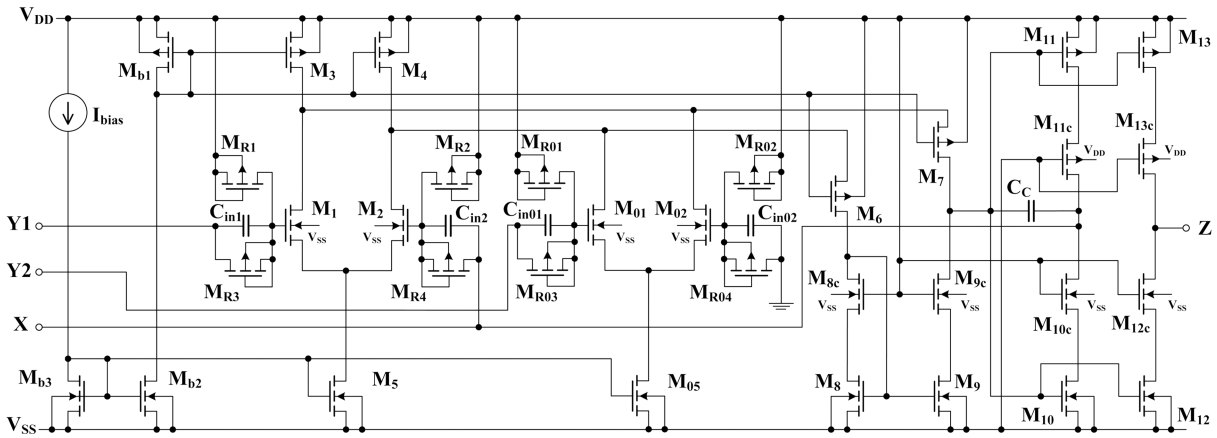


Figure 2. CMOS implementation of the novel LV LP DVCC based on QFG MOSTs.

amplifiers, [37-43]. The ideal DVCC is defined by the following hybrid matrix:

$$\begin{pmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_Z \end{pmatrix} = \begin{pmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_X \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{pmatrix}. \quad (3)$$

The novel DVCC based on QFG MOSTs is presented in Figure 2. The proposed structure is composed of input, second, and output stages. The input stage consists in differential pair transistors $M_1 - M_2$ and $M_{01} - M_{02}$ whose gate terminals are connected to the positive supply voltage via reverse-biased diode connected transistors $M_{R1} - M_{R2}$ and $M_{R01} - M_{R02}$, respectively. This type of connection assures that the differential pair transistors are placed in the saturation region and the threshold voltage is shifted away from the signal path. Transistors M_{b1}, M_{b2}, M_{b3}, M_3, M_4, M_5, and M_{05} are used to set up the bias currents necessary for the differential stages. In addition, transistors M_6 and M_7 provide a level shift function, and the cascoded current mirrors M_8, M_9, M_{8c}, and M_{9c} provide a differential to single-ended conversion. The second stage consists in transistors M_{10}, M_{10c}, M_{11}, and M_{11c}. The proposed circuit is enhanced by using cascode structures $M_{12} - M_{12c}$ and $M_{13} - M_{13c}$, rather than the simple one, to obtain an accurate copy of the input current and higher output impedance desirable for easy cascading; these transistors form the output stage of the proposed DVCC. The small Miller compensation network with C_C of 0.01 pF is employed for stability and for ensuring a good transient response with 10 pF load capacitance. The optimal transistor aspect ratios are given in Table 1.

It is observable in Figure 1(c) that the input of the QFG is connected in a high-pass filter configuration with cut-off frequency equal to:

$$f_c = \frac{1}{2\pi R_{\text{large}} C_{\text{total}}}, \quad (4)$$

Table 1. Component values and transistor aspect ratios from Figure 2.

QFG-DVCC	W/L [μm/μm]
M_1, M_2, M_{01}, M_{02}	3/0.5
M_3, M_4	13/1
M_5, M_{05}	4/0.6
M_6, M_7	20/1
M_8, M_9	8/1
M_{8c}, M_{9c}, M_{b2}, M_{b3}	2/1
M_{10}, M_{12}, M_{10c}, M_{12c}	10/0.5
M_{11}, M_{13}, M_{11c}, M_{13c}	30/0.5
M_{b1}	6/1
M_{R1} - M_{R4}, M_{R01} - M_{R04}	5/1
C_c= 0.01 pF, $C_{in1}, C_{in2}, C_{in01}, C_{in02}$ =0.2 pF, $I_{\text{bias}} = 1\mu$A	

where C_{total} is the total capacitance (Eq. (2)). To attain low cut-off frequency in the milli- hertz range, one should use a substantially large resistance value and moderately small capacitance. As a consequence, the filter will not affect the circuit performance working in higher frequencies (higher than the mHz range) [36].

However, to keep proper behavior of the DVCC, i.e., to also process the dc voltage, reverse-biased diode connected transistors M_{R3}, M_{R4}, M_{R03}, and M_{R04} are connected in parallel to the input capacitors C_{in1}, C_{in2}, C_{in01}, and C_{in02}, respectively. These connections create uncompensated voltage dividers. However, this effect, thanks to the internal feedback from the output of the second stage to X terminal, is suppressed [44].

It is worth mentioning that for some DVCC applications, there is a need to have both polarities of output current I_Z or multiple outputs I_{Z+} and/or I_{Z-}. This could be achieved by simply using current mirrors technique to copy and/or invert polarity of the output current I_Z without affecting the performance of X, $Y1$,

$Y2$, and Z terminals. This is the case for our proposed application example as a quadrature oscillator.

To finalize the verification of the proposed DVCC, all the required simulations are demonstrated in this part using 0.18-μm TSMC CMOS technology with the spice model shown in Figure 3.

Figure 4 depicts the frequency dependence of parasitic impedance for X and Z terminals. The parasitic impedance for X and Z terminals is apparently low and high, respectively. More specifically, the impedance value at low frequency is 31 dB at X input terminal, and the value of the output impedance at Z terminal is 135 dB; consequently, the high output impedance of Z terminal offers a solution to overcome the loading effect issue without the need for an additional buffer.

Figure 5 clarifies the frequency response of current gain I_Z/I_X and voltage gains V_X/V_{Y1}, V_X/V_{Y2}. The DVCC provides 19 MHz bandwidth at -3 dB. Figure 6 depicts the DC curves of I_X versus I_Z and related current errors $\Delta I = I_Z - I_X$ for various temperatures of 0, 27, and 60°C; it is evident that for the input current range of -50 to 50 μA, the current errors are negligible.

Figure 7 illustrates the DC curve of V_X versus V_{Y1} assuming that $Y2$ terminal is grounded. This curve shows an attractive rail-to-rail operating range. The low values of voltage errors $\boldsymbol{\Delta V} = V_{Y1} - V_X$ for temperatures of 0, 27, and 60°C are illustrated as well.

As shown in Figure 8, the voltage at X terminal follows the voltage difference of terminals $Y1$ and $Y2$ in a wide range; while stepping V_{Y2} to various values of [-150, -100, -50, 0, 50, 100, 150] mV.

Table 2 sums up the key design characteristics of the proposed QFG-DVCC circuit and the comparison with some other recently published works. It is notable that the proposed QFG-DVCC can be boastful of its attractive performances, especially the low supply voltage of ±400 mV and the ultra-low-power consumption of 6.6 μW, which are the primary aim of this design.

3. Non-ideal analysis of DVCC

Transistors mismatch, channel length modulation effect, and parasitic capacitances lead to difference between the ideal DVCC and the real one; the parasitic impedance of DVCC and the non-ideal gain effect adversely affect the circuit behavior and may pose deviations in the circuit characteristics. However, these effects could be minimized and unnoticeable when proper circuit design, layout design rules, and connection of the external passive elements with DVCC are applied. One of the suitable connections to absorb parasitic capacitances is that of grounded capacitors at Y and Z terminals, as a result of which a parallel connection of the low value of the parasitic capacitance with the external grounded capacitor is obtained. In the same way, the parasitic resistances at X termi-

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.MODEL CMOSN9 NMOS (                    LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ     = 1E-7          NCH     = 2.3549E17     VTH0    = 0.3669193
+K1     = 0.592797      K2      = 2.518108E-3   K3      = 1E-3
+K3B    = 4.7942179     W0      = 1E-7          NLX     = 1.745125E-7
+DVT0W  = 0             DVT1W   = 0             DVT2W   = 0
+DVT0   = 1.3683195     DVT1    = 0.4097438     DVT2    = 0.0552615
+U0     = 263.5112775   UA      = -1.363381E-9  UB      = 2.253823E-18
+UC     = 4.833037E-11  VSAT    = 1.017805E5    A0      = 1.9261289
+AGS    = 0.4192338     B0      = -1.069507E-8  B1      = -1E-7
+KETA   = -8.579587E-3  A1      = 2.789024E-4   A2      = 0.8916186
+RDSW   = 126.5291844   PRWG    = 0.4957859     PRWB    = -0.2
+WR     = 1             WINT    = 0             LINT    = 7.790316E-9
+XL     = -4E-8         XW      = 0             DWG     = -1.224589E-8
+DWB    = 1.579145E-8   VOFF    = -0.0895222    NFACTOR = 2.5
+CIT    = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB  = 0             ETA0    = 2.95614E-3    ETAB    = 1.374596E-4
+DSUB   = 0.013974      PCLM    = 0.7291486     PDIBLC1 = 0.1332365
+PDIBLC2 = 2.151668E-3  PDIBLCB = -0.1          DROUT   = 0.6947618
+PSCBE1 = 7.412661E10   PSCBE2  = 1.812826E-7   PVAG    = 9.540595E-3
+DELTA  = 0.01          RSH     = 5.9           MOBMOD  = 1
+PRT    = 0             UTE     = -1.5          KT1     = -0.11
+KT1L   = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1    = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL     = 0             WLN     = 1             WW      = 0
+WWN    = 1             WWL     = 0             LL      = 0
+LLN    = 1             LW      = 0             LWN     = 1
+LWL    = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO   = 8.71E-10      CGSO    = 8.71E-10      CGBO    = 1E-12
+CJ     = 9.67972E-4    PB      = 0.6966474     MJ      = 0.3609772
+CJSW   = 2.443898E-10  PBSW    = 0.8082076     MJSW    = 0.1013742
+CJSWG  = 3.3E-10       PBSWG   = 0.8082076     MJSWG   = 0.1013742
+CF     = 0             PVTH0   = 7.226579E-4   PRDSW   = -4.5298309
+PK2    = -4.696208E-4  WKETA   = 6.028223E-3   LKETA   = -8.791311E-3
+PU0    = 17.2549887    PUA     = 6.802365E-11  PUB     = 4.224871E-24
+PVSAT  = 1.298468E3    PETA0   = 1.003159E-4   PKETA  = -3.864603E-4
*
.MODEL CMOSP9 PMOS (                    LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ     = 1E-7          NCH     = 4.1589E17     VTH0    = -0.4002789
+K1     = 0.5772615     K2      = 0.026742      K3      = 0
+K3B    = 14.2532769    W0      = 1E-6          NLX     = 9.883899E-8
+DVT0W  = 0             DVT1W   = 0             DVT2W   = 0
+DVT0   = 0.6718731     DVT1    = 0.3118588     DVT2    = 0.1
+U0     = 118.0541064   UA      = 1.626518E-9   UB      = 1.229265E-21
+UC     = -1E-10        VSAT    = 2E5           A0      = 1.8109799
+AGS    = 0.4096261     B0      = 7.705744E-7   B1      = 2.657048E-6
+KETA   = 0.0212376     A1      = 0.5260122     A2      = 0.3207082
+RDSW   = 306.4304418   PRWG    = 0.5           PRWB    = 0.0612789
+WR     = 1             WINT    = 0             LINT    = 2.043723E-8
+XL     = -4E-8         XW      = 0             DWG     = -4.602158E-8
+DWB    = 8.005928E-9   VOFF    = -0.0992452    NFACTOR = 2
+CIT    = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB  = 0             ETA0    = 0.0331989     ETAB    = -0.0375363
+DSUB   = 0.7172358     PCLM    = 1.5224082     PDIBLC1 = 2.700462E-4
+PDIBLC2 = 0.0165863    PDIBLCB = -1E-3         DROUT   = 1.640424E-4
+PSCBE1 = 7.71553E9     PSCBE2  = 2.228426E-9   PVAG    = 5.1166248
+DELTA  = 0.01          RSH     = 6.7           MOBMOD  = 1
+PRT    = 0             UTE     = -1.5          KT1     = -0.11
+KT1L   = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1    = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL     = 0             WLN     = 1             WW      = 0
+WWN    = 1             WWL     = 0             LL      = 0
+LLN    = 1             LW      = 0             LWN     = 1
+LWL    = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO   = 6.92E-10      CGSO    = 6.92E-10      CGBO    = 1E-12
+CJ     = 1.173089E-3   PB      = 0.8524959     MJ      = 0.415401
+CJSW   = 2.217367E-10  PBSW    = 0.5936755     MJSW    = 0.2603391
+CJSWG  = 4.22E-10      PBSWG   = 0.5936755     MJSWG   = 0.2603391
+CF     = 0             PVTH0   = 1.425828E-3   PRDSW   = 0.9887283
+PK2    = 1.495689E-3   WKETA   = 0.0286138     LKETA   = -2.746502E-3
+PU0    = -1.2891258    PUA     = -5.395E-11    PUB     = 1E-21
+PVSAT  = -50           PETA0   = 1.003159E-4   PKETA  = -2.891811E-3 )
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Figure 3. Mosis parametric test results. Vendor: TSMC; feature size: 0.18 microns.

Table 2. Simulation results of the QFG-DVCC and comparison with other LV LP DVCCs in the literature.

Characteristics	Proposed	[21]	[40]	[41]	[42]
Supply voltage	±0.4 V	±0.5 V	±1.5 V	±1.5 V	±0.9 V
Power consumption	6.6 μW	10 μW	1.74 mW	2 mW	0.462 mW
DC current range	-50 to +50 μA	-30 to +30 μA	-1 to 1mA	—	
DC voltage range	-400 to +400 mV	-500 to +500 mV	-900 to 900 mV	—	—
3 dB bandwidth I_Z/I_X	19 MHz	10.2 MHz	120 MHz	80 MHz	598.4 MHz
Current gain I_Z/I_X	1	1	—	—	0.9999
3 dB bandwidth $V_X/V_{Y1}, V_X/V_{Y2}$	19 MHz	2.9 MHz, 3.3 MHz	85 MHz	—	588.84 MHz, 605.86 MHz
Voltage gain V_X/V_{Y1}, V_X/V_{Y2}	1	1	—	—	1, 0.999
Node X parasitic resistance: R_X/L_X	40 Ω/0.5 mH	70 Ω/3mH	9 Ω/ —	0.6 kΩ/ —	150.2 Ω/4.16 μH
Nodes Y1, Y2 parasitic resistances: $R_{Y1}/C_{Y1}, R_{Y2}/C_{Y2}$	2.3 GΩ/70 fF	0.933 TΩ/0.17 pF, 0.622 TΩ/0.25 pF	—	—	29.08 TΩ/3.86 fF, 29.08 TΩ/3.86 fF
Node Z parasitic resistance: R_Z/C_Z	6.26 MΩ/50 fF	55.7 MΩ/7.7 fF	—	14 kΩ/ —	5.03 MΩ/0.024 pF
CMOS technology	0.18 μm	0.18 μm	0.25 μm	0.25 μm	0.18 μm
Obtained results	Simulated	Simulated	Simulated	Simulated	Simulated

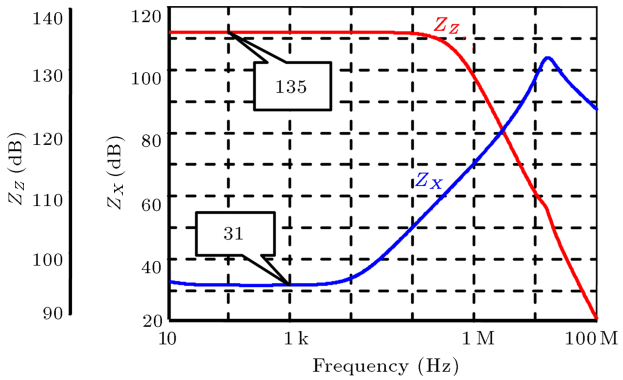

Figure 4. Frequency dependence of parasitic impedance of X and Z terminals.

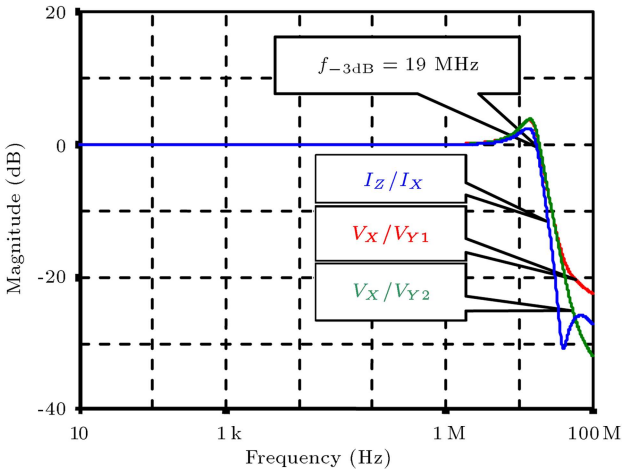

Figure 5. Frequency response of current gain I_Z/I_X and voltage gains $V_X/V_{Y1}, V_X/V_{Y2}$.

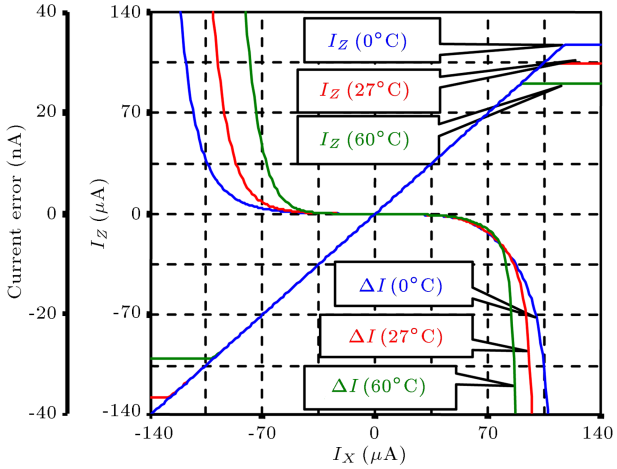

Figure 6. DC curves I_Z versus I_X and the current error for temperatures of 0, 27, and 60°C.

nal can be absorbed by a serial connection of this small parasitic resistance with the external grounded one [42].

Owing to these reasons, the block diagram of DVCC and its non-ideal model are studied and shown in Figure 9. The non-ideal model of DVCC consists of an ideal DVCC in addition to current (CF), Voltage Follower (VF), and the parasitic impedances of DVCC terminals. The parasitic impedances to each of the $Y1$, $Y2$, and Z terminals obtain a parallel combination of parasitic resistance and capacitance, whereas at X terminal, a serial combination of parasitic resistance and inductance in parallel to parasitic capacitance appears; the value of this parasitic capacitance is

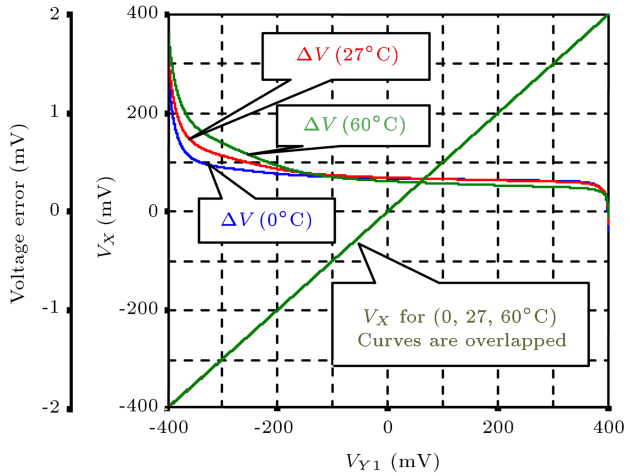

Figure 7. DC curves V_X versus V_{Y1} (with V_{Y2} grounded), showing the rail-to-rail operating range and the voltage error for temperatures of 0, 27, and 60°C.

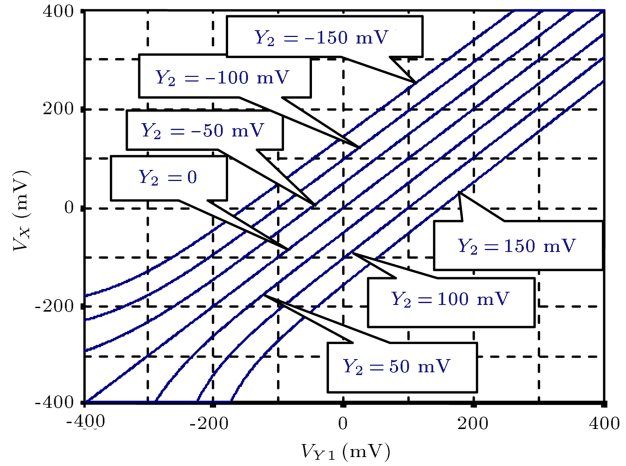

Figure 8. 7 DC curves V_X versus V_{Y1} for V_{Y2} = [-150, -100, -50, 0, 50, 100, 150] mV.

usually omitted as it affects response at a very high frequency. However, the values of these parasitic components could be easily calculated as in [21].

Ideally, the X terminal exhibits zero resistance, while the Y and Z terminals exhibit infinite resistance; practically, these resistances assume the finite value depending upon the internally used device parameters of the related active element [21,37]. However, the real QFG-DVCC can be characterized by the following hybrid matrix:

$$\begin{pmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_Z \end{pmatrix} = \begin{pmatrix} Z_X & \beta_1(s) & -\beta_2(s) & 0 \\ 0 & 1/Z_{Y1} & 0 & 0 \\ 0 & 0 & 1/Z_{Y2} & 0 \\ \alpha(s) & 0 & 0 & 1/Z_z \end{pmatrix} \begin{pmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{pmatrix}. \quad (5)$$

The voltage and current transfers of the DVCC are given by β_1(s), β_2(s), and α(s), respectively:

$$\beta_1(s) = \frac{\beta_{01}}{1 + s/w_{\beta 1}}, \quad (6)$$

$$\beta_2(s) = \frac{\beta_{02}}{1 + s/w_{\beta 2}}, \quad (7)$$

$$\alpha(s) = \frac{\alpha_0}{1 + s/w_{\alpha}}, \quad (8)$$

where β_{01}, β_{02}, and α_0 are the values of these transfers at low frequencies and $w_{\beta 1}$, $w_{\beta 2}$, and w_α represent their corresponding pole frequencies. The low-frequency voltage and current transfers are assumed to be $\beta_{0j} = 1 - \varepsilon vj$ for $j = 1, 2$ and $\alpha_0 = 1 - \varepsilon i$, where εvj and εi ($|\varepsilon vj| << 1$ and $|\varepsilon i| << 1$) represent voltage and current tracking errors of the QFG-DVCC, respectively. For a small-signal equivalent circuit, a straightforward analysis brings the following expressions to β_{01}, β_{02}, and α_0.

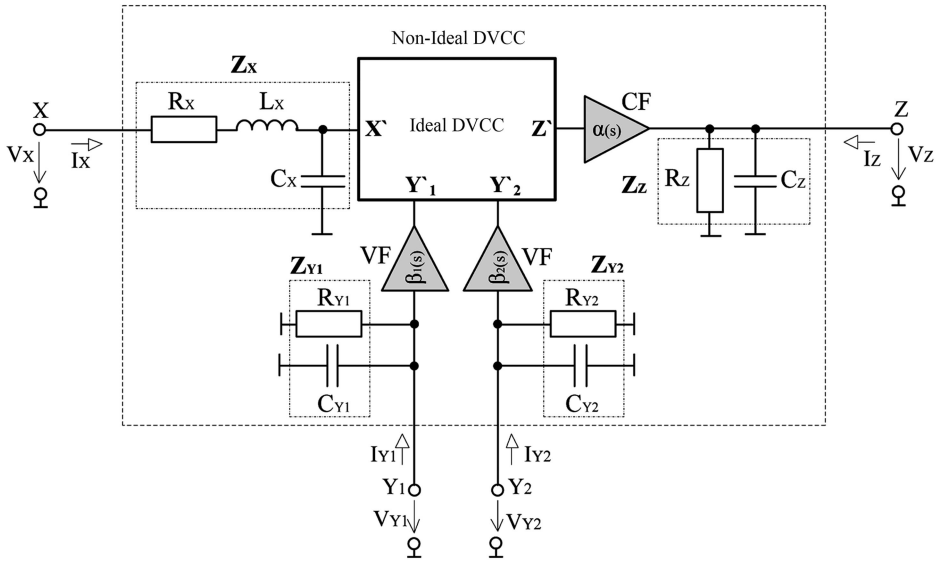

Figure 9. Model of non-ideal DVCC.

The voltage transfers β_{01} and β_{02} are:

$$\beta_{01} = \frac{V_X}{V_{Y1}} = \frac{g_{m,QFG,M1} r_{out1}(g_{mM10}+g_{mM11}) r_{out2}}{1+(g_{m,QFG,M2} r_{out1}(g_{mM10}+g_{mM11}) r_{out2})} \approx \frac{g_{m,QFG,M1}}{g_{m,QFG,M2}} \approx 1, \quad (9)$$

$$\beta_{02} = \frac{V_X}{V_{Y2}} = \frac{g_{m,QFG,M01} r_{out1}(g_{mM10}+g_{mM11}) r_{out2}}{1+(g_{m,QFG,M2} r_{out1}(g_{mM10}+g_{mM11}) r_{out2})} \approx \frac{g_{m,QFG,M01}}{g_{m,QFG,M2}} \approx 1, \quad (10)$$

where r_{out1} and r_{out2} are the output impedances of the first and second stages of QFG-DVCC and given as:

$$r_{out1} = \frac{1}{\frac{g_{o,M9c} g_{o,M9}}{g_{m,M9c}} + \frac{g_{o,M7}(g_{o,M3}+g_{o,QFG,M1}+g_{o,QFG,M02})}{g_{m,M7}+g_{mb,M7}}}, \quad (11)$$

$$r_{out2} = \frac{1}{\frac{g_{o,M10c} g_{o,M10}}{g_{m,M10c}} + \frac{g_{o,M11c} g_{o,M11}}{g_{m,M11c}+g_{mb,M11c}}}. \quad (12)$$

Then, the current transfer α_0 is:

$$\alpha_0 = \frac{I_Z}{I_X} = \frac{g_{m,M12}+g_{m,M13}}{g_{m,M10}+g_{m,M11}} \approx 1. \quad (13)$$

The impedance of the $Y1$ and $Y2$ terminals of the proposed QFG-DVCC is very high, because the quasi-floating-gate of the MOS transistor is used as the input to the amplifier stage. The resistance of the remaining terminal X is as follows:

$$R_X = \frac{1}{g_{m,QFG,M1} r_{out1}(g_{m,M10}+g_{m,M11})}. \quad (14)$$

Finally, the low-frequency resistance of the Z terminal can be expressed as:

$$R_Z = \frac{1}{\frac{g_{o,M12c} g_{o,M12}}{g_{m,M12c}} + \frac{g_{o,M13c} g_{o,M13}}{g_{m,M13c}+g_{mb,M13c}}}. \quad (15)$$

In Eqs. (9)-(15), g_m and g_{mb} denote the gate and bulk transconductances of MOST, $g_{m,QFG}$ denotes the transconductance of QFG-MOST, and g_o is the output conductance of the MOST.

4. Quadrature oscillator as an example of application

As an application example of the novel QFG DVCC with low voltage and ultra-low power, a quadrature oscillator using two active elements has been designed. Note that one of the first current-mode quadrature oscillators based on DVCC was presented in [45]. Quadrature sinusoidal oscillators are important circuits for various communication applications, wherein there is a requirement for multiple sinusoids that are 90° phase shifted, e.g., in quadrature mixers and single-sideband modulators or for measurement purposes in the vector generator or selective voltmeters [46,47]. Therefore, quadrature oscillators are widely used in many communications, signal processing, and instrumentation systems [48,49].

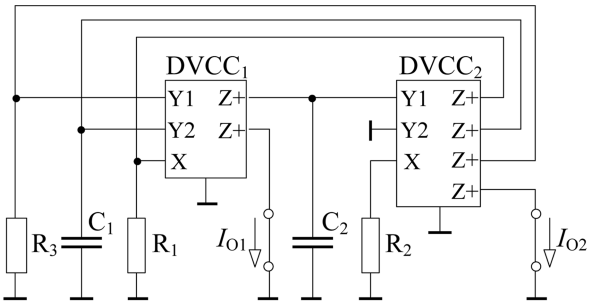

Figure 10. The proposed oscillator using two DVCCs.

The proposed structure is shown in Figure 10 and it can be seen that all passive elements are grounded, which make the circuit interesting for integrated implementation.

A routine analysis of the oscillator yields the following Characteristic Equation (CE):

$$CE: \ s^2 C_1 C_2 R_1 R_2 + sC_1(R_1 - R_3) + 1 = 0. \quad (16)$$

From Eq. (16), the Condition of Oscillation (CO) and the Frequency of Oscillation (FO) can be evaluated as:

$$CO: \ R_1 \leq R_3, \quad (17)$$

$$FO: \ f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{C_1 C_2 R_1 R_2}}. \quad (18)$$

From Relations (17) and (18), it is evident that the condition of oscillation can be controlled by R_3 without affecting the oscillation frequency. Similarly, by varying the value of the resistor R_2, only the oscillation frequency is affected.

The relationship between the output currents can be given as:

$$I_{O1} = jkI_{O2}, \quad (19)$$

where:

$$k = \omega_0 C_2 R_2, \quad (20)$$

ensuring that output currents I_{O1} and I_{O2} are quadrature (the phase difference $\phi = 90°$) and have equal amplitudes for $k = 1$.

5. Non-ideal analysis and sensitivity study

In this section, the non-idealities of the QFG DVCC shown in Eq. (5) and their influences on the proposed quadrature oscillator are studied. Assuming the non-ideal behavior of the active elements (non-unity voltage and current gains) and excluding parasitic resistances and capacitances, the characteristic equation, condition of oscillation, and frequency of oscillation change to:

$$CE: \quad s^2C_1C_2R_1R_2+\alpha_{01}\alpha_{02}\beta_{021}sC_1\left(R_1-\beta_{011}R_3\right) + \alpha_{01}\alpha_{02}\beta_{012}\beta_{021}=0, \tag{21}$$

$$CO: \quad R_1 \le \beta_{011}R_3, \tag{22}$$

$$FO: \quad f_0=\frac{1}{2\pi}\sqrt{\frac{\alpha_{01}\alpha_{02}\beta_{012}\beta_{021}}{C_1C_2R_1R_2}}, \tag{23}$$

and the affected relation between the output currents is:

$$I_{O1}=jk'I_{O2}, \text{ where } \quad k'=\frac{1}{\alpha_{02}\beta_{021}}\omega_0C_2R_2, \tag{24}$$

which means that the oscillator is still quadrature.

In Relations (21)-(23), it can be seen that the non-ideal behavior of the active elements affects both the condition and the frequency of oscillation; however, since the value of the resistor R_3 is always significantly higher than that of the resistor R_1, there is no problem in fulfilling the CO.

A sensitivity study forms an important index of the performance of any active network. The formal definition of sensitivity is as follows:

$$S_x^F=\frac{x}{F}\frac{\partial F}{\partial x}, \tag{25}$$

where F and x represent the frequency of oscillation f_0 and any of the passive elements (C_1, C_2, R_1, R_2) or active parameters (α_{0ij}, β_{0ij}). Using the above definition, the active and passive sensitivities of the proposed circuit are given as:

$$\left|S^{f_0}_{\alpha_{01},\alpha_{02},\beta_{012},\beta_{021},C_1,C_2,R_1,R_2}\right|=0.5. \tag{26}$$

Eq. (26) indicates that all the f_0 passive and active sensitivities are 0.5 in absolute value; hence, the circuit exhibits an attractive sensitivity performance.

For a complete analysis of the circuit, it is also important to take the main parasitic impedances and capacitances of the QFG DVCC into account. The proposed oscillator with the parasitic elements is shown in Figure 11. An analysis shows the dominant effect of the following parasitics:

- The non-zero input parasitic resistances R_{x1} and R_{x2} appearing at X terminals of DVCCs, where R_{x2} can be absorbed in the external resistor R_2, which is in serial with it;
- The parasitic resistance R_{ijp} appearing between the high output impedance terminal Z_j (where $j=1, 2, 3, 4$) of the ith DVCC and ground. Excluding R_{21p}, parasitic resistances are in parallel combination with those appearing at high input impedance terminal Y_{ik} (where $k=1, 2$), which are as follows:

$$R_{11p}=R_{y21}||R_{z11}, R_{22p}=R_{y12}||R_{z22} \text{ and}$$

$$R_{23p}=R_{y11}||R_{z23}.$$

Similarly, the parasitic capacitance C_{ijp} appears between the high output impedance terminal Z_j and ground. The parasitic capacitances C_{22p} and C_{11p} are absorbed into external capacitors C_1 and C_2, respectively, as they appear in parallel with them, where $C_{22p}=C_{y12}+C_{z22}$ and $C_{11p}=C_{y21}+C_{z11}$. In addition, the parasitic capacitances at high impedance terminals C_{y11} and C_{z23} are in shunt labeled as C_{23p} in Figure 12.

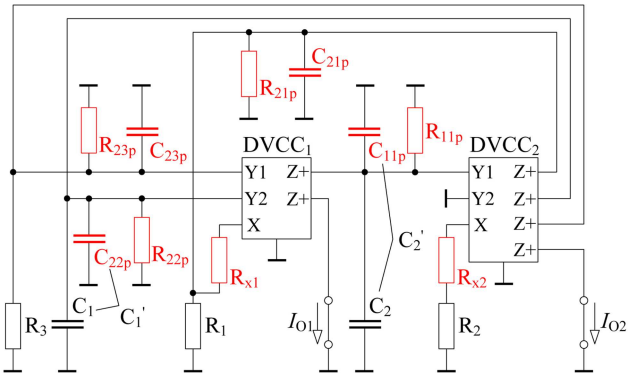

Figure 11. The proposed oscillator including the parasitic elements of the DVCC.

The effects of these parasitics can be alleviated

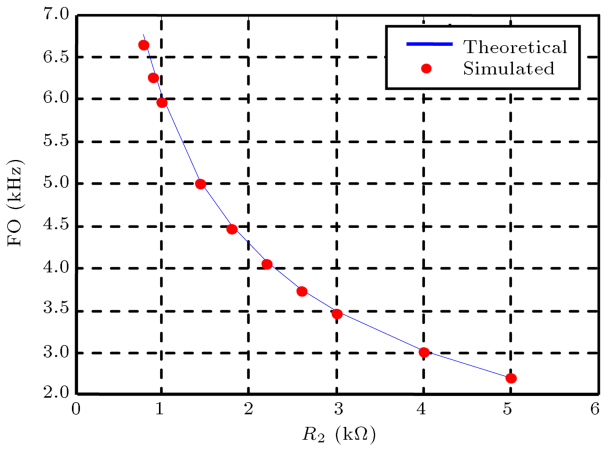

Figure 12. The variation of FO by R_2.

by considering the external capacitors C_1 and $C_2 >> C_{ijp}$; external resistors R_1, $R_3 << R_{21p}$, and R_{23p}; and the operating frequency $\omega_0 > \max[1/R_{22p}(C_1 + C_{22p}), 1/R_{11p}(C_2 + C_{11p})]$.

Considering the aforementioned parasitic effects, excluding parasitic resistances, and assuming that the current and voltage gains of active elements used are unities ($\alpha_{0ij} = 1$, $\beta_{0i1} = 1$, and $\beta_{0i2} = -1$), the ideal characteristic equation in Eq. (16) turns into:

$$CE: s^3 C_1' C_2' C_{3p} R_1 R_2 R_3 + s^2 R_1 \left[C_1'\left(C_2' R_2 + C_{3p} R_3 - C_{4p} R_3\right) + C_{3p} C_{4p} R_3\right] + s\left[C_1'\left(R_1 - R_3\right) + C_{3p} R_3 + C_{4p} R_1\right] + 1 = 0, \quad (27)$$

and the CO and FO in Relations (17) and (18) are modified as:

$$CO: C_1'^2 C_2' R_1 R_2 + C_1'^2\left(C_{3p} R_1 R_3 + C_{4p} R_3^2\right) + C_1' C_2' C_{4p} R_1 R_2 + C_1'\left[2 C_{3p} C_{4p} R_1 R_3 + C_{3p}^2 R_3^2\right] + C_{3p} C_{4p} R_3\left(C_{3p} R_3 + C_{4p} R_1\right) \le C_1'^2 C_2' R_2 R_3 + C_1'^2 R_3\left(C_{4p} R_1 + C_{3p} R_3\right) + R_3 C_1'\left(2 C_{3p} C_{4p} R_3 + C_{4p}^2 R_1\right), \quad (28)$$

$$FO: f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{R_1}\cdot\left[\frac{1}{C_1' C_2' R_2 + R_3\left[C_1'(C_{3p} - C_{4p}) + C_{3p} C_{4p}\right]}\right]}, \quad (29)$$

where $C_1' = C_1 + C_{22p}$ and $C_2' = C_2 + C_{11p}$.

It is found that the parasitics affect both the condition and the frequency of oscillation. However, these deviations are very small and can be ignored, since the value of external capacitors is much greater than C_{ijp}, the value of external resistors used is much lower than R_{ijp}, and the proposed oscillator operating frequency is much lower than the operating frequency of parasitics.

6. Simulation

In order to verify the workability of the oscillator designed, it has been simulated using SPICE. To the CMOS structure of the current conveyor in Figure 2, additional Z-terminals are added to create the required feedbacks in the oscillator circuit as shown in Figure 10. The values of the passive elements are set as follows:

$$C_1 = C_2 = 22\ nF, \quad R_1 = 1.43\ k\Omega, \quad R_3 = 2.00\ k\Omega.$$

The resistor R_2 is used to control the frequency of oscillation and in simulations, it varies in the range of 0.8 kΩ to 5 kΩ.

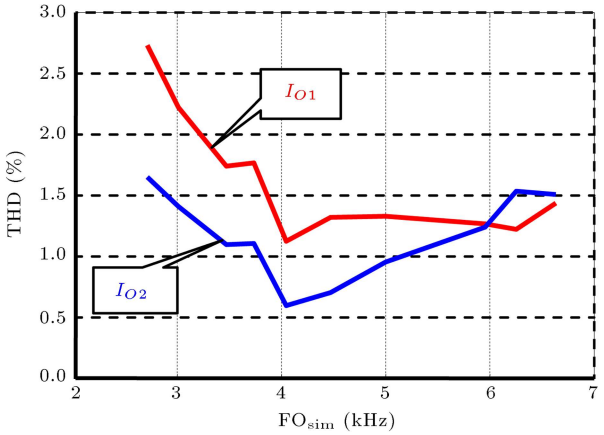

Figure 13. The variation of THD with the generated frequency.

Comparison of the theoretical value of the generated frequency with those given by simulations is shown in Figure 12.

The variation of the total harmonic distortion of the output currents I_{O1} and I_{O2} is shown in Figure 13. If the generated frequency is low, the required value of resistor R_2 needs to be high (see Figure 13) and it comes to voltage saturations of the current conveyor DVCC2. For high frequencies, the value of the resistor R_2 needs to be low (see Figure 13) and it comes to current limitations of the current conveyor DVCC$_2$. In both cases, the value of THD rises (Figure 13).

To complete the simulations, for $R_2 = 1.43$ kΩ (i.e., $f_{teor} = 5.06$ kHz), the steady state of the generated currents is given in Figure 14. The corresponding spectrum of these signals is shown in Figure 15. The real value of the generated signal is 5 kHz with THD of 1.33% and 0.96% for the currents I_{O1} and I_{O2}, respectively. The Monte Carlo mismatch analysis (50 runs) of the corresponding spectra of the oscillator

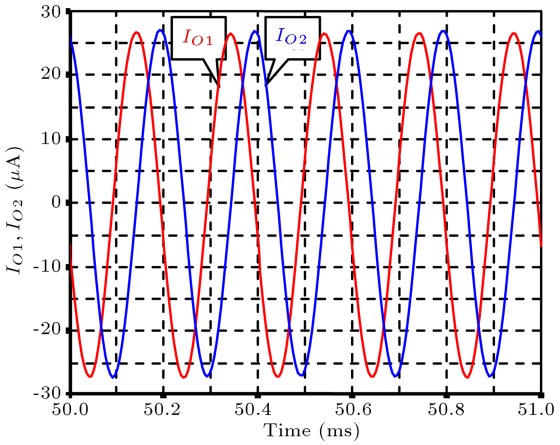

Figure 14. Steady-state oscillation waveforms of I_{O1} and I_{O2} for $R_2 = 1.43$ kΩ.

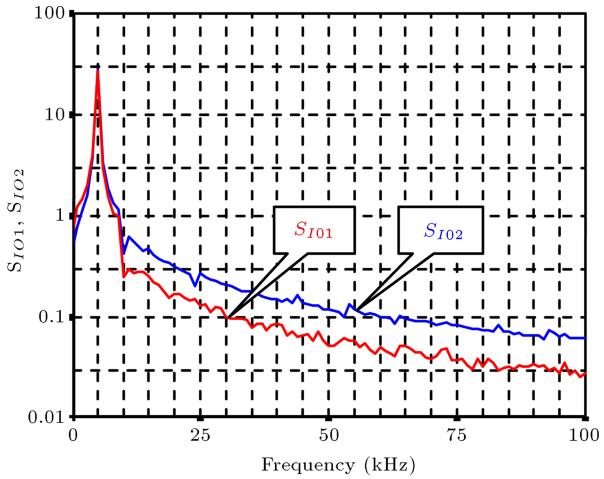

Figure 15. The corresponding spectra of the oscillator output currents I_{O1} and I_{O2}.

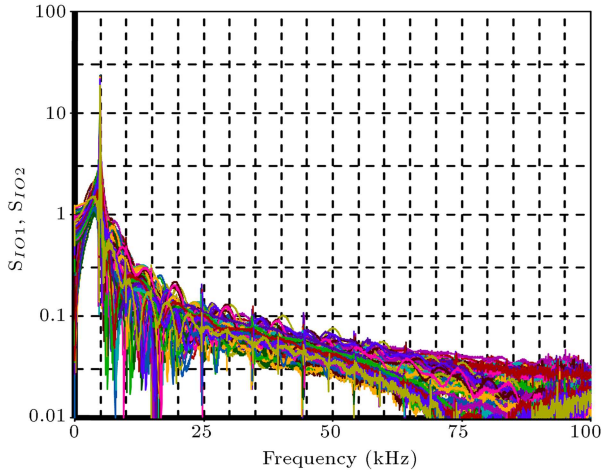

Figure 16. The Monte Carlo analysis of the corresponding spectra of the oscillator output currents I_{O1} and I_{O2}.

output currents I_{O1} and I_{O2} is shown in Figure 16 and it confirms the low circuit sensitivity to transistor mismatches.

The quadrature relationship between the generated waveforms has been verified using Lissagous figure and shown in Figure 17. The total power dissipation of the oscillator is 0.28 mW.

7. Conclusion

This paper deals with DVCC active element based on QFG technique. The proposed DVCC circuit can be used in various applications with attractive features, e.g., low-input impedance and high-output impedance, and it leads to superior properties in terms of cascading over other counterparts. Besides, low-voltage and ultra-low-power properties were achieved with sustaining optimum circuit performance. At the end, the richness of the oscillator possibilities inherent

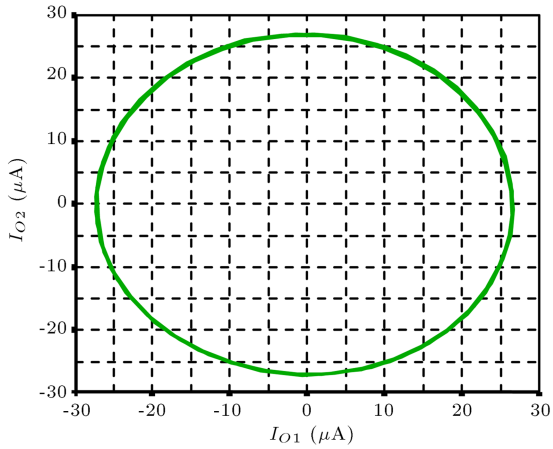

Figure 17. The quadrature relationship between the generated waveforms.

in producing quadrature signals and working with low-power consumption was demonstrated as well.

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