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New HCI and TDDB sensors based on transition time monitoring

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Abstract. A new on-chip HCI sensor based on measurement of fall transition time difference due to HCI between a stressed and reference inverter is proposed that has very small resolution while output has high correlation with HCI effect. Based on this new idea, a novel TDDB sensor is also proposed that is capable to detect both soft and hard breakdowns while it has low area overhead and high sensitivity. Differential structure of both sensors eliminates the effect of common-mode environmental variation, such as temperature. 180 nm TSMC technology and 65 nm of PTM are used for simulation. Analysis confirms HCI and TDDB sensor performances with 17% and 15% errors, respectively, in comparison with simulation results. The implemented layout area of both sensors is $101 \times 18\ \mu m^2$.

1. Introduction

The parametric shifts or circuit failures caused by Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), and Time Dependent Dielectric Breakdown (TDDB) have become more severe with shrinking device sizes and voltage margins [1].

The HCI-stress impact on NMOSFETs has become a major reliability concern in digital circuit design. It is the result of electron trapping or interface-state generation induced by the ionization impact of channel carriers near the drain region and it causes the degradation of electrical parameters of a transistor when the transistor is switching [2].

The wear out of the insulating properties of silicon dioxide in the CMOS gate results in the formation of a conducting path through the oxide to the substrate. Due to the presence of this conducting path, it is no longer possible to control the current between drain and source by controlling the gate voltage. With the technology scale down, the gate oxide thickness of CMOS devices decreases as well. Moreover, the saturating trend for supply voltage scaling results in a large electric field in the gate oxide, which forms tunneling currents. The lifetime of a particular gate oxide thickness is determined by the total amount of charge that flows through the gate oxide by tunneling current. Therefore, current generation devices are more prone to oxide breakdown compared to larger technologies. Oxide break down can be categorized into HBD and SBD. HBD is considered as a catastrophic failure of the device and hence the entire circuit. Compared to HBD, the conductance of SBD is limited. Even though SBD will not cause a catastrophic failure of the device, it will result in variation of circuit performance [3].

These mechanisms must be studied in order to develop accurate reliability models, which are used to design robust circuits. Another option for addressing aging effects is to use on-chip reliability monitors that can trigger real-time adjustments to compensate for lost performance or device failures [1]. In previous

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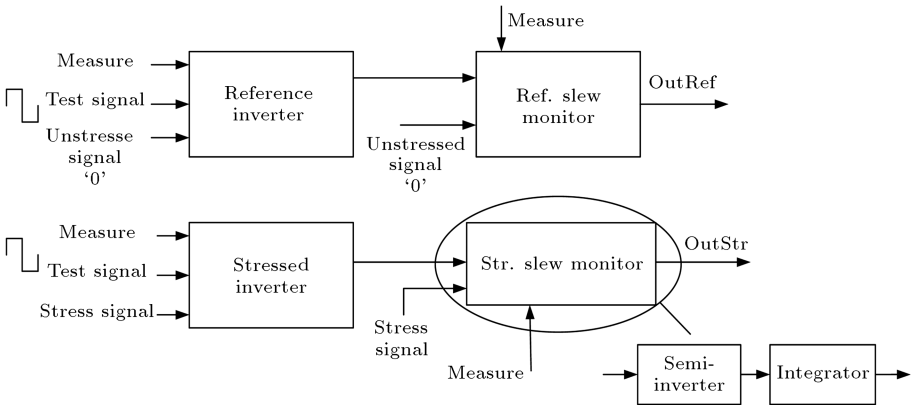

Figure 1. Block diagram of the new on-chip HCI sensor.

research, large number of NBTI monitoring circuits are proposed, but the numbers of HCI and TDDB sensors are lower.

In [2], an HCI sensor is proposed based on the phase difference between stressed and reference oscillator, and supply voltage of the stressed one is changed due to HCI affect; but in this sensor, the effect of all aging phenomena is mixed up and observed in output. Another sensor which measures frequency change of ring oscillator due to HCI is proposed in [4], but this method averages out the HCI across all PMOS transistors of the ring oscillator, resulting in loss of statistical information. These methods require a large number of oscillator stages to produce nearly-identical baseline frequencies, which increases the area of the sensors [5].

In [6], we have proposed a new NBTI sensor with the use of rise transition time monitoring that eliminates many disadvantages of the previous NBTI sensors and provides a high correlation between output and the desired aging effect. Fortunately, we could use the main idea of this NBTI sensor and propose a new HCI sensor, too.

About TDDB sensor, Singh et al. [7] proposes a TDDB sensor in which leakage current of PMOS changes the frequency of Schmitt-trigger oscillator. It has small area but consumes high power. Sensor in [4] only alarms when hard breakdown and failure occur and it is not useful for error prediction, because it cannot detect soft breakdowns. In [5], the sensor performs based on oscillator frequency change due to PMOS gate leakage current change affected by TDDB. This sensor has no differential structure to cope with PVT, hence a large number of sensors are required on-chip.

With the use of our new idea proposed in [6], a new TDDB sensor is proposed, too. The new TDDB sensor is capable to detect both soft and hard breakdowns. Also, output is only affected by TDDB, not mixed of aging phenomena, such as that happens in some of the previous sensors.

2. HCI sensor design

HCI is prominent in NMOS devices and causes threshold voltage (V_{th}) shift. The output fall slew of an inverter is a strong function of its NMOS drive strength. Also, it remains almost constant regardless of input transition time when it satisfies the Sakurai alpha-power model [8]. This section presents a new on-chip HCI sensor which consists of a reference inverter, a stressed inverter, and two new slew monitoring blocks, as shown in Figure 1. Each slew monitoring block consists of a semi-inverter and an integrator. Stress signal is applied to the input of stressed inverter during stress period while the input of reference inverter is connected to GND which makes its NMOS free from device aging. In measurement period, both reference and stressed inverters have the test input signal. In stress period, V_{th} of NMOS in stressed inverter is degraded depending on voltage level, duty cycle, and the number of cycles of applied stress signal.

In measurement period, both inverters conduct test signal with specific transition time (e.g. 40 ps in this work). Because of aging in NMOS of stressed inverter, output fall transition time of this inverter is more than that in reference inverter. To reveal this difference, we propose the new semi-inverter circuit, as shown in Figure 2, which has a resistor in pull-up network. When the input of semi-inverter switches to low voltage signal, the transistor Mp1 will turn on. During input fall transition, both short-circuit and dynamic current pass through R1. With increase in fall transition time due to HCI, the current amplitude through R1 decreases, thus signal in node n1 of stressed semi-inverter is higher in amplitude compared to that in reference semi-inverter.

In the final stage, a simple charge-pump based integrator [9] is used. The signal generated in semi-inverter output controls the on time and drain current of Mp2. When Mp2 switches on, Mn2 and Mn3 also turn on and discharge Cl. Therefore, in measurement

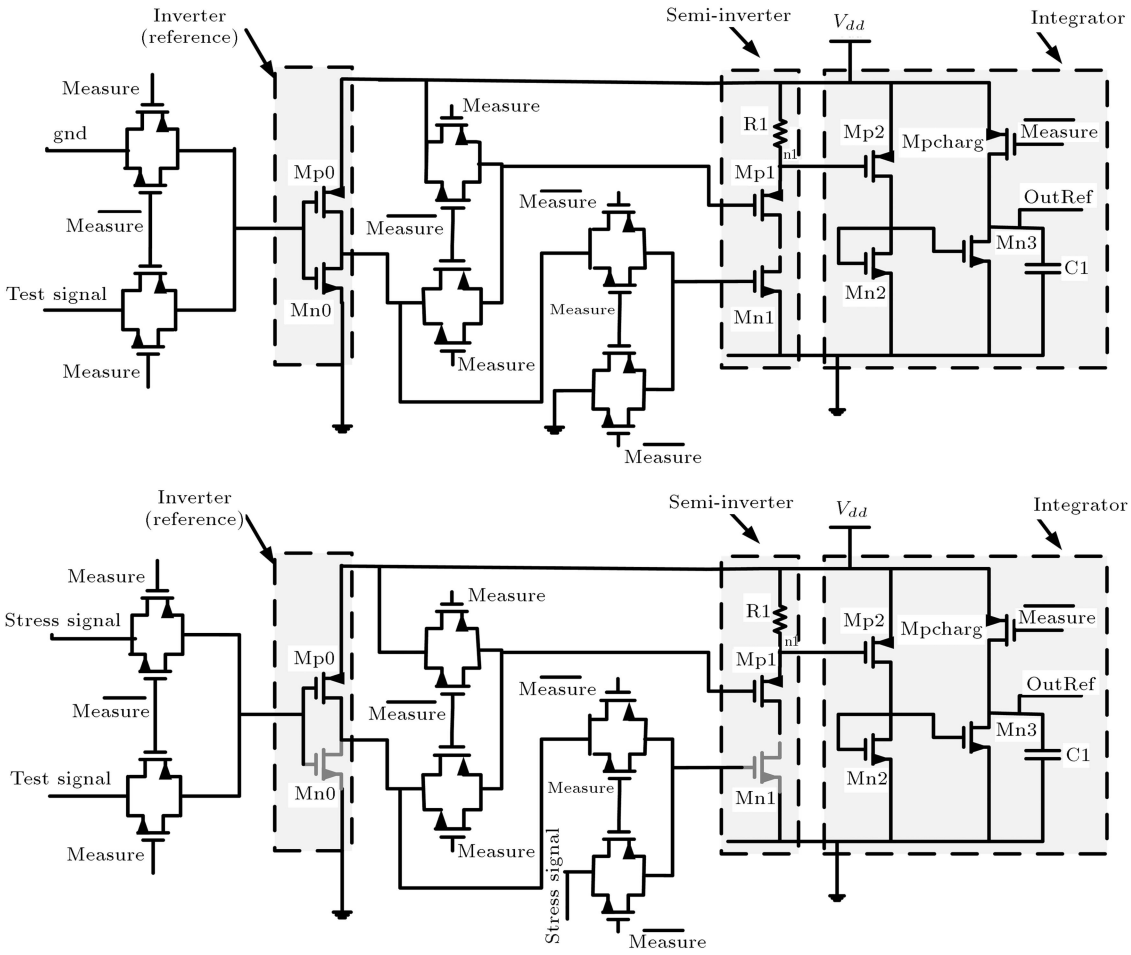

Figure 2. New HCI sensor circuit.

period, Cl will discharge proportional to n1 signal width and amplitude. Since n1 signal is different in the reference circuit and in the stressed one, the signals OutStr and OutRef are different. This difference is directly related to HCI effect in inverter. The integration time constant in integrator depends on C1 and Mn3 currents and can be tuned as required. In this design, the size of Mn3 and C1 are chosen for a small time constant such that the output will not reach GND before the measurement of proper number pulses of test signal. This issue will be explained further in the next section.

When sizing semi-inverter, it is important to note that the voltage amplitude at n1 should be low enough for Mp2 to be turned on. Output of integrator is charged to V_{dd} through the transistor Mpcharg when stress period starts. To have an accurate HCI sensor, aging in NMOS of semi-inverter and integrator should be low or under control. This issue has been ignored in the previous proposed HCI sensors. In this work, we control the HCI in all PMOS transistors by applying proper input signal switching (Figure 2). During stress period, NMOS of the reference semi-inverter is in relaxed mode. In measurement period, its input is connected to the output of reference inverter. The NMOS of stressed semi-inverter is in stressed phase during stress period, while in measurement period its gate is connected to the output of stressed inverter to measure the fall slew rate (Figure 3). In the most portion of the stress period, the semi-inverter output is high, therefore NMOS transistors in stressed integrator do not experience considerable aging effect, because they turn on for a very short time when semi-inverter input experiences fall transition during stress period. Also, with switch control, we have eliminated NBTI and HCI form PMOS transistors. Although one pulse of the test signal is sufficient to detect the difference in fall slew-rate, more than one pulse is employed to measure the fall transition difference. This improves the sensor sensitivity and gain. Thus, final difference between OutRef and OutStr is the cumulative difference of all measured pulses that makes a stepwise waveform in output (Figure 4). In this work, for sufficient sensitivity, we measure the fall slew difference of 24 pulses in test signal during each measurement period for 180 nm technology. So we have 24 step levels in OutRef and OutStr.

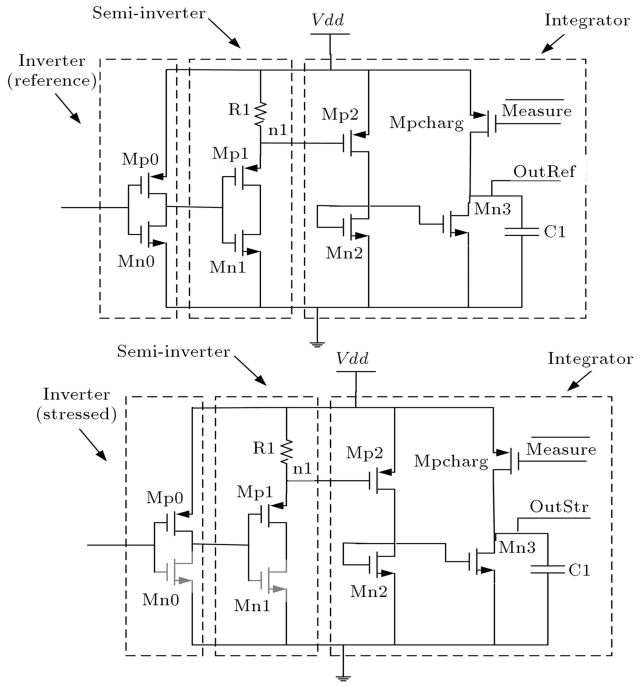

Figure 3. HCI sensor circuit in measurement mode.

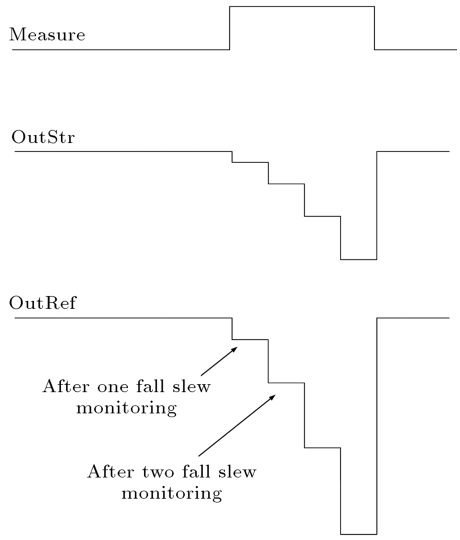

Figure 4. The waveform of stressed and reference circuit output signals.

3. HCI sensor analysis

As a verification of this research, when we do not have any fabrication chance, sensor performance analysis is the best approach.

The output fall transition time of inverter ($\tau_{\text{fall-out}}$) can be computed by:

$$\tau_{\text{fall-out}} = \frac{C_L.V_{dd}}{I_{\max}}, \tag{1}$$

where C_l is the output loading capacitance, and $I_{\max}$ is the maximum value of the discharging current, when the inverter satisfies Sakurai condition (fast input transition time with reasonable loading) based on [10]:

$$\tau_{\text{fall-out}} = \frac{C_L V_{dd}}{K_n W_n (V_{gs} - V_{thn})}, \tag{2}$$

where K_n is the transistor conduction factor defined for $\alpha = 1$, and V_{thn} and W_n are threshold voltage and width of Mn0. The change of $\tau_{\text{fall-out}}$ because of HCI in Mn0 is:

$$\Delta\tau = \tau_{\text{fall-out}} \frac{\Delta V_{thn}}{V_{dd} - V_{thn} - \Delta V_{thn}}, \tag{3}$$

where $\tau_{\text{fall\_out0}}$ is the initial output fall transition time of inverter and ΔV_{thn} is the HCI degradation.

In semi-inverter, the input transition time affects the current passed through R1, therefore the maximum current passes through R1 can be calculated based on [10] similar to non-Sakurai inverter (with slow input). Therefore:

$$I_{\max\_R1} = \sqrt{\frac{K_p.W_p.V_{dd}^2.C_L}{(1 + RK_p.W_p)\tau_{\text{in}}}}, \tag{4}$$

where K_p and W_p are parameters of Mp1; C_L is the load capacitor of semi-inverter; and τ_{in} is the input fall transition time of semi-inverter (same as the output fall initial transition time of inverter). The result of Eq. (4) is:

$$\Delta I_{\max} = \sqrt{\frac{K_p.W_p.V_{dd}^2.C_L}{(1 + RK_p.W_p)}} \left(\frac{1}{\sqrt{\tau_{\text{in}}}} - \frac{1}{\sqrt{\tau_{\text{in0}}}} \right), \tag{5}$$

where τ_{in0} is the initial input fall transition time of semi-inverter (before degradation), and τ_{in} is the input fall transition time of semi-inverter after degradation. After simplification and use of Taylor expansion, decrease in $I_{\max}$ of R1, due to change of inverter $\tau_{\text{fall-out}}$, is:

$$\Delta I_{\max} = -\frac{I_{\max\,0}}{2}.\frac{\Delta\tau}{\tau_{\text{in}}}, \tag{6}$$

in which $\Delta\tau$ is calculated in Eq. (3). In integrator, Mp2 turns on when $V_{n1}(t) = R_1.I_{Mp1}(t) > |V_{thp}|$. In order to calculate the output voltage difference between reference and stressed circuit of sensor, it is necessary to obtain gate voltage of Mn3. In this sensor, Mn2 and Mp2 are always in the saturation region; also $I_{Mp2} = I_{Mn2}$. Thus by using of this equality, we can finally obtain:

$$V_d = V_{\text{drain}_{Mp2}} = V_{\text{drain}_{Mn2}}$$

$$= A + B\left(\frac{V_{dd}}{2} - V_{thp} - V_{gMp2}\right),$$

$$A = \frac{2 * \vartheta_{satn} C_{oxn} W_{Mn2} V_{thn}}{\vartheta_{satn} C_{oxn} W_{Mn2} - \vartheta_{satp} C_{oxp} W_{Mp2}},$$

$$B = \frac{2\vartheta_{satp} C_{oxn} W_{Mp2}}{\vartheta_{satn} C_{oxn} W_{Mn2} - \vartheta_{satp} C_{oxp} W_{Mp2}}, \quad (7)$$

in which ϑ_{sat} is velocity saturation, W is the width of transistor, and C_{ox} is the gate-oxide capacitance. Based on Eq. (7), with decrease in V_{gMp2}, V_{dMn2}, which is connected to V_{gMn3}, will increase; so Mn3 current decreases, therefore C_L discharges less in stressed circuit than reference circuit.

In the start of measurement time, the output (Mn3 drain) is V_{dd} and Mn3 is in the saturation region. Therefore, the difference voltage of OutStr and OutRef is:

$$V_{\text{out}\_str} - V_{\text{out}\_ref} = \frac{1}{C_L}\left(\int_0^{t_{on_{str}}} I_{Mn3_{str}} dt - \int_0^{t_{on_{ref}}} I_{Mn3_{ref}} dt\right), \quad (8)$$

in which t_{onStr} and t_{onRef} are the on time periods of Mn3_{ref} and Mn3_{str}. By using the equation and the approximation that t_{onstr} and t_{onref} are equal:

$$V_{\text{out}\_str} - V_{\text{out}\_ref} = \frac{K_n W_n}{C_1} \int_0^{t_{on}} B\left(V_{gMp2_{str}} - V_{gMp2_{ref}}\right) dt. \quad (9)$$

In order to calculate the above integral, we assume V_{gMp2} as a triangle which its height is changed due to HCI (Figure 5). So we have:

$$V_{out\_str} - V_{out\_str} = \frac{K_n W_n}{2C_L} B.t_{on}.\Delta V_{\max}. \quad (10)$$

We use Eq. (10) for the first steps while Mn3 is in saturation region. Even though the current of Mn3 during saturation region differs with change of V_{ds},

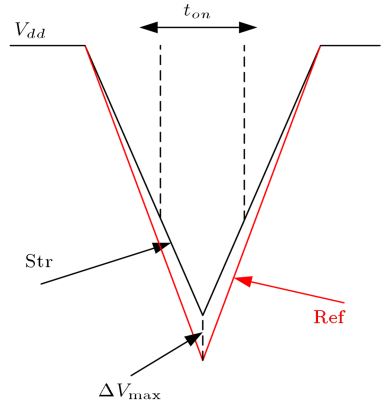

Figure 5. An approximation for voltage waveform in n1 node of the sensor.

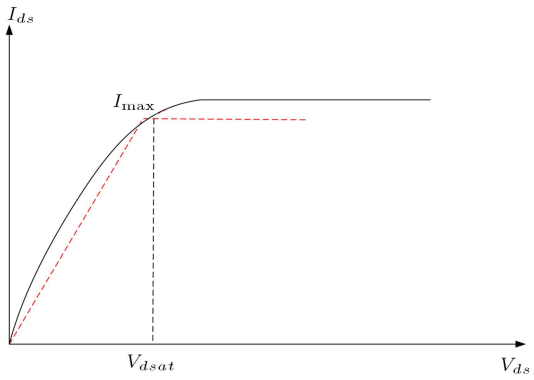

Figure 6. $I_d - V_{ds}$ curve of a transistor with special V_{gs}.

the change is small and we ignore it. With increase in output voltage, Mn3 enters linear region. In the last steps, if we use transistor current formula of linear region in Eq. (8), it gets so complicated. To avoid the complexity, we use an approximation as follows. In all of the output voltage steps in both reference and stressed circuits, V_{gs} of Mn3 is constant, so Mn3 current corresponds to only one $I_d - V_{ds}$ curve (Figure 6).

Thus, we can calculate the current in the linear region with $I = \frac{I_{\max}}{V_{dsat}} V_{ds}$ and define $\frac{V_{ds}}{V_{dsat}} = \text{LinCoeff}$ and use it in Eq. (8). Finally the gain or sensitivity of sensor that means the ratio of output voltage difference to V_{th} degradation (ΔV_{th}) is calculated as follows ($V_{\max 0} = R1.I_{\max 0}$):

$$\begin{aligned}\text{gain} = &\left(\frac{K_n W_n}{2C_{L1}} B.t_{on1}.\frac{V_{\max 0}}{2}.\frac{1}{V_{dd} - V_{thn} - \Delta V_{thn}}\right) \\ &+ \left(\frac{K_n W_n}{2C_{L2}} B.t_{on2}.\frac{V_{\max 0}}{2}.\frac{1}{V_{dd} - V_{thn} - \Delta V_{thn}}\right) \\ &+ \left(\frac{K_n W_n}{2C_{L3}} B.t_{on3}.\frac{V_{\max 0}}{2}.\frac{1}{V_{dd} - V_{thn} - \Delta V_{thn}}\right) \\ &+ \ldots + \text{LinCoeff}_{16}\left(\frac{K_n W_n}{2C_{L16}} B.t_{on16}.\frac{V_{\max 0}}{2}\right. \\ &\left..\frac{1}{V_{dd} - V_{thn} - \Delta V_{thn}}\right) + \text{LinCoeff}_{17} \\ &\left(\frac{K_n W_n}{2C_{L17}} B.t_{on17}.\frac{V_{\max 0}}{2}.\frac{1}{V_{dd} - V_{thn} - \Delta V_{thn}}\right) \\ &+ \ldots + \text{LinCoeff}_{24}\left(\frac{K_n W_n}{2C_{L24}} B.t_{on24}.\frac{V_{\max 0}}{2}\right. \\ &\left..\frac{1}{V_{dd} - V_{thn} - \Delta V_{thn}}\right). \end{aligned} \quad (11)$$

Comparison between analysis and simulation confirms that fortunately the proposed analysis follows the simulation result. The sensor performance with average error of 17% is shown in Figure 7.

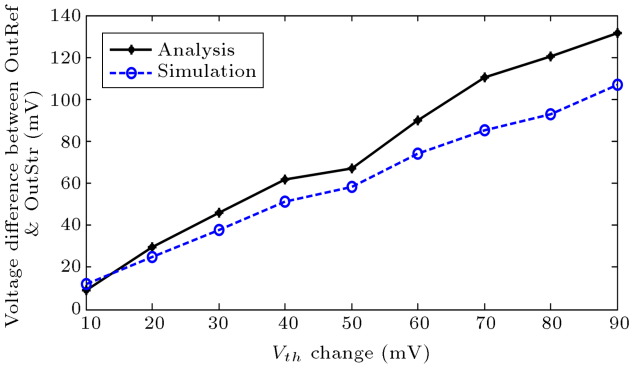

Figure 7. HCI sensor output in simulation and analysis of 180 nm TSMC.

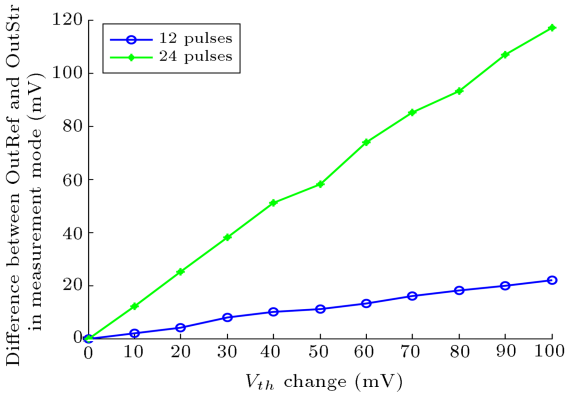

Figure 8. Differential output voltage of the new proposed sensor with respect to V_{th} degradation in 180 nm TSMC.

4. HCI sensor simulation result

The proposed sensor has been designed and simulated using 180 nm TSMC technology model. We have used 180 nm TSMC because it is a real and complete model for mismatch, variation, and other simulations. Even though the aging effects are not much pronounced in this domain of technology, we felt that it would still serve as a proof of concept to verify the sensor design.

A pulse signal with 50 MHZ frequency and 50% duty cycle and transition time up to 300 psec (for Sakurai model of inverter) is utilized for test signal in cadence. With increase in the number of measured pulses, the sensor gain and sensitivity are increased. In 180 nm, sensor has average gain about 1 mV/mV when 24 pulses are measured. Its resolution is about 2 mV change in V_{th} that causes 1 mV difference in output voltage. Figure 8 shows the differential output versus V_{th} change in NMOS of stressed inverter. Its average power consumption is 24 nW in stress mode and 50 μW during measurement mode.

Since both stress and reference circuits use an identical structure and are laid out next to each other, their dependency on process variation will be the same. To account for the variation in supply voltage (10%), channel length, width, resistance, and capacitance (5%), we have performed Monte Carlo simulation (1000 runs). Simulation shows a mean value of 1 mV/mV for average gain with standard deviation to mean ratio ($\frac{\sigma}{\mu}$) about 0.6%. Based on Monte Carlo simulation, the mismatch effect causes no distortion in sensor performance. Figure 9 shows the layout of the sensor. The proposed HCI sensor size is 101×18 μm^2.

Table 1 shows the comparison of the new sensor with recently reported HCI sensors. Obviously, the new sensor has higher sensitivity with smaller power consumption; also, the output of new sensor is only affected by HCI, not mixed of aging phenomena; and with proper signal controlling, statistical study is available in this sensor. Differential structure eliminated effect of environmental variation.

To ensure good performance of this sensor, it is also confirmed in 65 nm of PTM [11] technology model (Figure 10). This time, 18 pulses are measured to achieve proper sensitivity. Sensor's average gain is 1 mV/mV. Its resolution is about 0.5 mV change in V_{th} that causes 0.5 mV difference in output voltage.

The sensor's average power consumption is 0.4 μW in stress mode and 18 μW during measurement mode. The differential structure simulation confirmed that the temperature variation has negligible effect on the sensor performance (Figure 11).

5. TDDB sensor

The time to oxide breakdown for PMOS is one order of magnitude higher than NMOS [3], hence in this work, we consider TDDB on NMOS in sensor design. The wear out of insulating property of silicon dioxide forms a conducting path through oxide to the substrate. TDDB is modeled with a resistor in gate-source of

Table 1. Comparison between HCI monitoring circuits.

HCI sensor	Tech.	Area (μm^2)	Average power (μW)	Resolution	Type
[2]	45 nm	18.58×7.97	Stress mode: 8.57 Measure mode: 30.86	1 nsec/10 mV	NBTI/HCI monitoring
[4]	65 nm	214×551	N/A	< 1 ps (frequency resolution)	NBTI/HCI/TDDB monitoring
This work	180 nm	18×101	Stress mode: 0.024 Measure mode: 50	1 mV/2 mV	HCI monitoring

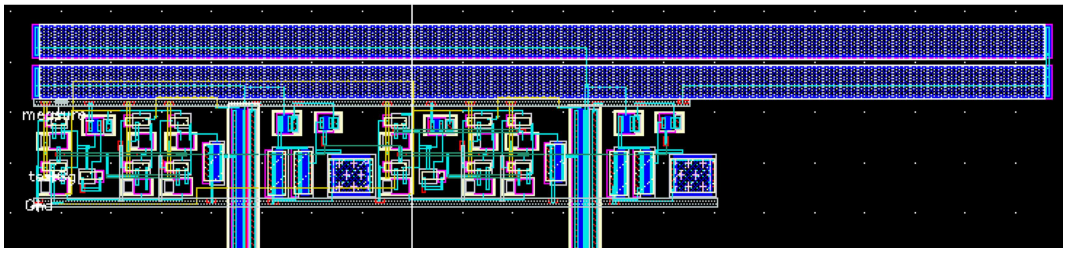

Figure 9. Layout of the proposed HCI sensor in 180 nm TSMC.

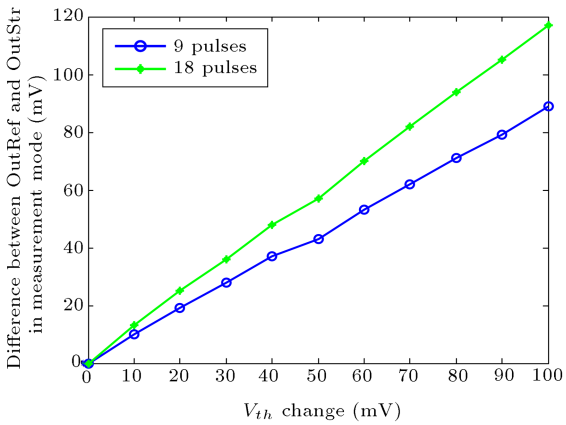

Figure 10. Differential output voltage of the new proposed sensor with respect to V_{th} degradation in 65 nm PTM.

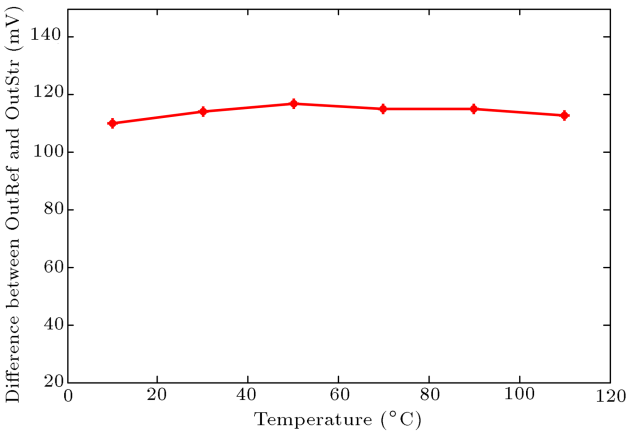

Figure 11. Temperature variation has negligible effect on HCI sensor performance and sensitivity.

affected transistor that causes a leakage current as in Figure 12. When TDDB is becoming worse on the device, the RBD value is also decreasing. Based on the published data, the break down resistor range is from GΩ (no TDDB) to a few KΩ (hard breakdown) [3].

Totally, the architecture of TDDB sensor is similar to HCI sensor, but in order to clarify TDDB effect, two inverters are necessary in each stressed and reference circuit. Figure 13 shows the TDDB sensor design. With proper signal control, only Mn1 is affected by TDDB and output is changed with its degradation; hence, other transistors are controlled via

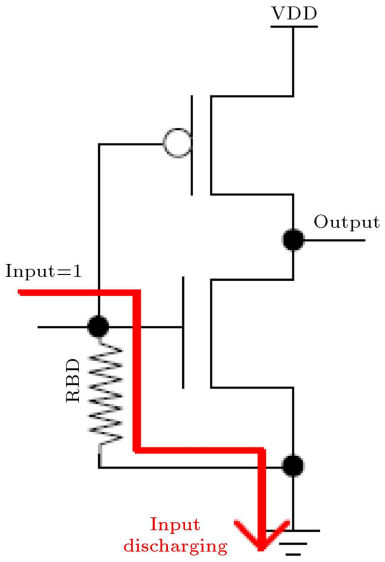

Figure 12. TDDB model in NMOS transistor [3].

switching. This switch control eliminates the other aging effect of other transistor in output that is an improvement with respect to previous sensors.

In this TDDB sensor, Mn1 of the second inverter in the stressed circuit is affected by oxide breakdown. Because of the modeled resistor breakdown, as shown in Figure 12, the voltage at gate of Mn1 will be charged to a lower voltage level than V_{dd} because of the resistor which increases the outfall transition time of this inverter that is the input of semi-inverter. After this stage, the performance of sensor is similar to HCI sensor in that the semi-inverter with integrator clears the change of this fall transition time with respect to the corresponding time in reference circuit. So we avoid repetition.

6. TDDB sensor analysis

The fall transition time in output of the second inverter of TDDB sensor is calculated based on Eq. (2). In the stressed part of sensor, Mn1 is affected by TDDB, so due to RBD leakage current, V_{gs} of Mn1 is lower than V_{dd}, so we have:

$$\Delta\tau_{fall-out} = -\tau_{fall-out0}\frac{\Delta V_{gs}}{V_{gs} - V_{th} + \Delta V_{gs}}. \qquad (12)$$

To calculate the value of ΔV_{gs} for Mn1 in the stress

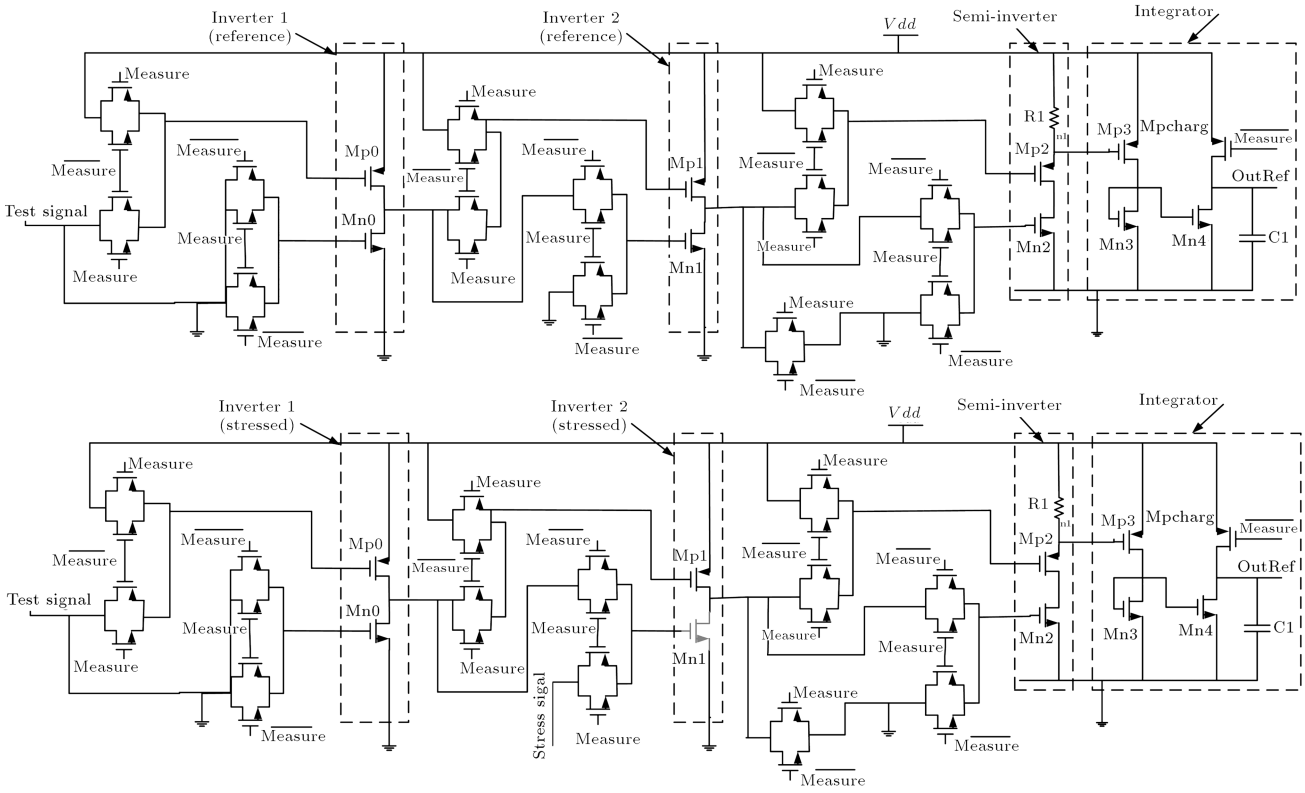

Figure 13. New TDDB sensor.

circuit, we use the following equation based on [12,13]:

$$\Delta V_{BD} = \frac{-R_{eq}}{R_{BD} + R_{eq}} V_{dd}, \tag{13}$$

in which V_{BD} is the voltage across RBD of Mn1 and is equal to V_{gs} of Mn1. Also, R_{eq} is the equivalent resistance of Mp0 and effective switches. Hence, more TDDB effect decreases RBD of Mn1 which causes decrease in voltage swing in the gate of the second inverter and results in fall transition time increment in output of the second inverter. The next stage analysis and performance is similar to HCI that we avoid to repeat.

Comparison between analysis and simulation for different values of RBD shows 15% error (Figure 14).

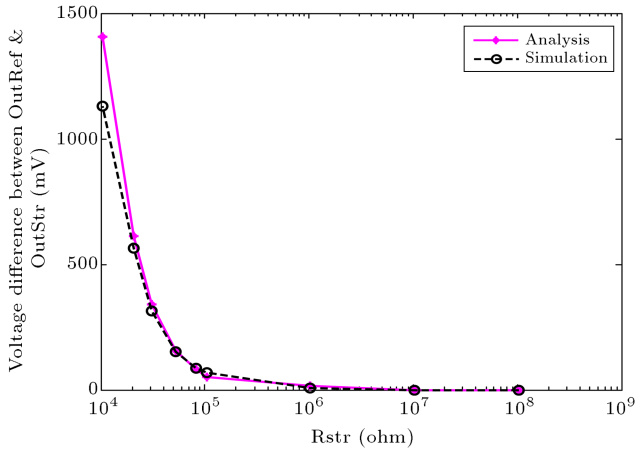

Figure 14. Comparison between analysis and simulation of the new TDDB sensor.

7. TDDB sensor simulation result

This sensor is simulated in cadence with 180 nm TSMC model. Figure 15 shows the simulation result. At first that no TDDB has occurred in Mn1, the output difference is zero. When soft breakdown occurs, non-zero voltage appears in output until hard breakdown happens in which RBD of Mn1 is about 10 kOhm in this time. So the leakage current of resistor increases and test signal will not be transformed to the output of the second inverter; hence, stress circuit has no stepwise signal in its output anymore.

In Figure 15, the mean value of sensor output difference with consideration of process and V_{dd} variation is shown. Fortunately, it has negligible effect on sensor performance and $\frac{\sigma}{\mu}$ is about 0.6%. Figure 16 shows the layout of the sensor. The proposed TDDB sensor size is $101 \times 18\ \mu m^2$.

Table 2 shows a comparison between the novel TDDB sensor and worthwhile previous TDDB sensors. Fortunately, the new sensor with ability to sense both hard and soft breakdowns provides low area and power with robustness against environmental variation, whereas the sensor of [7] suffers from high

Table 2. Comparison between TDDB sensors.

TDDB sensor	Tech.	Area (μm^2)	Average power(μW)	Type
[7]	130 nm	150	Stress mode: 469.5 Measure mode: 14.03	NBTI/TDDB monitoring
[4]	65 nm	214×551	N/A	NBTI/HCI/TDDB monitoring
[5]	45 nm	77.3	Stress mode: 0.009 Measure mode: 0.085	NBTI/TDDB monitoring
This work	180 nm	18×101	Stress mode: 0.15 Measure mode: 13	TDDB monitoring

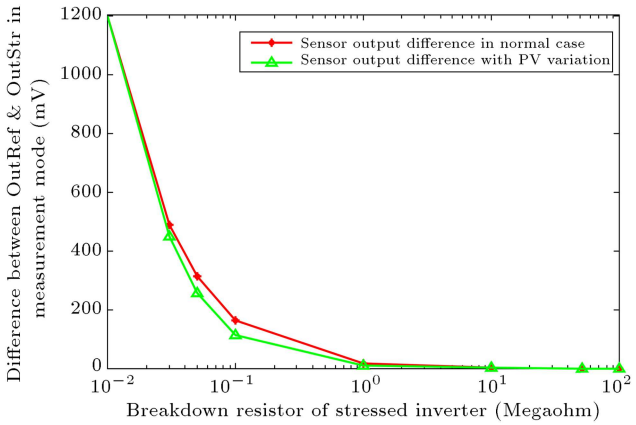

Figure 15. TDDB sensor output for different RBD in 180 nm of TSMC.

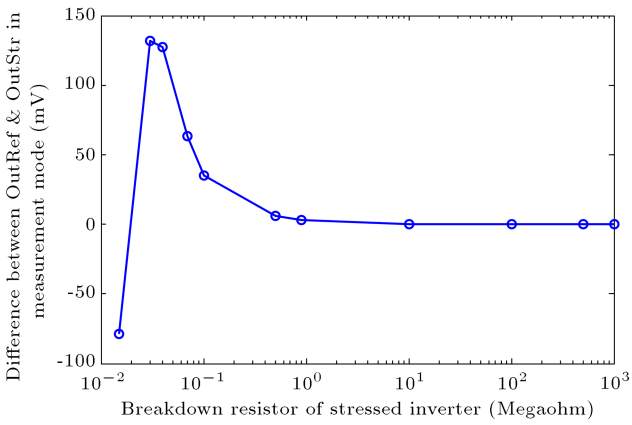

Figure 17. TDDB sensor output for different RBD in 65 nm of PTM.

power consumption, sensor of [4] only senses hard breakdown while sensing soft breakdown is essential to predict circuit failure, and sensor of [5] is affected by environmental variation.

Figure 17 shows the simulation result in 65 nm of PTM. Before an obvious soft breakdown output is zero, with more breakdown, a voltage difference appears in output to 15 Kohm of breakdown resistor that is the time in which hard breakdown occurs and disturbs the performance of circuit. In this technology, sensor average power consumption is 0.16 W in stress mode and 12 μW during measurement mode. The power report of this sensor in 65 nm and 180 nm confirms reasonable amount of power consumption.

Figure 18 shows that temperature does not disturb the performance of TDDB sensor. This is an important point of this sensor that due to its differential structure, the effect of common mode environmental variation will be eliminated.

8. Conclusions

This paper proposes a new high resolution HCI and TDDB sensor in 180 nm TSMC and 65 nm PTM of CMOS technology which measures the difference in fall slew degradation due to HCI and TDDB. The differential structure of the sensors limits the effect of environmental variation such as temperature. Both of the sensors' outputs have high correlation with their desired aging effect. The TDDB sensor can support both hard and soft breakdown measurements. Analysis of the HCI and TTDB sensor performance exhibits 17% and 15% error with respect to simulation results. The implemented layout area for both is 18×101 μm^2. It is

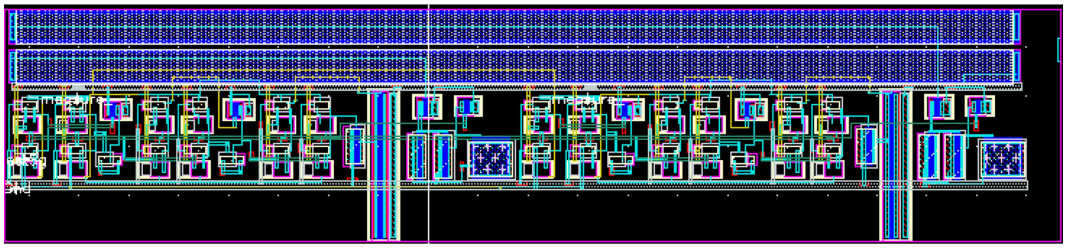

Figure 16. TDDB sensor layout in 180 nm TSMC.

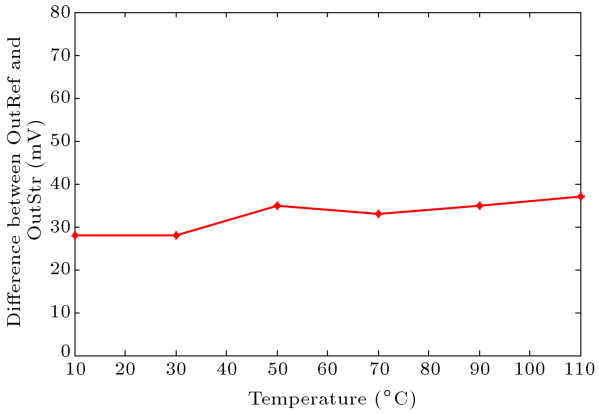

Figure 18. Temperature effect on TDDB sensor.

desirable for future to combine these new NBTI, HCI, and TDDB sensors in one sensor.

Acknowledgment

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