Scientia Iranica D (2015) 22(3), 1068–1076

SCIENTIA IRANICA

Sharif University of Technology
Scientia Iranica
Transactions D: Computer Science & Engineering and Electrical Engineering
www.scientiairanica.com

A new, single CCII- based, voltage-mode, first-order, all-pass filter and its quadrature oscillator application

F. Yucel[a] and E. Yuce[b,*]

a. *Department of Informatics, Akdeniz University, 07059, Konyaalti-Antalya, Turkey.*
b. *Department of Electrical & Electronics Engineering, Pamukkale University, 20070, Kinikli-Denizli, Turkey.*

Received 4 April 2014; received in revised form 12 October 2014; accepted 12 January 2015

KEYWORDS
All-pass filter;
Oscillator;
Voltage-mode;
Second-generation current conveyor;
MOS transistor.

Abstract. In this paper, a new Voltage-Mode (VM) first-order All-Pass Filter (APF) topology composed of only a grounded capacitor is proposed. The proposed APF uses a single, minus-type, second-generation, current conveyor (CCII-), which can be constructed by only five MOS transistors. It has low power consumption. The resonance frequency of the proposed APF can be adjusted by changing only a resistor value. However, it needs a single matching condition. As an application, a quadrature oscillator example is given. A non-ideality analysis for the proposed APF is also given. A number of time domain and frequency domain simulation results and an experimental test result are included to confirm the theory.

1. Introduction

All-Pass Filters (APFs), namely, phase shifters, are widely used in modern communication and instrumentation systems to change only the phases of electrical signals, while keeping their amplitudes constant at all frequencies. Previously, APF circuits were realized using Operational Amplifiers (OAs) [1-3], which have some drawbacks, such as slew-rate limitations. Afterwards, active building blocks, such as second-generation current conveyors (CCIIs) [4], were employed in many filter configurations, oscillators, inductor simulators, etc. A Voltage-Mode (VM) first-order APF circuit reported by Salawu (1980) employs only one plus-type CCII (CCII+) and four passive components [5], but a resistor and a capacitor are connected in series to the X-terminal of the CCII+ in this configuration. Also, all three resistors of [5] are floating. The VM APF circuit in [6] using a single minus-type CCII (CCII-) has high input impedance, but employs a floating capacitor. Other CCII+ based VM APF circuits employing one CCII+ and three passive elements are reported in [7], and they do not use a grounded capacitor. In [8], the CCII- based VM APFs are composed of a grounded capacitor, while the grounded capacitor is connected in series to the X-terminal of the CCII-. A VM APF realized by Pandey and Paul (2004) uses a single CCII- and three passive elements [9], and employs a floating capacitor. A recent paper has reported APF configuration employing only grounded passive elements [10]. Nevertheless, it uses two CCII+s and two capacitors. A first-order VM APF circuit with a variable voltage gain CCII has been proposed in [11], which has high input impedance, and employs a grounded capacitor. However, CCII is not standard and the APF has three critical passive component matching conditions. A first-order APF configuration using a Dual-Output CCII (DO-CCII) has been reported in [12]. This configuration includes a grounded capacitor, but the internal structure of the DO-CCII is complex. Another example of a first-order VM APF circuit with high

*. *Corresponding author. Tel.: +90 536 6894121*
E-mail addresses: fyucel@akdeniz.edu.tr (F. Yucel); erkanyuce@yahoo.com (E. Yuce)

input impedance and a grounded capacitor uses a modified CCII- (MCCII-)[13]. Nonetheless, the current gain of the MCCII- is -0.5, which is different from a standard current conveyor, and, moreover, the internal structure of the MCCII- is complex. A first-order VM APF circuit employing three MOS transistors, two resistors, and a grounded capacitor, is proposed in [14]. However, this circuit uses two bias voltages. Also, the resonance frequency of the circuit can be adjusted by the simultaneous change of two matched resistors. Two VM APF configurations in [15], respectively, include single DO-CCII and MCCII-, but, the internal structures of the DO-CCII and MCCII- are complex.

A single, dual-X, second-generation, current conveyor (DX-CCII) based VM APF has been proposed in [16]. However, the internal structure of the DX-CCII is complex. A first-order VM filter containing a Differential Difference Current Conveyor (DDCC) is reported in [17], wherein the internal structure of the DDCC is also complex. APF configurations using two Differential Voltage Current Conveyors (DVCCs) and having high input and low output impedances have also been reported in [18,19], while the internal structure of the DVCC is complex. The circuits of [20] and [21] are, respectively, composed of DDCC(s) and DVCCs. The APF structure of [22] employs a single Inverting Current Differencing Buffered Amplifier (ICDBA) whose internal structure is also complex. Recently, a dual output VM APF [23] using a single Voltage Differencing Inverting Buffered Amplifier (VDIBA) has been proposed, but it uses a floating capacitor.

In this work, a new VM first-order APF configuration, using only a grounded capacitor, is proposed. Only a resistor, but no capacitor, is connected in series to the X-terminal of the CCII-; thus, the proposed circuit can be operated at higher frequencies [24]. The resonance frequency of the proposed APF can be adjusted by changing only a resistor value. It dissipates low power, and needs a single matching constraint. As an example, a quadrature oscillator application employing only two grounded capacitors is given. A non-ideality analysis for the proposed APF is also given. A number of time domain and frequency domain simulation results and an experimental test result are accomplished to verify the claimed theory.

This paper is organized as follows: The introduction is given in Section 1, and CCII- is treated in Section 2. The proposed VM APF structure is presented in Section 3, and, in Section 4, parasitic impedance effects on the proposed APF are investigated. As an application example, a quadrature oscillator is given in Section 5. Simulation and experimental test results for the proposed circuits are given in Sections 6 and 7, respectively, and some concluding remarks are given in Section 8.

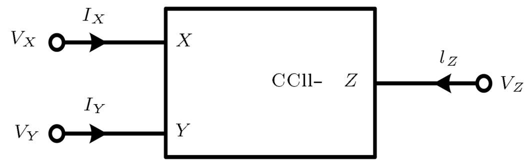


Figure 1. Electrical symbol of the CCII-.

2. Circuit description

The electrical symbol of the CCII- with three terminals is depicted in Figure 1. The CCII-, ideally defined by $V_X = V_Y, I_Y = 0$ and $I_Z = -I_X$, can be presented with the following matrix equation:

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} \beta & 0 \\ 0 & 0 \\ 0 & -\alpha \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \end{bmatrix}. \tag{1}$$

In Eq. (1), α and β are, respectively, frequency dependent non-ideal current and voltage gains, which are ideally equal to unity. At sufficiently low frequencies, α and β can be presented as $\alpha = 1 - \varepsilon_\alpha(|\varepsilon_\alpha| << 1)$ and $\beta = 1 - \varepsilon_\beta(|\varepsilon_\beta| << 1)$, where ε_α and ε_β are, respectively, current and voltage tracking errors, and are ideally equal to zero.

The internal structure of the CCII- [25] used in simulations of the proposed circuits is given in Figure 2. It includes only five MOS transistors, $M_1 - M_5$, and a bias voltage, V_B. M_1 and M_2 transistors are used to create a current mirror. It is assumed that all MOS transistors in Figure 2 are operated in a saturation region. The bulk of all MOS transistors are connected to the relevant sources to prevent a body effect.

3. The proposed voltage-mode, first-order, all-pass filter

The proposed VM first-order APF circuit, shown in Figure 3, employs only one CCII-, three resistors (one

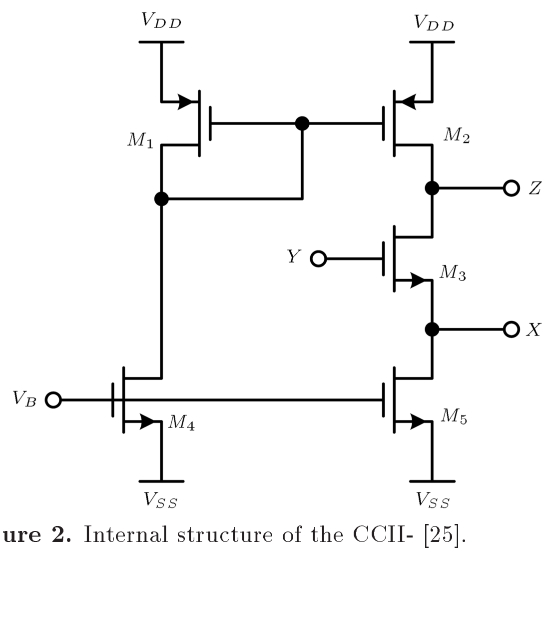


Figure 2. Internal structure of the CCII- [25].

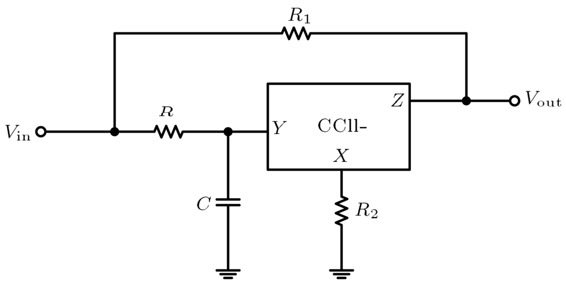


Figure 3. The proposed first-order voltage-mode APF circuit.

of them is grounded) and a grounded capacitor. In this circuit, $R_1 = 2R_2$ must be chosen to obtain the proper APF Transfer Function (TF), which can be ideally derived as:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{1 - sCR}{1 + sCR}. \tag{2}$$

Here, the phase response is evaluated as follows:

$$\varphi(\omega) = \pi - 2\tan^{-1}(\omega CR), \tag{3}$$

where the phase changes from 180° to 0° as the frequency varies from zero to infinity. In Figure 3, if R and C are interchanged, the proposed APF, employing a single floating capacitor and two grounded resistors, has the following TF and phase response, respectively:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{1 - sCR}{1 + sCR}. \tag{4a}$$

$$\varphi(\omega) = -2\tan^{-1}(\omega CR). \tag{4b}$$

Then, its pole frequency can be controlled via an electronically tunable grounded resistor, as the configurations given in [26,27].

Routine analysis of the circuit in Figure 3 with non-ideal gains gives the following TF:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{\alpha\beta\frac{R_1}{R_2} - 1 - sCR}{sCR + 1}, \tag{5}$$

where the phase response of the proposed APF can be obtained as:

$$\varphi(\omega) = \pi - \tan^{-1}\left(\frac{\omega CR}{\alpha\beta\frac{R_1}{R_2} - 1}\right) - \tan^{-1}(\omega CR). \tag{6}$$

It is important to note that one can reduce non-ideal gain and parasitic impedance effects using the methods discussed in [28].

4. Influence of the parasitic impedances

A non-ideal CCII- model, with only parasitic impedances, is depicted in Figure 4. The TF of the

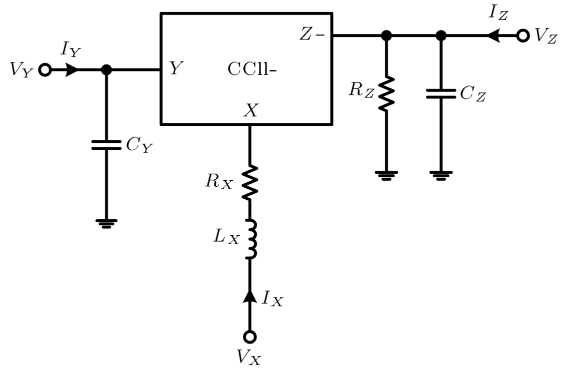


Figure 4. CCII- model with parasitic impedances.

proposed APF with the influences of the parasitic elements can be derived as:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{\frac{\frac{R_1}{R_2}}{(1+s(C+C_Y)R)\left(1+\frac{R_X}{R_2}+\frac{sL_X}{R_2}\right)} - 1}{1 + \frac{R_1}{R_Z} + sC_ZR_1}. \tag{7}$$

If R_1 and R_2 in Eq. (7) satisfy the following conditions:

$$R_1 << \frac{R_Z}{\sqrt{1 + \omega^2 C_Z^2 R_Z^2}}, \tag{8a}$$

$$R_2 >> \sqrt{R_X^2 + \omega^2 L_X^2}, \tag{8b}$$

the proposed APF operates properly.

Likewise, the operating frequency of the proposed APF is evaluated as follows:

$$f \leq \frac{1}{2\pi}\min\left\{\frac{\sqrt{0.01R_Z^2 - R_1^2}}{C_Z R_Z R_1}, \frac{\sqrt{\frac{R_2^2}{0.01} - R_X^2}}{L_X}\right\}. \tag{9}$$

5. A quadrature oscillator application

The quadrature oscillator in Figure 5 is designed as an application of the proposed APF. It consists of the proposed APF block, a CCII- element, a unity gain inverting amplifier, an extra grounded resistor, and an additional grounded capacitor. A Common-Source (CS) stage with diode-connected load, in Figure 6, is used as the unity gain inverting amplifier [29,30]. The

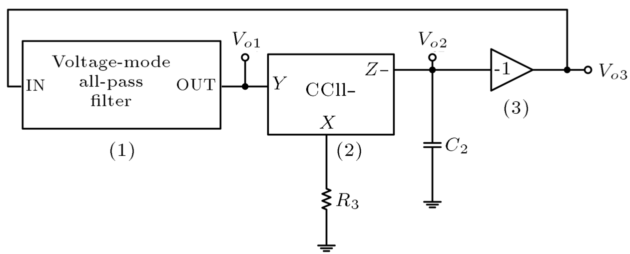


Figure 5. A quadrature oscillator circuit employing the proposed APF.

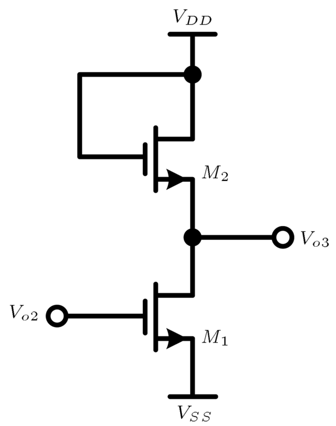


Figure 6. Unity gain inverting amplifier [29,30].

bulk of both transistors in the CS stage are connected to the relevant sources to prevent a body effect. The internal structure of the unity gain inverting amplifier is given in Figure 6. Further, V_{o1} and V_{o3} can, respectively, be defined by:

$$V_{o1} = \frac{j\omega C_2 R_3}{\alpha_2 \beta_2} V_{o2}, \tag{10a}$$

$$V_{o3} = -\beta_3 V_{o2}, \tag{10b}$$

where β_2 is the non-ideal voltage gain of CCII- and β_3 is the voltage gain of the inverting amplifier, which is ideally equal to unity [29,30]. Also, the aspect ratios of the NMOS transistors are selected equal to each other.

The characteristic equation for the proposed oscillator is evaluated as:

$$D(s) = s^2 C C_2 R R_3 + s\left(C_2 R_3 - \alpha_2 \beta_2 \beta_3 C R\right) + \alpha_2 \beta_2 \beta_3 \left(\alpha_1 \beta_1 \frac{R_1}{R_2} - 1\right) = 0. \tag{11}$$

The Oscillation Condition (OC) of the circuit can be expressed by:

$$C_2 R_3 = \alpha_2 \beta_2 \beta_3 C R. \tag{12}$$

The Oscillation Frequency (OF) of the proposed oscillator is calculated as:

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{\alpha_2 \beta_2 \beta_3 \left(\alpha_1 \beta_1 \frac{R_1}{R_2} - 1\right)}{C C_2 R R_3}}. \tag{13}$$

Here, the OF can be controlled via R_1 or R_2 without disturbing the OC. Apart from this, $\alpha_1 \beta_1 R_1 > R_2$ must be chosen in Eq. (13).

6. Simulation results

Simulations of the proposed APF are accomplished by the SPICE program. The proposed circuit is simulated using 0.13 μm IBM CMOS technology parameters [31]. Symmetrical DC power supply voltages are chosen as $V_{DD} = -V_{SS} = 0.75$V. The bias voltage, V_B, in Figure 2 is chosen as -0.07 V.

Table 1. Aspect ratios of the MOS transistors.

Transistor type	***W/L***
NMOS transistors	17.55 μm/1.3μm
PMOS transistors	3.9 μm/1.3μm

Aspect ratios (W/L) of the MOS transistors in Figure 2 are given in Table 1. The X-terminal parasitic resistor of the CCII- is found to be about 242.6Ω, and the value of L_X is very small. Passive components of the proposed APF in Figure 3 are chosen as $R = 5$ kΩ, $R_1 = 2$ kΩ, $R_2 = 1$ kΩ (effect of R_X is included) and $C = 20$pF, which also yield a pole frequency of $f_o \cong$ 1.59 MHz.

Voltage and current gain characteristics of the CCII- given in Figure 2, versus frequency, are drawn in Figure 7, where DC voltage and current gains are, respectively, $\alpha_o \cong 0.58$ and $\beta_o \cong 0.57$. Also, variations of the X-terminal parasitic impedance of the CCII- in Figure 2, against frequency, are drawn in Figure 8.

The gain and phase response of the proposed APF in Figure 3 is shown in Figure 9. The gain of the VM APF is approximately equal to -1.5 dB, which is acceptable.

A sinusoidal input voltage with a peak value of 100 mV at 1.59 MHz is applied to the proposed APF. Further, only the channel widths of M_3, M_4 and M_5 transistors, in Figure 2, with a step of 0.13 μm, are changed from 16.9 μm to 18.2 μm. The input and corresponding output voltages are given in Figure 10. It is seen from Figure 10 that the variations of parameter W affect the offset voltages of the proposed filter.

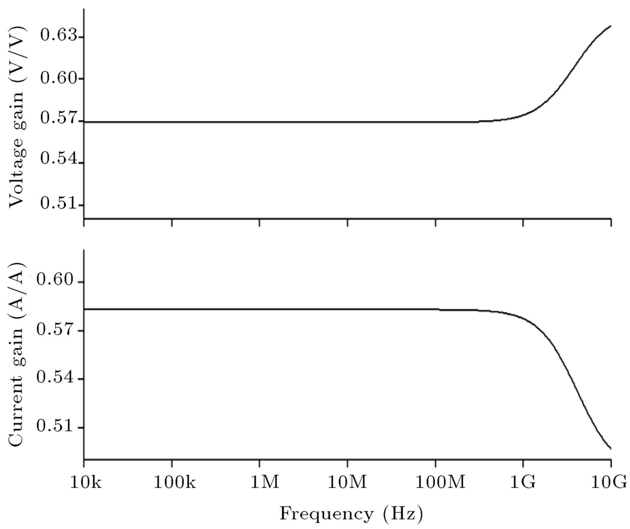


Figure 7. Variations of non-ideal voltage and current gains of the CCII- versus frequency.

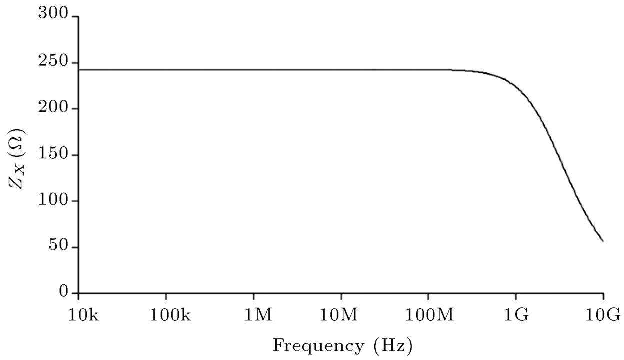


Figure 8. Variations of X-terminal parasitic impedance of the CCII- versus frequency.

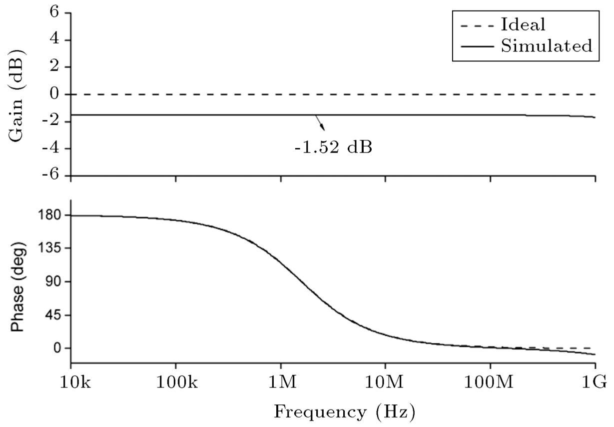


Figure 9. Gain and phase response of the proposed APF.

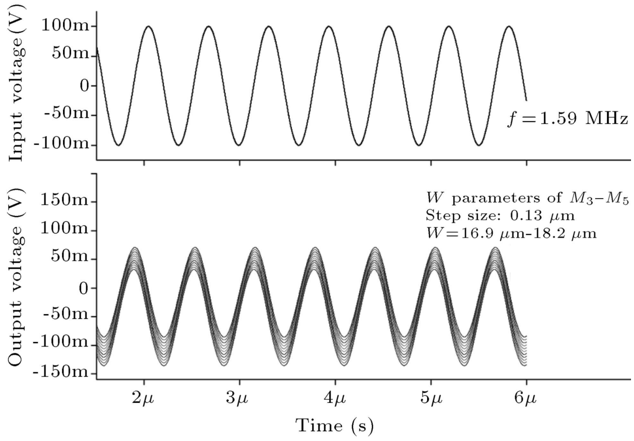


Figure 10. Analysis of the proposed APF circuit by changing W of the transistors M_3, M_4 and M_5.

A Monte Carlo analysis with fifty runs for 20% variations of the capacitor value of the proposed APF is achieved in which a sinusoidal input signal with peak value of 100 mV at a frequency of 5 MHz is applied. Figure 11 shows the input and corresponding output voltages. It is observed from Figure 11 that the change of the capacitor values slightly varies the resonance frequency of the proposed APF.

The total power dissipation of the proposed APF

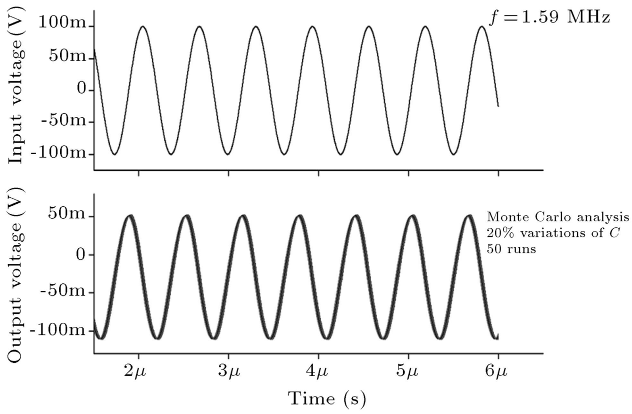


Figure 11. Monte Carlo analysis of the proposed APF circuit by changing C value.

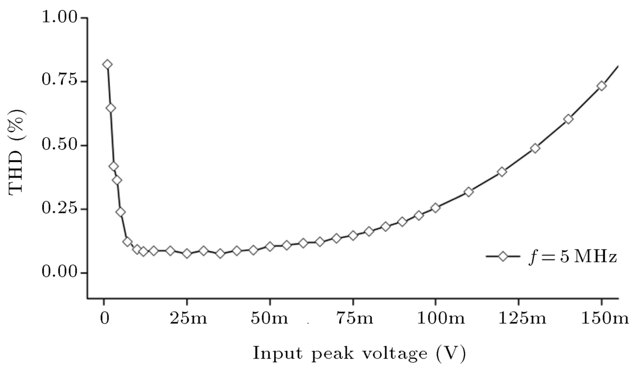


Figure 12. THD against peak value of the applied sinusoidal signal at 5 MHz frequency.

is calculated as 0.83 mW in simulations. The Total Harmonic Distortion (THD) variation, with respect to the peak value of the applied sinusoidal signal, at a frequency of 1.59 MHz, is depicted in Figure 12.

The quadrature oscillator in Figure 5 is simulated by choosing passive elements as $R = R_1 = 2$ kΩ, $R_2 = R_3 = 1.2$ kΩ and $C = C_2 = 20$ pF. The W/L ratios of NMOS transistors of the unity gain inverting amplifier in Figure 6 are chosen as 130 μm/1.3 μm. Output signals of V_{o1}, V_{o2} and V_{o3} at 4.54 MHz are depicted in Figure 13. Also, the change of the OF affects the peak value of the oscillator signal (V_{o3}), as drawn in Figure 14. It is seen from Figure 14 that if the OF increases, the peak value of the oscillator signal decreases.

The THDs of V_{o1}, V_{o2} and V_{o3} are, approximately, found as 2.8%, 2.04% and 3.45% at 4.54 MHz.

7. An experimental test result

The CCII- is realized using two commercially available active devices, such as AD844s [32]. The proposed APF constructed with two AD844s, three resistors, and a capacitor, is depicted in Figure 15, where input voltage with 1 V peak to peak at a resonance

Table 2. Comparison of the CCII based VM first-order all-pass filter circuits.

References	Number of CCII	Number of grounded resistors (number of total resistors)	number of grounded capacitors (number of total capacitors)	Technology	Power supplies
[5]	1	0 (3)	1 (1)	—	—
[6]	1	2 (3)	0 (1)	LF351	—
[7]	1	0 (2)	0 (1)	AD844	±12 V
[8]	1	0 (2) or 0 (1)	1 (1) or 2 (2)	—	—
[9]	1	1 (2)	0 (1)	AD844	±12 V
[10]	2	2 (2)	2 (2)	AD844	±12 V
[11]	1	1 (4)	1 (1)	0.35 μm	±3 V
[12]	1	0 (2)	1 (1)	0.35 μm	±1.5 V
[13]	1	0 (2)	1 (1)	0.35 μm	±2.5 V
[14]	1	0 (2)	1 (1)	0.35 μm	±1.5 V
[15]	1	0 (2)	1 (1)	0.13 μm	±0.75 V
This work	1	1 (3)	1 (1)	0.13 μm	±0.75 V

-: Not available.

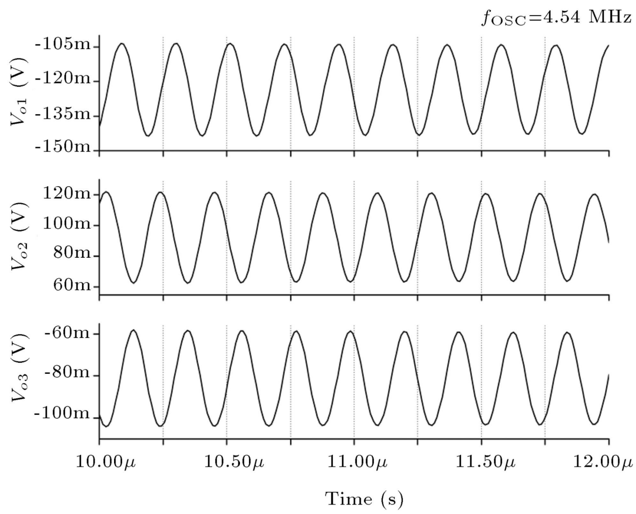


Figure 13. Output signals of the proposed quadrature oscillator.

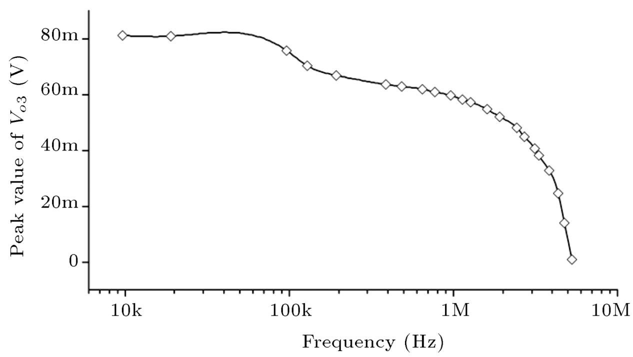


Figure 14. Peak value of V_{o3} versus frequency.

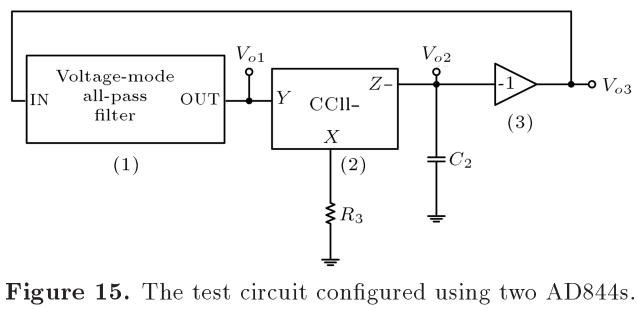
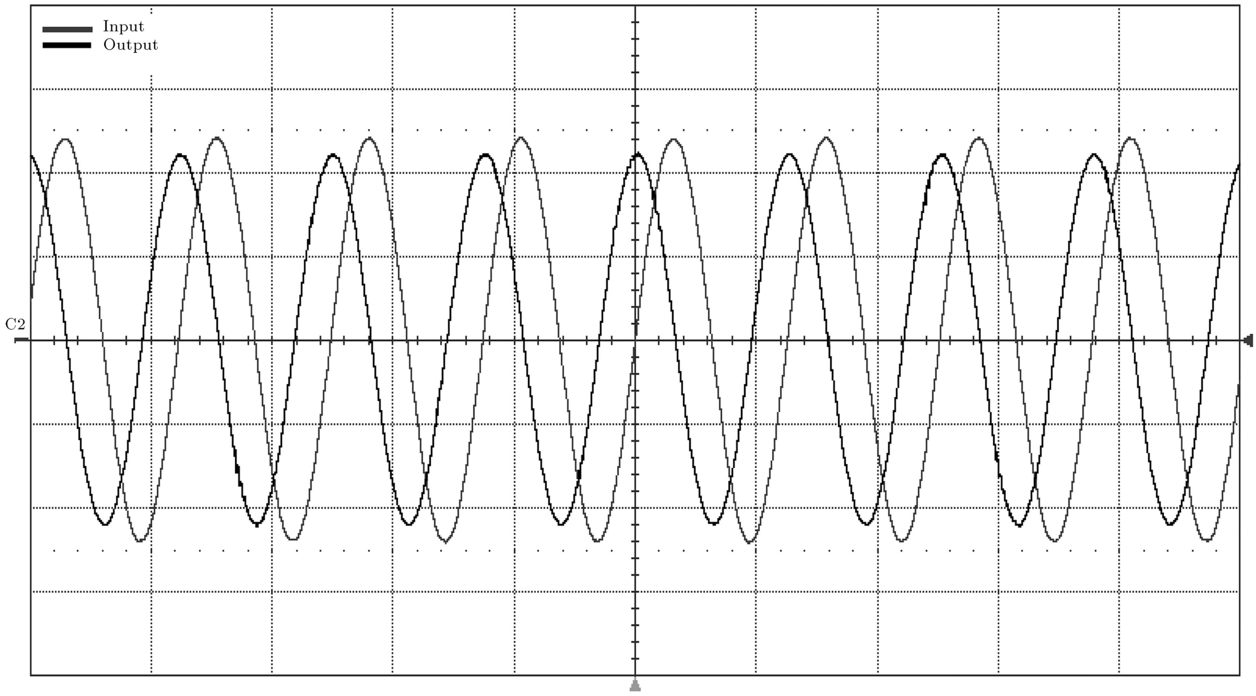


Figure 15. The test circuit configured using two AD844s.

frequency of 159 kHz is applied. Also, the symmetrical DC power supply voltages of the AD844s of Figure 15 in experimental tests are chosen as ±12V. The passive component values are also given in Figure 15. Hence, the experimental test is achieved and the time domain response of the proposed APF is given in Figure 16.

It is observed from Figures 9-14 and 16 that simulation and experimental test results agree quite well, whereas the differences among them can be attributed to the non-idealities of the active devices mentioned in the text.

The first-order, CCII based, VM first-order, APF circuits in related open literature and the one proposed are compared in Table 2.



Maesure:	P1: pkpk(C1)	P2: freq(C1)	P3: pkpk(C2)	P4: freq(C2)	P5: ampl(C2)	P6: ampl(C1)
value	964 mV	158.9248 kHz	888 mV	159.0514 kHz	873.5 mV	956.3 mV
mean	963.86 mV	158.998400 kHz	911.23 mV	158.998651 kHz	875.708 mV	953.592 mV
min	961 mV	158.5800 kHz	885 mV	155.6195 kHz	699.2 mV	796.7 mV
max	970 mV	159.3980 kHz	976 mV	162.2115 kHz	967.1 mV	967.9 mV
sdev	1.85 mV	108.831 kHz	18.84 mV	336.240 kHz	13.279 mV	19.998 mV
num	292	1.752e+3	292	2.044e+3	292	292
status	✔	✔	✔	✔	✔	✔

C1 F BwL DC1M 200 mV/div 0.00 mV ofst
C2 F BwL DC1M 200 mV/div 0.00 mV ofst
Timebase 0.0 µs 5.00 µs/div 50.0 kS 1.0 GS/s
Trigger C1 DC Auto 0 mV Edge Positive

Figure 16. Time-domain experimental test results.

8. Conclusion

In this study, a new VM, first-order, APF topology, including three resistors, a grounded capacitor and only a single CCII-, is proposed. The resonance frequency of the proposed APF can be adjusted by changing only a resistor value. The proposed circuit consumes low power. Nevertheless, it needs a single matching constraint. Also, it does not have high input and low output impedances. A quadrature oscillator using only grounded capacitors is treated as an application example. Non-ideal gain and parasitic impedance effects for the proposed APF are also given. A number of time domain and frequency domain simulation results and an experimental test result included verify the claimed theory well.

Acknowledgments

This work is partly funded by the Pamukkale University Scientific Research Project (BAP) Management Office; grant number 2012FBE033. Also, the authors would like to thank the anonymous reviewers and associate editor for their invaluable comments for improving the paper.

References

1. Ponsonby, J.E.B. "Active all-pass filter using a differential operational amplifier", *Electronics Letters*, **2**(4), pp. 134-135 (1966).
2. Dutta Roy, S.C. "RC active all-pass networks using a differential-input operational amplifier", *Proceedings of the IEEE*, **57**(11), pp. 2055-2056 (1969).
3. Schoonaert, D.H. and Kretzschmar, J. "Realization of operational amplifier all-pass networks", *Proceedings of the IEEE*, **58**(6), pp. 953-955 (1970).
4. Sedra, A. and Smith, K.A. "Second-generation current conveyor and its applications", *IEEE Transactions on Circuit Theory*, **17**(1), pp. 132-134 (1970).
5. Salawu, R.I. "Realization of an all-pass transfer function using the second generation current conveyor", *Proceedings of the IEEE*, **68**(1), pp. 183-184 (1980).

6. Liu, S.I. and Tsao, H.W. "The single CCII biquads with high-input impedance", *IEEE Transactions on Circuits and Systems*, **38**(4), pp. 456-461 (1991).
7. Toker, A., Ozcan, S., Kuntman, H. and Cicekoglu, O. "Supplementary all-pass sections with reduced number of passive elements using a single current conveyor", *International Journal of Electronics*, **88**(9), pp. 969-976 (2001).
8. Pal, K. and Rana, S. "Some new first-order all-pass realizations using CCII", *Active and Passive Electronic Components*, **27**(2), pp. 91-94 (2004).
9. Pandey, N. and Paul, S.K. "All-pass filters based on CCII- and CCCII-", *International Journal of Electronics*, **91**(8), pp. 485-489 (2004).
10. Horng, J.W. "Current conveyors based allpass filters and quadrature oscillators employing grounded capacitors and resistors", *Computers and Electrical Engineering*, **31**(1), pp. 81-92 (2005).
11. Yuce, E., Pal, K. and Minaei, S. "A high input impedance voltage-mode all-pass/notch filter using a single variable gain current conveyor", *Journal of Circuits, Systems and Computers*, **17**(5), pp. 827-834 (2008).
12. Metin, B. and Pal, K. "Cascadable allpass filter with a single DO-CCII and a grounded capacitor", *Analog Integrated Circuits and Signal Processing*, **61**(3), pp. 259-263 (2009).
13. Metin, B. and Cicekoglu, O. "Component reduced all-pass filter with a grounded capacitor and high-impedance input", *International Journal of Electronics*, **96**(5), pp. 445-455 (2009).
14. Yuce, E. "A novel CMOS-based voltage-mode first-order phase shifter employing a grounded capacitor", *Circuits, Systems and Signal Processing*, **29**(2), pp. 235-245 (2010).
15. Yucel, F. and Yuce, E. "CCII based more tunable voltage-mode all-pass filters and their quadrature oscillator applications", *International Journal of Electronics and Communications (AEÜ)*, **68**(1), pp. 1-9 (2014).
16. Minaei, S. and Yuce, E. "Unity/variable-gain voltage-mode/current-mode first-order all-pass filters using single dual-X second-generation current conveyor", *IETE Journal of Research*, **56**(6), pp. 305-312 (2012).
17. Ibrahim, M.A., Minaei, S. and Yuce, E. "All-pass sections with high gain opportunity", *Radioengineering*, **20**(1), pp. 3-9 (2011).
18. Ibrahim, M.A., Minaei, S. and Yuce, E. "All-pass sections with rich cascadability and IC realization suitability", *International Journal of Circuit Theory and Applications*, **40**(5), pp. 461-472 (2012).
19. Minaei, S. and Yuce, E. "Novel voltage-mode all-pass filter based on using DVCCs", *Circuits, Systems and Signal Processing*, **29**(3), pp. 391-402 (2010).
20. Metin, B., Pal, K. and Cicekoglu, O. "All-pass filters using DDCC- and MOSFET-based electronic resistor", *International Journal of Circuit Theory and Applications*, **39**(8), pp. 881-891 (2011).
21. Maheshwari, S. "High input impedance voltage-mode first-order all-pass sections", *International Journal of Circuit Theory and Applications*, **36**(4), pp. 511-522 (2008).
22. Metin, B., Pal, K. and Cicekoglu, O. "CMOS-controlled inverting CDBA with a new all-pass filter application", *International Journal of Circuit Theory and Applications*, **39**(4), pp. 417-425 (2011).
23. Herencsar, N., Minaei, S., Koton, J., Yuce, E. and Vrba, K. "New resistorless and electronically tunable realization of dual-output VM all-pass filter using VDIBA", *Analog Integrated Circuits and Signal Processing*, **74**(1), pp. 141-154 (2013).
24. Yuce, E. and Minaei, S. "Universal current-mode filters and parasitic impedance effects on the filter performances", *International Journal of Circuit Theory and Applications*, **36**(2), pp. 161-171 (2008).
25. Bruun, E. "A combined first- and second-generation current conveyor structure", *International Journal of Electronics*, **78**(5), pp. 911-923 (1995).
26. Wang, Z. "2-MOSFET transresistor with extremely low distortion for output reaching supply voltages", *Electronics Letters*, **26**(13), pp. 951-952 (1990).
27. Yuce, E., Minaei, S. and Alpaslan, H. "Novel CMOS technology-based linear grounded voltage controlled resistor", *Journal of Circuits, Systems and Computers*, **20**(3), pp. 447-455 (2011).
28. Yuce, E. "Negative impedance converter with reduced non-ideal gain and parasitic impedance effects", *IEEE Transactions on Circuits and Systems I- Regular Papers*, **55**(1), pp. 276-283 (2008).
29. Razavi, B., *Fundamentals of Microelectronics*, 1st Edn., New York, NY, USA, Wiley (2008).
30. Minaei, S. and Yuce, E. "High input impedance NMOS-based phase shifter with minimum number of passive elements", *Circuits, Systems, and Signal Processing*, **31**(1), pp. 51-60 (2012).
31. T97f SPICE BSIM3 Version 3.1 Parameters, https://www.mosis.com/cgi-bin/cgiwrap/umosis/swp/params/ibm-013/t97f_8hp_5lm-params.txt, Accessed date: 01/03/2014.
32. AD844 Datasheet, http://www.analog.com, Accessed date: 01/03/2014.

Biographies

Firat Yucel was born in 1982 in Kutahya, Turkey. He received the BSc and MSc degrees from Suleyman Demirel University (Isparta, Turkey) at Electronics and Computer Education and the PhD degree from Pamukkale University (Denizli, Turkey) at Electrical and Electronics Engineering in 2005, 2008 and 2015, respectively. He is currently a lecturer in the Department of Informatics of Akdeniz University, Antalya, Turkey. His current research interests include CMOS based circuits, computer-aided automation systems and artificial intelligence based optimization. He has served as reviewer for a number of international journals and on various scientific projects. He is author or co-author of several papers published in scientific journals or conference proceedings.

Erkan Yuce was born in 1969 in Nigde, Turkey. He received a BS degree from the Middle-East Technical University, an MS degree from Pamukkale University, Turkey, and a PhD degree from Bogazici University, Turkey, all in Electrical and Electronics Engineering, in 1994, 1998 and 2006, respectively. He is currently Associate Professor in the Electrical and Electronics Engineering Department of Pamukkale University, Turkey. His current research interests include analog circuits, active filters, synthetic inductors and CMOS based circuits. He is the author or co-author of about 100 papers published in scientific journals or conference proceedings.