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Minimum power Miller-compensated CMOS operational amplifiers

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Abstract. A new approach for the design of two-stage Miller-compensated CMOS op amps is presented. The paper studies the basic relations between power consumption, unity-gain bandwidth, the biasing region, technology parameters, and the external capacitive load. As a result, simple and efficient design guides are provided to achieve the minimum possible power consumption for the given specifications and for short-channel devices. It is shown that the conventional design procedures do not always result in minimum power op amps. The presented results are also verified by *Spectre* simulations.

1. Introduction

Integrated op amps are widely used in analog circuits and systems, such as amplifiers, active filters, and analog to digital converters. Among all available choices, Miller-compensated op amps have been the most popular topology used over the decades. The applications extend from extremely low-power biomedical circuits [1,2] to high frequency wireless transceivers [3-5], indicating both the maturity and the flexibility of the topology.

There are a vast number of papers and textbook chapters dedicated to the study of Miller-compensated op amps [6-10]. However, the op amp designers typically rely on either trial and error or traditional rule of thumb. For example, it is believed that the total needed power is proportional to the required gain-bandwidth product [11,12]. This is, however, not generally true, as will be shown in this paper. In order to enhance stability, an op amp designer may traditionally choose the dc current of the second stage, to be much higher than that of the first stage [10,13,14], which, again, as will be shown in this paper, is not always the best choice. Moreover, most existing op amp design guides are developed for long-channel device equations [10,14-16], hence, not applicable to modern transistors.

In this paper, we will analyze the popular Miller-compensated op amp to illustrate the fundamental relations between power consumption, bandwidth, stability, external load, and technology parameters. As a result, a simple approach is provided to minimize the power consumption of the op amp for the given design specifications. In Section 2, Miller-compensated op amps are modeled and analyzed, followed by derivation of the required total current in Section 3. Minimum power op amps are introduced in Section 4 followed by the verification of the results in Section 5. In Section 6, some additional design constraints are introduced, and, finally, the conclusion is given in Section 7.

2. Op amp model and analysis

A simplified model for two-stage Miller-compensated op amps is shown in Figure 1, where C_1 is the total parasitic capacitance at the inter-stage node,

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and C_2 is the total output capacitance, including the external load C_L. (For simplicity, the finite output conductances of the stages are ignored in the model shown in Figure 1. This introduces negligible error in the position of high frequency zero/poles that are used through our analysis.) The nulling resistor, R_Z, is included in the model to move the feed-forward zero towards the left-half complex plane [17].

For the op amp shown in Figure 1, the open loop gain can be found as:

$$T(s) = \frac{-g_{m1}g_{m2}\left[1+sC_C(R_Z-1/g_{m2})\right]}{s\left[s^2R_ZC_CC_1C_2+s(C_1C_2+C_1C_C+C_2C_C)+g_{m2}C_C\right]}, \quad (1)$$

which includes three poles and a single zero. It is well known that the power consumption of the op amp can be reduced, when the zero, z, is placed atop the first non-dominant pole, p_2 [18]. For a typical situation of $C_2 > C_1$, taking

$$R_Z = \frac{1}{g_{m2}} \times \left(1 + \frac{C_2}{C_C}\right), \quad (2)$$

results in a pole/zero doublet pair at:

$$p_2 = z = -\frac{g_{m2}}{C_2}. \quad (3)$$

Substituting Eq. (2) into Eq. (1) simplifies the transfer function as:

$$T(s) = -\frac{\text{GBW}}{s\,(1+s/p_3)}, \quad (4)$$

where p_3 (the non-dominant pole) and GBW are calculated as follows:

$$p_3 = -\frac{g_{m2}C_C}{C_1\,(C_2+C_C)}, \quad (5)$$

$$\text{GBW} = \frac{g_{m1}}{C_C}. \quad (6)$$

Finally, from Eq. (4), the phase margin can be approximated as:

$$\text{PM} \approx \tan^{-1}\left(\frac{p_3}{\text{GBW}}\right). \quad (7)$$

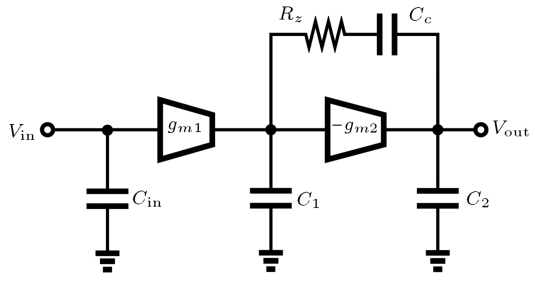

Figure 1. Miller-compensated op amp topology.

Note that the above phase margin is calculated by assuming that the op amp is used in a unity feedback configuration. In the appendix, however, the results are extended to other useful configurations.

In order to extend the analysis into the circuit level, without loss of generality, we consider a g_m stage as a single transistor, M_1, along with its load current source (see Figure 2). The transconductance, g_m, can be conveniently related to the bias current, I, by the transconductance efficiency, Γ [19], as:

$$g_m = \Gamma \times I. \quad (8)$$

Similarly, we express the input and output capacitances of the stage using the definition of the transit frequency, ω_T, as:

$$C_{gg} = g_m/\omega_T, \quad (9)$$

$$C_{dd} = \xi \times C_{gg}, \quad (10)$$

where ξ is the proportionality factor.

3. Required DC current

Eq. (7) implies that to achieve the desired closed-loop stability, the non-dominant pole, p_3, should be pushed above tan(PM) times the GBW. This, considering Eqs. (5) and (6), requires:

$$\frac{g_{m1}g_{m2}}{C_1(C_2+g_{m1}/\text{GBW})} \simeq \tan(\text{PM}) \times \text{GBW}^2, \quad (11)$$

which serves as our design constraint. The circuit components in Eq. (11) can be expressed in terms of the bias currents of the two stages (I_1 and I_2) and the g_m characterization parameters: Γ, ω_T, ξ. Defining $x \triangleq I_2/I_1$, we can write:

$$g_{m1} = \Gamma_1 \times I_1 = \Gamma_1 \times \frac{I_{\text{tot}}}{1+x}, \quad (12a)$$

$$g_{m2} = \Gamma_2 \times I_2 = \Gamma_2 \times \frac{xI_{\text{tot}}}{1+x}, \quad (12b)$$

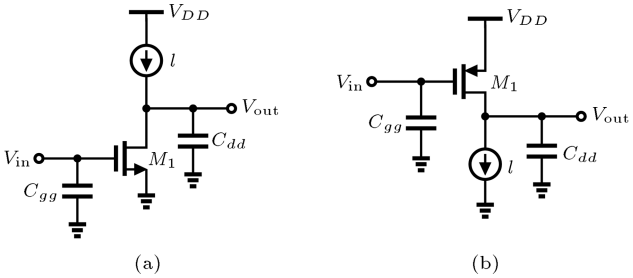

Figure 2. Circuit model of a g_m stage: (a) NMOS g_m stage; and (b) PMOS g_m stage.

where $I_{\rm tot}$ is the total dc current and subscripts "1" and "2" stand for the corresponding stages of the op amp. Also, we can write C_1 and C_2 as:

$$C_1 = C_{dd1} + C_{gg2} = \frac{\xi_1 \cdot g_{m1}}{\omega_{T1}} + \frac{g_{m2}}{\omega_{T2}}, \tag{13a}$$

$$C_2 = C_{dd2} + C_L \simeq C_L. \tag{13b}$$

Substituting Eqs. (12) and (13) into Eq. (11), and solving for $I_{\rm tot}$, the total required dc current can be calculated. Assuming GBW $\ll \omega_{T1}$ and ω_{T2}, $I_{\rm tot}$ can be approximated as:

$$I_{\rm tot} \simeq \frac{(1+x)\left(\xi_1\Gamma_1\omega_{T2} + x\Gamma_2\omega_{T1}\right)}{x \cdot \Gamma_1\omega_{T1} \cdot \Gamma_2\omega_{T2}} \times \tan({\rm PM}) \times {\rm GBW}^2 \times C_L. \tag{14}$$

4. Minimum power design

For the transistors in a given technology, both Γ and ω_T are functions of gate-source bias voltage, V_{GS} [20]. Therefore, the required $I_{\rm tot}$ in Eq. (14) will be a function of three design variables; V_{GS1}, V_{GS2}, and x. These design variables can then be optimized to result in the minimum possible $I_{\rm tot}$ (or power consumption). In the following, we will first investigate the optimum design, according to the long-channel device equations. Then, the analysis will be extended to the more realistic case of short-channel devices.

4.1. Long-channel analysis

For long-channel transistors, we have [19]:

$$\Gamma(V_{GS}) = 2/(V_{GS} - V_t), \tag{15a}$$

$$\omega_T(V_{GS}) = 3\mu(V_{GS} - V_t)/2L^2, \tag{15b}$$

where V_t is the threshold voltage, μ is the carrier mobility, and L is the channel length. Using Eq. (15) and defining $V_{OD} \triangleq V_{GS} - V_t$, the $I_{\rm tot}$ given in Eq. (14) becomes:

$$I_{\rm tot} \simeq \frac{(1+x)L^2}{3x}\left(\frac{\xi_1}{\mu_1}\frac{V_{OD2}}{V_{OD1}} + \frac{x}{\mu_2}\frac{V_{OD1}}{V_{OD2}}\right)\tan({\rm PM}) \times {\rm GBW}^2 \times C_L, \tag{16}$$

which depends on the ratio V_{OD2}/V_{OD1} rather than the values of V_{GS1} or V_{GS2}. This is because, according to Eq. (15), the product $\omega_T \times \Gamma$ is constant (for long-channel devices), which means there is no preferred value for V_{GS} to minimize Eq. (14). It can be shown, from Eq. (16), that $I_{\rm tot}$ is minimized at:

$$\left(\frac{V_{OD2}}{V_{OD1}}\right)_{opt} = \sqrt{\frac{1}{\zeta_1}\frac{\mu_1}{\mu_2}}, \tag{17a}$$

$$x_{opt} = 1. \tag{17b}$$

Interestingly, Eq. (17b) suggests that $I_{\rm tot}$ should be equally distributed among the two stages of the op amp, regardless of the technology and transistor type (i.e. NMOS or PMOS) used in each stage. This, in conjunction with Eq. (17a), maintains a proper balance between g_{m1} and g_{m2}, and the parasitic capacitance introduced by each of them at the inter-stage node.

The choice, $x_{opt} = 1$, is in contrast with the conventional design guides that put, $I_2 \gg I_1$. As an example, in Figure 3, the constant $I_{\rm tot}$ contours are plotted using Eq. (16), for the given technology parameters. The optimum design (given by Eq. (17)) is also indicated in Figure 3, along with a typical design from [14]. In comparison, the total power consumption is reduced to half by the optimum design. Note that the optimum design (i.e. $I_1 = I_2$ instead of $I_1 \ll I_2$) also results in a higher g_{m1}, which is desired, as it also improves the noise performance of the op amp.

4.2. Short-channel analysis

For the short-channel devices, Γ and ω_T are again functions of V_{GS} [20]. However, the dependency is much more complicated than that of the long-channel devices given in Eq. (15). Typical short-channel Γ and ω_T plots are shown in Figure 4. As can be seen, reducing V_{GS} improves Γ until it gradually reaches the upper limit of $1/\eta V_T$ at the sub-threshold region (V_T is the thermal voltage and η is the non-ideality factor). In contrast to Γ, ω_T increases with V_{GS} and reaches its maximum at the strong inversion region.

Figure 4(c) shows product $\Gamma \times \omega_T$ that is maximum at $V_{GS} = \widehat{V}$. It is, therefore, reasonable to assume that the optimum choices for V_{GS1} and V_{GS2} are close to their corresponding $\widehat{V}$. Note that $\partial(\Gamma \times \omega_T)/\partial V_{GS}$ is small near $\widehat{V}$, around which, product $\Gamma \times \omega_T$ is

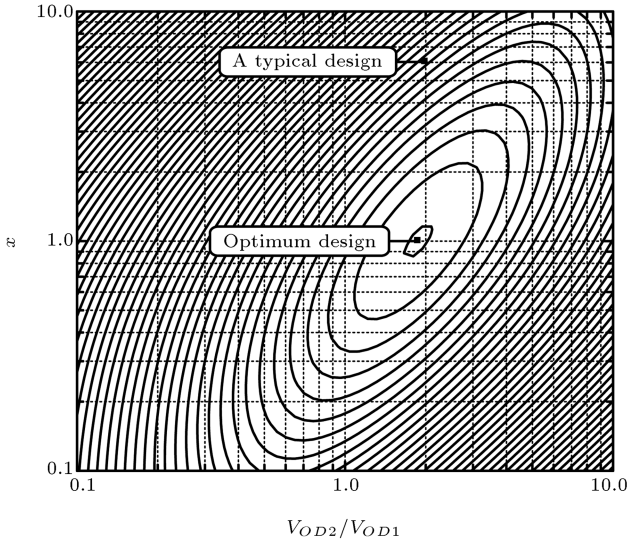

Figure 3. Constant $I_{\rm tot}$ contours plotted for $\sqrt{\mu_1/\zeta_1\mu_2} = 1.9$.

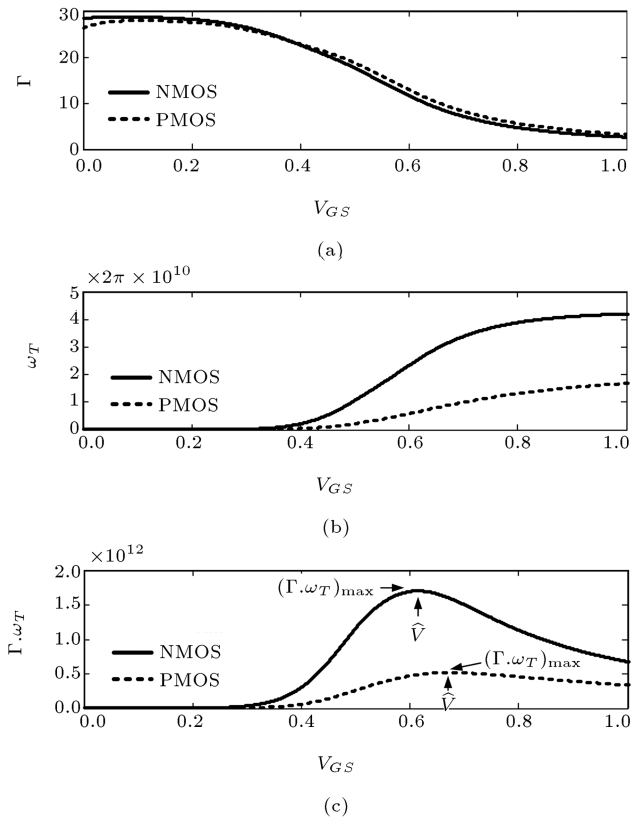

Figure 4. Simulated performance of 0.18-μm transistors biased at $V_{\rm DS} = V_{DD}/2 = 0.9$ V, employing an equally sized complementary transistor as load: (a) Γ; (b) ω_T; and (c) $\Gamma.\omega_T$.

approximately constant, i.e.:

$$\Gamma_1 \times \omega_{T1} \simeq (\Gamma \cdot \omega_T)_{1,\max}, \tag{18a}$$

$$\Gamma_2 \times \omega_{T2} \simeq (\Gamma \cdot \omega_T)_{2,\max}. \tag{18b}$$

By applying Eq. (18) to Eq. (14), $I_{\rm tot}$ can be approximated (near $V_{GS1} \approx \widehat{V_1}$ and $V_{GS2} \approx \widehat{V_2}$) as:

$$I_{\rm tot} \simeq \frac{1+x}{x}\left(\frac{\xi_1}{(\Gamma \cdot \omega_T)_{2,\max}}\frac{\omega_{T2}}{\omega_{T1}} + \frac{x}{(\Gamma \cdot \omega_T)_{1,\max}}\frac{\omega_{T1}}{\omega_{T2}}\right) \times \tan({\rm PM}) \times {\rm GBW}^2 \times C_L. \tag{19}$$

It can be shown that Eq. (19) is minimized by choosing:

$$\left(\frac{\omega_{T2}}{\omega_{T1}}\right)_{\rm opt} = \frac{1}{\zeta_1}\left(\frac{\Gamma_2}{\Gamma_1}\right)_{\rm opt} = \sqrt{\frac{1}{\zeta_1} \times \frac{(\Gamma \cdot \omega_T)_{2,\max}}{(\Gamma \cdot \omega_T)_{1,\max}}}, \tag{20a}$$

$$x_{\rm opt} = 1. \tag{20b}$$

Again, this indicates that $I_{\rm tot}$ should be equally distributed among the two stages of the op amp, similar to that obtained for long-channel transistors. Finally, substituting Eq. (20) into Eq. (19) results in:

$$I_{\rm tot,min} \simeq \frac{4\sqrt{\xi_1}\tan({\rm PM}) \times {\rm GBW}^2 \times C_L}{\sqrt{(\Gamma \cdot \omega_T)_{1,\max} \times (\Gamma \cdot \omega_T)_{2,\max}}}, \tag{21}$$

which gives the minimum required dc current for a given C_L, GBW, phase margin, and technology parameters. According to Eq. (21), the required $I_{\rm tot,min}$ is proportional to GBW^2, rather than GBW, as suggested by the widely used figure of merit for op amps (FOM $\propto$ GBW$\times C_L/I_{\rm tot}$). Eq. (21) also clearly states the impact of technology on the performance of the op amp and its required power consumption. For example, $(\Gamma \cdot \omega_T)_{\max}$ in 90-nm technology is about four times that in 0.18-μm technology node [20]. According to Eq. (21), this suggests that power consumption could be reduced by the same factor, when porting an op amp design from 0.18-μm to 90-nm technology.

5. Design example

Let us design the op amp shown in Figure 5, for the given specifications of C_L=10 pF, GBW=400 MHz, and tan(PM)=2. For the sake of simplicity, the width of M_{L1} is chosen to be the same as M_1, which, according to simulations, results in ξ_1=1.65. Using Eq. (21) and the technology parameters extracted from Figure 4, the required total dc bias can be calculated as $I_{\rm tot,min}$=742 μA. (Note that the op amp is differential and the actual dc bias will be twice.) Using Eq. (20), the optimal values for the design variables are also summarized in Table 1. For comparison, the exact optimum design obtained based on numeric minimization of Eq. (14) is also given in Table 1. As can be seen,

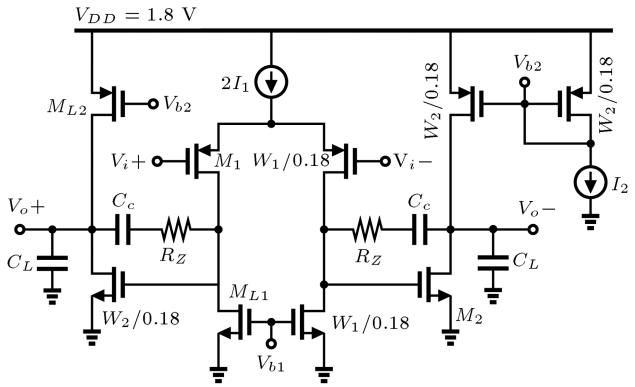

Figure 5. Op amp used in simulations.

Table 1. Design variables for the design example in Section 5.

	Approx. solution	Exact solution
$x_{\rm opt}$	1	1.38
$V_{GS1,\rm opt}$	0.80 V	0.76 V
$V_{GS2,\rm opt}$	0.58 V	0.61 V
$I_{\rm tot,min}$	742 μA	791 μA

Table 2. Comparing theory and simulation results.

	Theoretical	Simulation
I_1	332 μA	332 μA
I_2	459 μA	459 μA
W_1	19 μm	19 μm
W_2	24 μm	24 μm
z	-88.6 MHz	-90.2 MHz
p_2	-88.6 MHz	-90.9 MHz
p_3	-800 MHz	-794 MHz
GBW	400 MHz	386 MHz
PM	63.4°	65.3°

the solutions are slightly different. The main reason is the approximation made by Eq. (18), where $\Gamma \times \omega_T$ is approximated by the corresponding maximum around $\widehat{V}$. This also explains why the exact total current is higher than that given by the approximate solution. Nevertheless, the approximate $I_{\text{tot,min}}$ solution is only 6% off.

Given the exact solution (i.e. x=1.38 and I_{tot}=791 μA), both I_1 and I_2 are easily calculated, as given in Table 2. The width of the transistors (W_1 and W_2 in Figure 5) are also easily obtained, as we already know both V_{GS} and I_D for the transistors. For this purpose, at constant bias current, the transistor widths are swept in DC analysis, until the intended V_{GS} values are obtained. Using Eq. (12), the values of g_{m1} and g_{m2} are evaluated to calculate the required C_C and R_Z values from Eqs. (6) and (2), respectively. Both theoretical and Spectre simulation results are summarized in Table 2. As can be seen, the analysis and simulations are in close agreement.

In order to compare the optimumn design with the conventional design guides, the op amp in Figure 5 has also been designed with a typical choice of $I_2 = 5 \times I_1$. Using the same design specifications and V_{GS} values, this resulted in 46% increase in the total power consumption, compared to the optimum design.

6. Additional design constraints

Eq. (21) gives the minimum theoretical bound for I_{tot} that is required to achieve the given specifications. However, there may be some additional design constraints that increase the total power consumption. Two important instances of such constraints are briefly studied in this section.

6.1. Physical limitation

Keeping V_{GS1} and V_{GS2} at their optimum values around $\widehat{V}$, the bias current can be reduced (e.g. for lower GBW's) by shrinking the transistor width. Once the width of the transistors reaches its minimum (ruled either by the foundry or by the designer), any further reduction in power consumption can be only achieved by reducing V_{GS}, which finally pushes the transistors into the sub-threshold region. As a result, Eq. (21) becomes invalid and $I_{\text{tot,min}}$ should be recalculated.

For minimum width transistors, the total interstage capacitance will also be limited to its minimum value ($C_{1,\text{min}}$). Assuming that the transistors have been pushed into the sub-threshold region (i.e. $\Gamma_1 = 1/\eta_1 V_T$ and $\Gamma_2 = 1/\eta_2 V_T$), the required total current can be calculated from Eq. (11) as:

$$I_{\text{tot}} \simeq \frac{1+x}{\sqrt{x}} \times \sqrt{\tan(\text{PM})\eta_1\eta_2 C_{1,\text{min}} C_L} \times V_T \times \text{GBW}, \tag{22}$$

which is, again, minimized at $x_{opt} = 1$, resulting in:

$$I_{\text{tot,min}} \simeq 2\sqrt{\tan(\text{PM})\,\eta_1\eta_2 C_{1,\text{min}} C_L} \times V_T \times \text{GBW}. \tag{23}$$

Note that this $I_{\text{tot,min}}$ is proportional to GBW. Equating (23) and (21), the GBW below which the width limitation occurs can be calculated. For example, given the technology parameters shown in Figure 4 and for ξ_1=1, PM=64°, and $C_{1,\text{min}}/C_L$=10 fF/10 pF, the width limitation occurs at GBW<60 MHz. For higher desired GBWs, Eq. (21) will be valid.

6.2. Pole/zero doublet limitation

Let us investigate the location of the pole/zero doublet, $\omega_{\text{dblt}} = g_{m2}/C_L$. Using Eq. (12b), ω_{dblt} can be expressed in terms of I_{tot} as:

$$\omega_{\text{dblt}} = \frac{\Gamma_2}{C_2}\frac{x}{1+x} \times I_{\text{tot}}. \tag{24}$$

Thus, similar to I_{tot} in Eq. (21), ω_{dblt} would be also proportional to GBW^2. This means that, for small GBW's (or equivalently for small unity-gain bandwidths ω_u's), the ratio $\omega_{\text{dblt}}/\omega_u$ is also reduced. In high precision applications and due to a possible doublet mismatch, a small ratio, $\alpha = \omega_{\text{dblt}}/\omega_u$, may degrade the settling time [21,22]. Therefore, depending on the application, one may limit the ratio to α_{min}. As a result, a lower bound for I_{tot} can be found by rewriting Eq. (24) as:

$$I_{\text{tot}} \simeq \frac{1+x}{x} \cdot \frac{C_L}{\Gamma_2} \times \alpha_{\text{min}} \times \text{GBW}. \tag{25}$$

For the best cases of large x (i.e. $I_2 \gg I_1$) and maximum Γ_2 (i.e. sub-threshold biasing of the second stage), the lower bound given in Eq. (25) becomes:

$$I_{\text{tot,min}} \simeq C_L \eta_2 V_T \alpha_{\text{min}} \times \text{GBW}. \tag{26}$$

7. Conclusion

Two-stage Miller-compensated op amps were studied in this paper to gain a clear understanding about the required dc power and its relation to the bandwidth and other electrical specifications. Simple design guides were also provided in order to minimize the power consumption of the op amps. For instance, it was shown that unlike the conventional design guides, it is best to assign equal power to each stage of the op amp. Performed for both long and short-channel devices, the analysis has clearly revealed the impact of the technology on the performance of the op amps. Using two examples, it was also shown how additional design constraints can be conveniently considered in the design procedure.

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Appendix A

Here, we will extend the results obtained in the previous sections to the other op amp configurations,

as shown in Figure A.1. For all configurations, the op amp's internal topology is the same as that shown in Figure 1.

Let us first examine the closed-loop amplifier shown in Figure 6(a). Neglecting the feed-forward current through the feedback resistor (i.e. assuming $g_{m2} \gg g$), the loop gain can be approximated by:

$$T(s) \simeq -\frac{(1+A_V)^{-1}}{(1+sC_{in}/g(1+A_V))} \times \frac{g_{m1}g_{m2}\left[1+sC_C(R_Z-1/g_{m2})\right]}{s[s^2R_ZC_CC_1C_2+s(C_1C_2+C_1C_C+C_2C_C)+g_{m2}C_C]}, \quad \text{(A.1)}$$

which has the same poles and zeros as Eq. (1), except for an additional input pole at $p_4 = g(1+A_V)/C_{in}$. Assuming $p_4 \gg$ GBW (which holds at reasonable resistor values) and also satisfying the pole/zero cancellation condition in Eq. (2), the loop gain will be simplified to:

$$T(s) = f \times \frac{-\text{GBW}}{s\,(1+s/p_3)}, \quad \text{(A.2)}$$

where $f = 1/(1+A_V)$. Indeed, Eq. (A.2) is an extension of Eq. (4) for the closed loop circuit, shown in Figure A.1(b), with an arbitrary feedback coefficient f (that is not necessarily unity). For this generalized case, we can revise Eq. (7) as PM $\simeq \tan^{-1}[p_3/(f \times \text{GBW})]$. The only modification that this will cause in our analysis is that all the terms tan(PM) in Eq. (11) and the following equations would be simply replaced by $f \times$ tan(PM). Of course, this has no effect on the optimum choices for x, V_{GS1}, and V_{GS2}.

Two-stage op amps are also widely used in active-RC filters to realize closed-loop integrators, as shown in Figure A.1(c). As shown by the authors in [23], under typical assumptions of $C \gg C_{in}$ and GBW $\gg (g_{in}+g)/C$, the high frequency loop gain of the integrator is identical to that of the op amp in the unity-gain feedback configuration. As a result, the analysis performed in the previous sections is also applicable to the op amps used in active-RC filters.

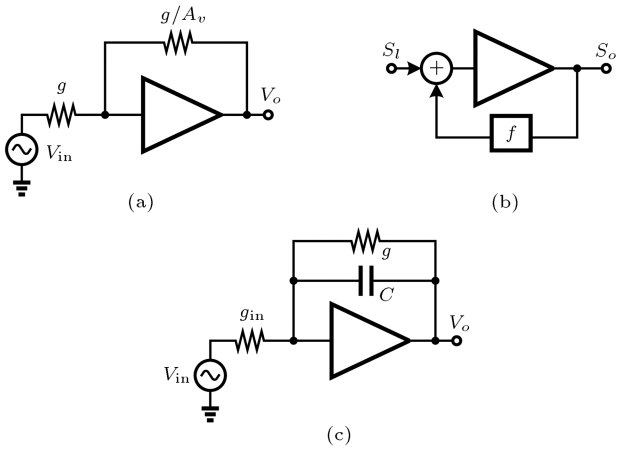

Figure A.1. Widely used op amp configurations: (a) Closed-loop amplifier; (b) arbitrary feedback coefficient; and (c) active-RC integrator.

Biographies

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