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A tunable high-Q active inductor with a feed forward noise reduction path

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Abstract. The analysis and design of a tunable low noise active inductor is presented. The noise performance of the proposed gyrator-based active inductor is improved without either degrading its quality factor or consuming more power using a linear Feed Forward Path (FFP). The proposed low noise active inductor has been designed and fabricated using standard 0.18-μm CMOS technology. The measurements show a 3 fold improvement in the input noise current compared to that of conventional active inductors. The active inductor was tuned and measured at the resonance frequency of 2.5 GHz, which could be extended as high as 5.5 GHz, with a quality factor of 30. The circuit draws 4.8 mA from a 1.8 V supply.

1. Introduction

An inductor is one of the components that significantly facilitates the design of radio frequency integrated circuits. Inductors are widely used in the input matching networks of low noise amplifiers. They are an indispensable part of low phase noise oscillators, frequency selective and tuned radio frequency circuits, and many other applications, which make inductors a ubiquitous part of radio frequency circuits.

The characteristics of on-chip passive inductors in today's CMOS technology are far from those of ideal inductors. The most important barriers against the effective use of inductors are their large size and low quality factor. The lack of tuning capability is another drawback of the passive on-chip inductors.

Active inductors (AIs), on the other hand, do not suffer from these handicaps. Small dimensions, high quality factor and tunability are among the advantages of active inductors. Despite all the advantages, the inferior noise performance of active inductors, in addition to their nonlinearity, high current consumption, and dependency on temperature and process variations, is the most important barrier to their practical use in many applications.

Reported work in this area is mostly concerned with improvements in quality factor and resonant frequency, while the noise and linearity characteristics of the AI have not yet received much attention.

In this paper a novel, high-Q, tunable active inductor with low equivalent noise current is proposed. The linearity of the proposed AI is also improved compared to the linearity of conventional circuits for AI.

This paper is organized as follows. Section 2 presents a review the state of the art research. The proposed noise reduction technique is described in section 3. The measurement results are given in section 4 and the conclusions are drawn in section 5.

2. Background

Figure 1(a) shows one of the most common topologies of active inductors that uses a gyrator comprised of two

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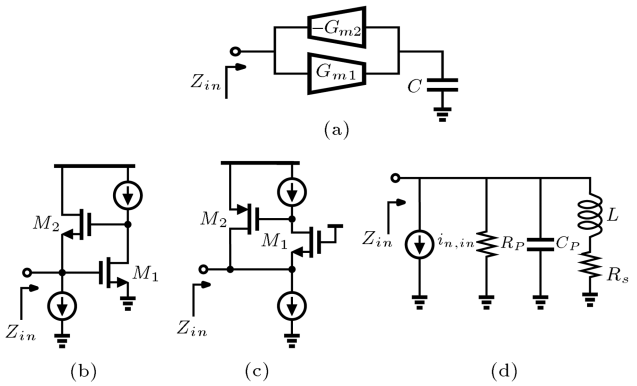

Figure 1. Active inductor. (a): General structure; (b,c): Two mostly used circuits; and (d): Equivalent RLC model with the equivalent noise current source.

back to back transconductances, G_{m1} and G_{m2}, and a capacitor, C [1]. The input impedance of the gyrator-based circuit in Figure 1(a) is inductive, and can be calculated as:

$$Z_{in} = \frac{sC}{G_{m1}G_{m2}}. \tag{1}$$

Two mostly used circuits for gyrator based active inductors are shown in Figure 1(b) and (c), in which transistors M_1 and M_2 and the gate-source capacitance of M_2 (i.e. C_{gs2}) are used to implement G_{m1}, G_{m2}, and C, respectively [2,3]. Although the self-resonant frequency (f_r) of these active inductors is high, due to their simple structure, the input/output resistances of M_1 and M_2 degrade the quality factor (Q).

Figure 1(d) shows the equivalent input impedance and the input-referred noise current of the AIs shown in Figure 1(b) and (c). For the sake of simplicity, let us neglect the transistors' gate-drain and junction capacitors (i.e. C_{gd}, C_{sb} and C_{db}). Assuming ideal current sources and using the hybrid-π small signal model, the components of the equivalent RLC model of Figure 1(d) can be calculated as:

$$L = \frac{C_{gs2}}{g_{m1}g_{m2}}, \tag{2a}$$

$$C_p = C_{gs1}, \tag{2b}$$

$$R_p = \frac{1}{g_{m1}} \| r_{o2} \simeq \frac{1}{g_{m1}}, \tag{2c}$$

$$R_s = \frac{1}{g_{m1}g_{m2}r_{o1}}, \tag{2d}$$

where, g_m, r_o and C_{gs} are the transistors' transconductance, output resistance and gate-source capacitor, respectively. Neglecting the small series resistance (R_s), the self-resonant frequency, f_r, and the quality factor, Q, can be derived as:

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC}} = \frac{1}{2\pi}\sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}}$$

$$= \sqrt{f_{T1}f_{T2}}, \tag{3a}$$

$$Q = \frac{R_p}{L\omega_r} = \frac{1}{g_{m1}L\omega_r}, \tag{3b}$$

where, f_T is the transit frequency of transistors.

Eqs. (3a) and (3b) reveal that the self-resonant frequency can be potentially high, while the quality factor is often low, due to the parallel resistance, R_p, given in (2c).

Neglecting the flicker noise, the input-referred noise current, $i_{n,in}$, can be derived as:

$$\overline{i_{n,in}^2} = 4kT\gamma \left[\underbrace{\left(\frac{1}{g_{m1}(L\omega)^2} + g_{m1} \right)}_{\text{due to } M_1} + \underbrace{g_{m2}}_{\text{due } M_2} \right], \tag{4}$$

where the channel thermal noise is assumed to be $\overline{i_d^2} = 4kT\gamma g_m$, in which γ is the channel excess noise factor. Using (3b), the input-referred noise current can be rewritten as:

$$\overline{i_{n,in}^2} = 4kT\gamma \left[\underbrace{\left(\frac{Q + 1/Q}{L\omega} \right)}_{\text{due to } M_1} + \underbrace{g_{m2}}_{\text{due to } M_2} \right]. \tag{5}$$

The noise current of a passive inductor with the same quality factor can be derived as:

$$\overline{i_{n,\text{in,passive}}^2} = \frac{4kT}{QL\omega}. \tag{6}$$

As can be seen from Eq. (5), the input noise current of the AIs is composed of two components, one of which, i.e. noise due to M_1, is higher by a factor of Q^2 compared to the noise current of the passive inductor with the same quality factor. Therefore, enhancing Q by lowering g_{m1} increases the input noise current. Moreover, according to Eq. (2a), smaller g_{m1} demands higher g_{m2} (for the same L), which will result in further degradation of the noise performance of AIs.

A number of techniques have been employed to enhance the quality factor of the active inductor. The quality factor can be improved by using a negative resistance in parallel with the AI [2-4]. This negative resistance, however, degrades the noise performance and increases the power consumption of the active inductor. The quality factor can also be improved by utilizing a series resistance (R_f) at the gate of M_2 [5,6] in Figure 1(b) and (c). The nonlinear dependency

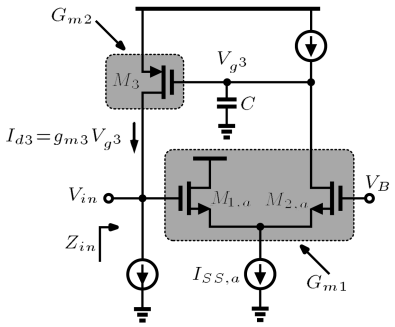

Figure 2. Using the differential stage to improve the quality factor independent of input noise current.

of the inductance and Q on R_f, and increasing input noise current are the main drawbacks of this technique. A feedback transistor, as suggested in [7], can also be employed to enhance Q at the cost of potential instability at higher frequencies.

The quality factor is often improved by replacing the common gate stage with a differential stage [8,9], as depicted in Figure 2. The equivalent circuit of AI shown in Figure 2 can again be taken as that shown in Figure 1(d) with:

$$L = \frac{2C}{g_{m1,a}g_{m3}}, \tag{7a}$$

$$C_p \simeq \frac{1}{2}C_{gs1,a} + C_{gd1,a} + C_{gd3} + C_{db3}, \tag{7b}$$

$$R_p = r_{o3}, \tag{7c}$$

$$R_s \simeq \frac{2}{g_{m1,a}g_{m3}r_{o2,a}}, \tag{7d}$$

where, C is the total capacitance at the gate of M_3. As can be seen from Eq. (7c), compared to the AI shown in Figure 1(c), higher parallel equivalent resistance (R_p) results in improving the quality factor. At the resonance frequency, the quality factor of AI shown in Figure 2 can be derived as:

$$Q = \frac{\left(R_p \| \frac{(L\omega_r)^2}{R_s}\right)}{L\omega_r} = \frac{\left(r_{o3} \| \frac{C \times r_{o2,a}}{C_p}\right)}{L\omega_r}. \tag{8}$$

The equivalent input referred noise current can also be calculated as:

$$\overline{i_{n,in}^2} = 4kT\gamma \left[\underbrace{\left(\frac{2}{g_{m1,a}(L\omega)^2}\right)}_{\text{due to Diff. Stage}} + \underbrace{g_{m3}}_{\text{due M3}} \right], \tag{9}$$

which reveals that the input noise current can be minimized for a given L and a constant Q, by properly choosing the transconductances, $g_{m1,a}$ and g_{m3}.

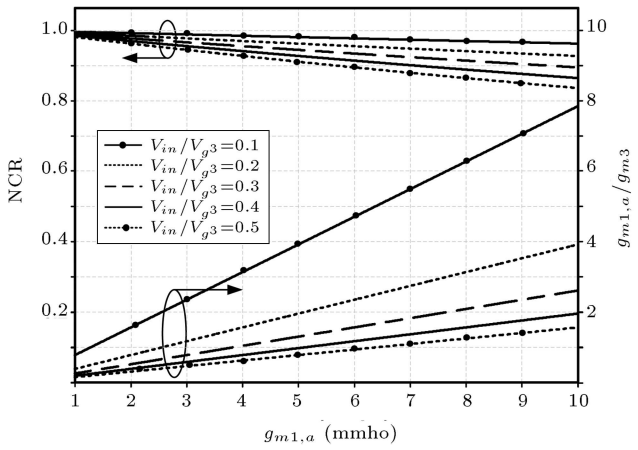

Figure 3. The ratio of $g_{m1,a}$ to g_{m3} and the ratio of the noise current due to the differential pair to the overall noise current (NCR).

As can be seen from Eq. (9), the noise due to transistor M_3 can be minimized by a smaller g_{m3}. To sustain the same drain current for M_3 (i.e. the same $i_{d3} = v_{in}/L\omega$), this requires a higher voltage amplitude at the gate of M_3 (i.e. v_{g3}). Therefore, the reduction of g_{m3} (to enhance the noise performance) is limited by the maximum voltage swing that can be tolerated at the gate of M_3 in Figure 2.

The reduction of $i_{n,in}$ can also be achieved by choosing a larger $g_{m1,a}$. The transconductance, $g_{m1,a}$, can be increased by increasing either aspect ratio (W/L) or the bias current of the differential pair, $M_{1,a}$ and $M_{2,a}$. Wider transistors degrade the linearity performance of the differential pair due to the smaller overdrive voltage for the transistors, $M_{1,a}$ and $M_{2,a}$. The bias current is also limited by power consumption. That is, power and linearity impose an upper limit for reducing the noise due to the differential stage.

In Figure 3, the ratio of $g_{m1,a}$ to g_{m3} and the ratio of the noise current, due to the differential pair transistors, to the overall noise current (NCR) are plotted as a function of $g_{m1,a}$ for different values of v_{in}/v_{g3}. As can be seen in Figure 3, although the differential pair transistors consume more power than M_3 (due to the higher g_m), the noise current of the active inductor is mainly determined by the differential pair. Therefore, reduction of the noise due to $M_{1,a}$ and $M_{2,a}$ can effectively improve the overall noise performance of the active inductor.

3. Proposed active inductor

3.1. Noise performance

In this section, we propose a method for reducing the overall noise current of the active inductor, without increasing power consumption. As shown in Figure 4,

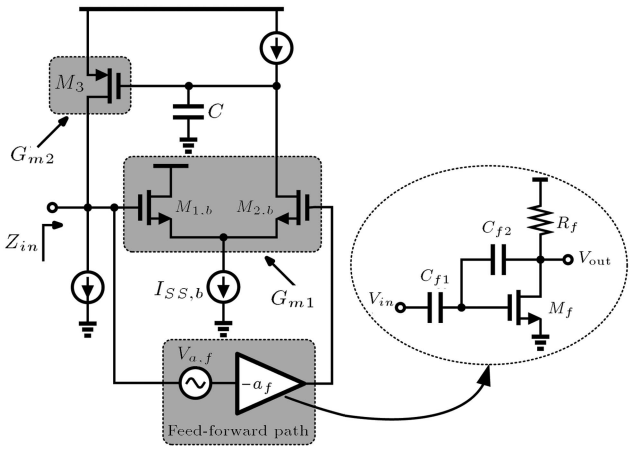

Figure 4. Using the FFP to improve the noise performance of the active inductor.

we add a feed forward path (FFP) from the input to the gate of $M_{2,b}$. The equivalent inductance of the circuit shown in Figure 4 can be derived as:

$$L = \frac{2C}{(a_f + 1)g_{m1,b}g_{m3}}, \tag{10}$$

where, a_f is the gain of the feed forward path.

According to Eqs. (7a) and (10), for a given inductance (L), the ratio of the transconductance of the modified differential pair shown in Figure 4, ($g_{m1,b}$), to that of the basic differential pair shown in Figure 2, ($g_{m1,a}$), can be written as:

$$\frac{g_{m1,b}}{g_{m1,a}} = \frac{1}{a_f + 1}. \tag{11}$$

Therefore, for a given overdrive voltage, the bias current (I_{ss}) and the aspect ratio (W/L) of transistors in the differential pair with FFP can be reduced by ($a_f + 1$), i.e.:

$$\frac{I_{ss,b}}{I_{ss,a}} = \frac{(W/L)_{1,b}}{(W/L)_{1,a}} = \frac{1}{a_f + 1}. \tag{12}$$

The current reduction in the differential pair transistors compensates for the extra power consumption, due to the amplifier of the FFP, such that the overall power consumption of the active inductor remains unchanged.

The input referred noise current of the active inductor shown in Figure 4 can be calculated as:

$$\overline{i_{n,in}^2} = \underbrace{\frac{8kT\gamma}{g_{m1,b}(a_f + 1)^2(L\omega)^2}}_{\text{Differential Stage}} + \underbrace{\frac{\overline{v_{n,f}^2} \times a_f^2}{(a_f + 1)^2(L\omega)^2}}_{\text{FFP}} + \underbrace{4kT\gamma g_{m3}}_{\text{M}_3}, \tag{13}$$

where, $v_{n,f}$ is the input referred noise voltage of the FFP amplifier.

According to Eqs. (11) and (13), the differential pair noise reduces with the FFP gain (a_f), while the noise due to the transistor M_3 remains unchanged. The noise due to FFP, however, grows with a_f and can degrade the overall noise performance of the active inductor; that is, for a low noise operation, $v_{n,f}$ is to be minimized as much as possible. Moreover, the FFP has an adverse effect on the linearity of the active inductor. This is because, according to Eq. (10), the equivalent inductance changes when a_f changes with the input amplitude due to the nonlinearity.

The FFP amplifier is realized by a common source amplifier, which is linearized by the use of feedback. The resistive feedback, however, degrades the noise performance and the quality factor of AI. To avoid these penalties, the capacitive feedback loop comprising C_1 and C_2, as shown in Figure 4, is used to improve the linearity performance of the FFP amplifier.Assuming $g_{mf}R_f \gg 1$, the input referred noise voltage of FFP can be calculated as:

$$\overline{v_{n,f}^2} \simeq \frac{4kT\gamma}{g_{mf}} \times \left(\frac{a_f + 1}{a_f}\right)^2, \tag{14}$$

where $a_f = C_1/C_2$ is the gain of the FFP.

Assuming the same total power consumed in the differential pair with FFP, shown in Figure 4, and without FFP, shown in Figure 2, the drain current of the transistor, M_f, can be derived as:

$$I_{df} = I_{ss,a} - I_{ss,b}, \tag{15}$$

which can be rewritten by using (12) as:

$$I_{df} = a_f I_{ss,b} = 2a_f I_{d1,b}. \tag{16}$$

Let us take m as the ratio of the aspect ratio (W/L) of M_f to that of $M_{1,b}$. Therefore, assuming the square law characteristic of CMOS transistors, the ratio of g_{mf} to $g_{m1,b}$ can be calculated as:

$$\frac{g_{mf}}{g_{m1,b}} = \sqrt{\frac{(W/L)_f}{(W/L)_{1,b}} \times \frac{I_{df}}{I_{d1,b}}} = \sqrt{2ma_f}. \tag{17}$$

From Eqs. (13), (14) and (17), the input noise current of the active inductor can be derived as:

$$\overline{i_{n,in}^2} = \frac{8kT\gamma}{g_{m1,b}(L\omega)^2}\left(\underbrace{\frac{1}{(a_f + 1)^2}}_{\text{Diff. Stage}} + \underbrace{\frac{1}{\sqrt{8ma_f}}}_{\text{FFP}}\right) + 4kT\gamma g_{m3}. \tag{18}$$

The ratio of the noise current component, due to the differential pair with FFP, to that without FFP (NR),

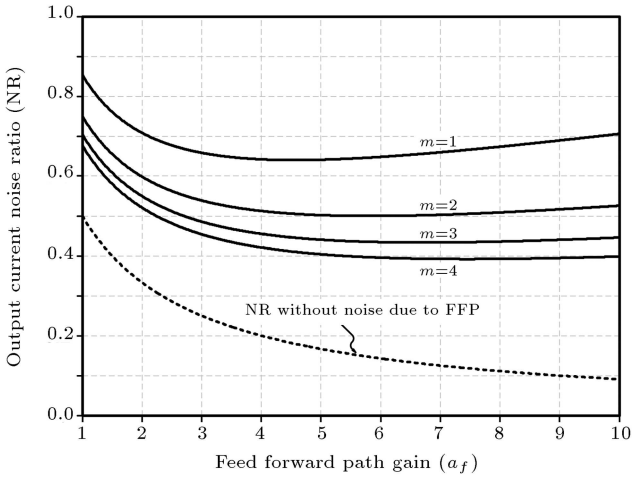

Figure 5. The input referred noise current ratio due to the differential stage with and without FFP.

can be derived as:

$$NR = \underbrace{\left(\frac{1}{a_f+1}\right)}_{\text{diff. Stage}} + \underbrace{\left(\frac{a_f+1}{\sqrt{8ma_f}}\right)}_{\text{FFP}}, \tag{19}$$

which indicates that increasing m (i.e. larger FFP transistor) results in lower NR.

Figure 5 shows NR as a function of the gain of the FFP (a_f) for different values of m. As can be seen in Figure 5, with the same power consumption, the noise due to the differential pair is reduced by about 40% for m=5. It also can be seen that increasing a_f does not always improve noise performance. This is because, when the total noise is dominated by the FFP, according to Eq. (19), increasing a_f degrades the overall noise performance. However, if the noise contribution of the FFP can be somehow cancelled, as reported by the authors in [10], then, NR would have been a decreasing function of a_f, as:

$$NR = \frac{1}{a_f+1}, \tag{20}$$

which is independent of m. This is shown by the dashed line in Figure 5. In this case, as depicted in Figure 5, the noise due to the differential pair is reduced by about 80%.

3.2. Active inductor circuit realization

A simplified circuit of the overall active inductor is shown in Figure 6. To enhance the effective transconductance, the current-reuse differential pair, comprised of transistors $M_{1a,b}$ and $M_{2a,b}$, is used to realize G_{m1}. The circuit linearity is improved by the emitter degeneration resistors, R_{E1} and R_{E2}. The integration capacitor (i.e. C at the drain of $M_{1a,b}$ and $M_{2a,b}$) is adjusted by four digital bits to tune the inductance of the active inductor.

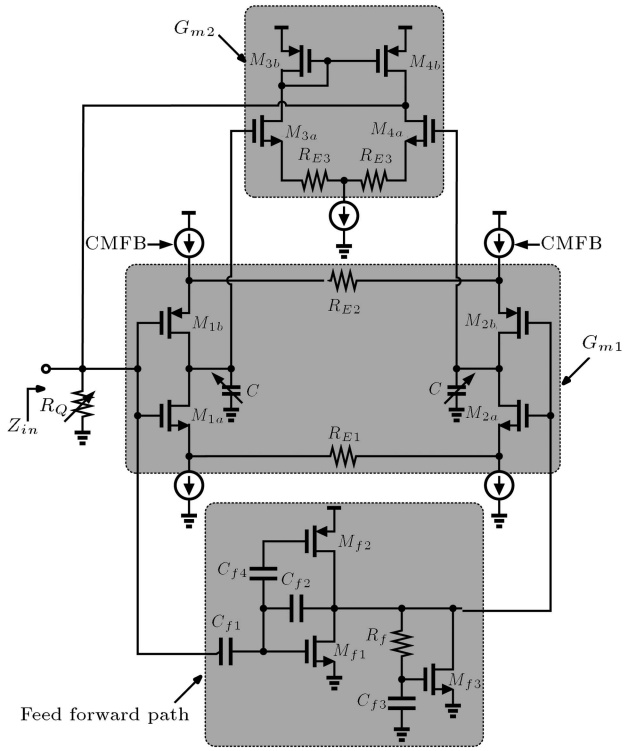

Figure 6. Simplified circuit of the overall active inductor.

The complementary common source transistors, $M_{f1,2}$, and capacitors, $C_{f1,2}$, constitute the FFP amplifier. The circuit, including transistor M_{f3}, resistor R_f and capacitor C_{f3}, is used to set the output dc voltage of the complementary transistors, $M_{f1,2}$.

The PMOS transistor M_3 in Figure 4 is replaced by the differential stage with a current mirror load consisting of transistors $M_{3a,b}$ and $M_{4a,b}$, as shown in Figure 6. This is to cancel the effect of common mode noise voltages generated by the tail current sources. Degeneration resistor R_{E3} is also used to improve the linearity of the differential pair.

Due to the infinite input and the large output resistance of the differential stages, the quality factor of the active inductor is potentially high. The parallel resistor, R_Q, at the input of the active inductor is to tune the quality factor of the active inductor. This resistor is adjusted by four digital bits.

4. Measurement results

The active inductor shown in Figure 6 was fabricated using standard 0.18-μm CMOS technology. The layout of the chip is shown in Figure 7. Die size is 0.2×0.4=0.08 mm^2. The overall active inductor draws 4.8 mA from a 1.8 V supply.

Tunability is one of the advantages of active inductors. According to Eq. (10), the inductance of the active inductor can be tuned by changing the equivalent transconductance of the differential stages

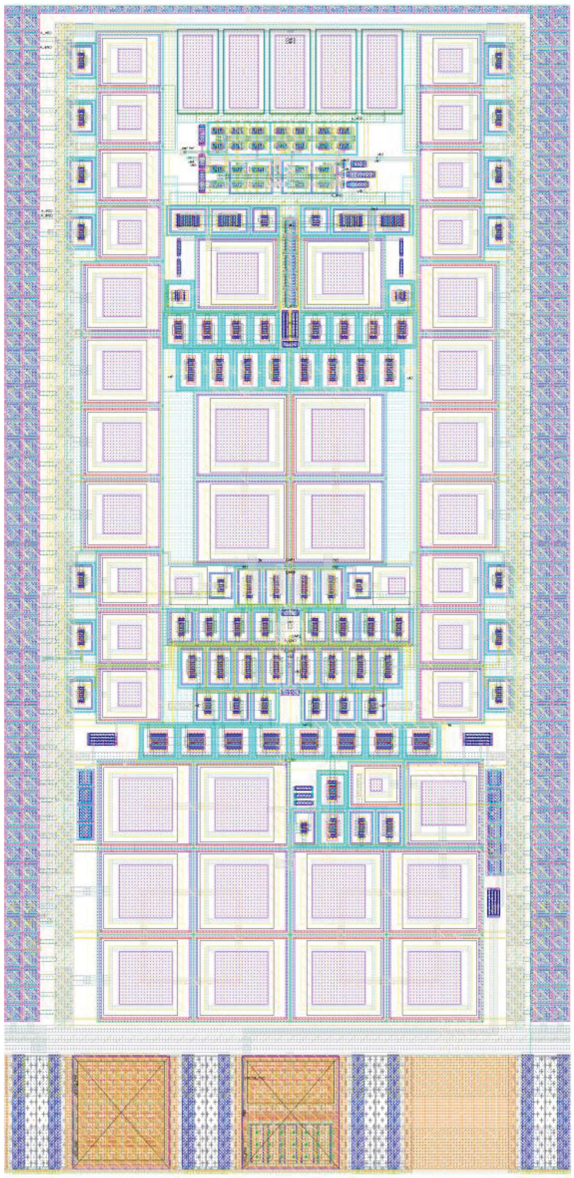

Figure 7. The layout of the fabricated active inductor.

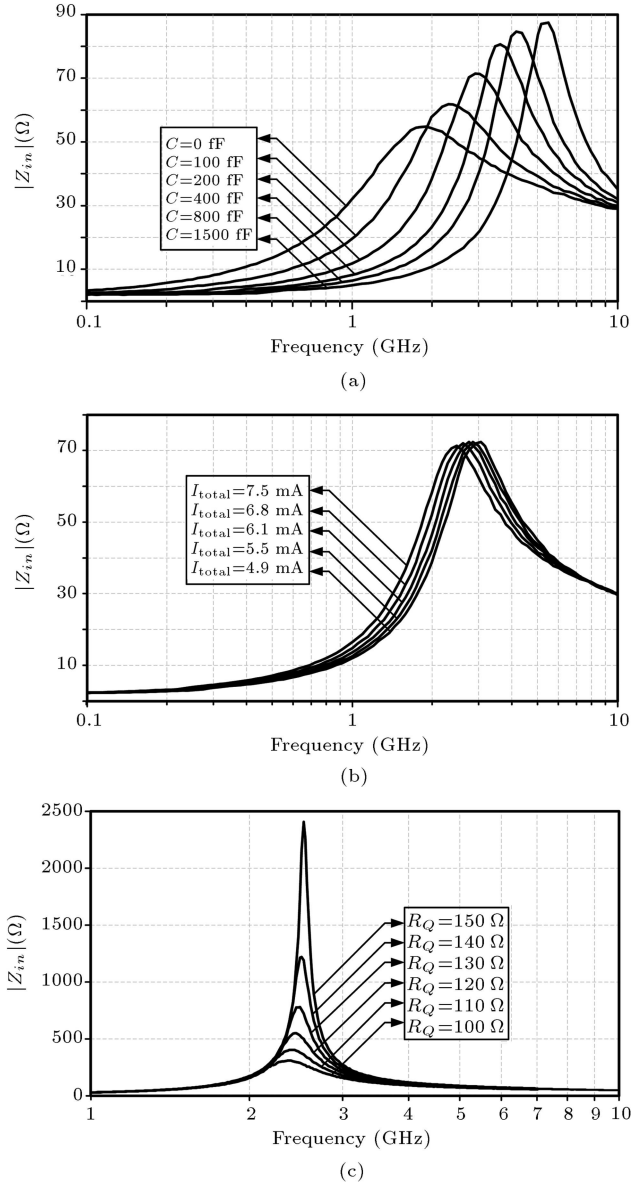

Figure 8. The measured impedance magnitude of the active inductor for different values of: (a): C; (b): the total current; and (c): R_Q values.

in a continuous manner or changing the integration capacitance in discrete steps. The measured impedance magnitude of the active inductor, for different values of C and the total current, are plotted in Figure 8(a) and (b), respectively.

Figure 8(a) demonstrates that the resonance frequency of the active inductor varies with the integration capacitor C, due to variation in the inductance. As shown in Figure 8(a), the resonance frequency of the active inductor changes from 1.8 GHz to 5.5 GHz by changing C from 0 to 1.5 pF. Furthermore, as depicted in Figure 8(b), the circuit inductance and, consequently, the resonance frequency can also be tuned by adjusting the tail currents of the differential pairs.

The magnitude of the input impedance of the circuit, for different values of R_Q, is plotted in Figure 8(c). As can be seen in Figure 8(c), the quality factor of the active inductor can widely be tuned by changing R_Q, while its resonance frequency remains unchanged.

Figure 9 shows the measured input referred noise current of the proposed active inductor for L=5.2 nH and Q=30. Using Eq. (5) and neglecting the noise due to M_2, the simulated noise current of a conventional AI with the same Q and L, as shown in Figure 1, is also plotted by the dashed line in Figure 9. As can be seen in Figure 9, compared to conventional AI, the input noise of the proposed AI is reduced by a factor of about 3.

The linearity of the active inductor tuned for L=5.2 nH and Q=30 was investigated by measuring the IIP3 at 2.5 GHz. A two-tone signal at 2.499 GHz

Table 1. Performance summary of the proposed LNA and its comparison with some previously published works.

Ref.	[2]	[11]	[12]	This work
Technology	0.18-μm CMOS	0.13-μm CMOS	0.35-μm CMOS	0.18-μm CMOS
Resonance freq. (GHz)	1.9 to 3.8	0.5 to 10.1	0.4 to 1.1	1.8 to 5.5
Quality factor	40	up to 3000	2 to 80	3 to 30
Noise power (dBm)	N/A	N/A	-57	-68.3
Noise current (pA/$\sqrt{\text{Hz}}$)	140 (@2.4 GHz)	100 (@5 GHz)	N/A	19 (@5 GHz)
IIP3 (dBm)	N/A	N/A	-15	-8.7
V_{DD} (V)	1.8	1.6	2.7	1.8
DC power (mW)	10.8	13.56	45.9	8.64
Die area (mm^2)	0.53	0.004	0.028	0.08

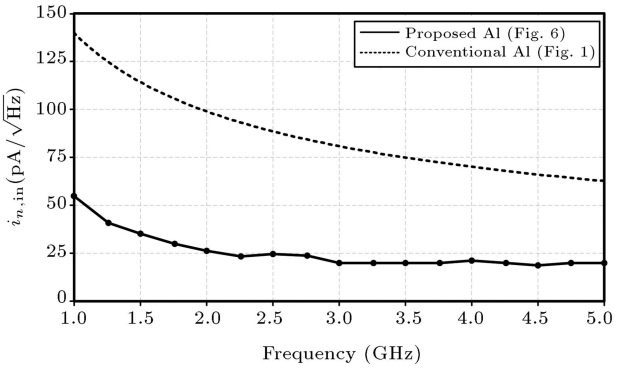

Figure 9. The input referred noise current of the proposed AI shown in Figure 6 and conventional AI shown in Figure 1.

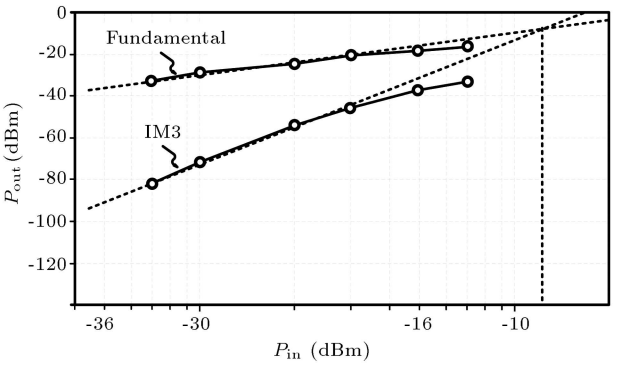

Figure 10. The measured IIP3 of the active inductor.

and 2.501 GHz was applied to the active inductor and an IIP3 of about -8.7 dBm was measured, as shown in Figure 10.

The measured performance of the active inductor is summarized in Table 1 and compared to that of previously published work. The proposed active inductor shows superior noise performance while consuming less power.

5. Conclusion

A tunable low-noise gyrator-based active inductor was presented. It was shown that, unlike conventional gyrator-based active inductors, a better noise performance of the active inductor can be achieved without either degrading its quality factor or consuming more power. The noise reduction is done by using a feed forward path which is linearized by the use of a capacitive feedback network. In addition to the tunable resonance frequency and quality factor, the measurements proved that the noise and linearity performance of the proposed active inductor is considerably better compared to that of previously reported work. The improved noise and linearity performance of the proposed active inductor makes it a suitable candidate for radio frequency circuits.

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