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Research Note

A new on-chip sensor design for NBTI using slew rate monitoring

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Abstract. In this paper, an on-chip NBTI sensor based on rise transition time difference measurement of inverter is proposed. This sensor supports both AC and DC stress mode with very short measurement time of 50 nsec. The new sensor, with direct correlation between V_{th} degradation and its output voltage change, has a resolution of 1 mV per 0.5 mV threshold voltage shift. Differential structure of the sensor eliminates the effect of common-mode environmental variation such as temperature. A 65 nm CMOS technology model is used for simulation of the sensor. The average power consumption of this sensor is 0.14 μW in stress mode and 4.54 μW during measurement mode. The implemented layout area is 98.9 μm^2.

1. Introduction

Negative Bias Temperature Instability (NBTI) is the major reliability concern that has limited the circuit lifetime in nano-scale CMOS technologies, and is characterized by a positive shift in the absolute value of pMOS threshold voltage when biased in strong inversion [1,2]. However, when the pMOS device turns off, it enters recovery phase in which the absolute value of V_{th} decreases. To cope with NBTI, a solution is adaptive design technique, using an on-chip sensor to monitor aging phenomena [1]. This technique helps to prolong circuit lifetime by adjusting the circuit parameter, such as Adaptive Body Biasing (ABB) or power supply adjustment, using the real time feedback of the on-chip sensor [3,4]. An approach in NBTI sensor is to apply stress for a given duration first. Then, the signal is removed, and a special parameter affected by NBTI during stress period is measured. In order to evaluate the effect of NBTI accurately, this measurement must be done quickly to avoid the effect of recovery. The recovery time is often less than 1 microsecond [5,6].

The fully digital on-chip sensors in [5,7] utilize ring oscillator frequency degradation to monitor the NBTI. However, these sensors suffer from the weak direct correlation between frequency and V_{th} shift, since the frequency change is also affected by nMOS drive strength degradation, due to Positive Bias Temperature Instability (PBTI) [8]. Also, this method averages out NBTI across all pMOS transistors of the ring oscillator, resulting in loss of statistical information [4]. The measurement time is 2 μsec in [5] and less than 1 μsec in [7].

In [2], the frequency shift of a Ring Oscillator is measured with a pMOS header under NBTI stress, which is biased in the subthreshold region during measurement for high sensitivity. This sensor is very sensitive to temperature variation, and needs extensive calibration. In [9] a Delay-Locked Loop (DLL) is used in which the increase of pMOS threshold is translated into a control voltage shift in DLL. In this sensor, the measurement time is too long, and hence the effect of

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recovery cannot be ignored. In [1,5,7], the monitoring output provides a digital word. In order to use this output to compensate NBTI effect, a DAC (digital to analogue converter) is needed that imposes area overhead [3]. In [8] NBTI sensor based on rise slew-rate monitoring is proposed, which requires a high-speed highly accurate comparator. In this paper, an on-chip NBTI sensor with new structure is proposed, which measures the output rise transition-time difference of a stressed inverter with an unstressed inverter.

2. NBTI and slew rate

V_{th} degradation under static stress can be obtained by [10]:

$$\Delta V_{th} = A.\left((1+\delta)t_{ox} + \sqrt{C(t-t_0)}\right)^{2n}, \quad (1)$$

where A is linearly proportional to the hole density, and has an exponential dependence on temperature and the electric field; t_{ox} is the gate oxide thickness, δ is a constant (5 mV), and n is the time exponent. In dynamic behaviour, the following long-term predictive model [10-12] for NBTI degradation is used in simulation:

$$\Delta V_{th} = \left(\frac{\sqrt{K_v^2 \alpha T_{clk}}}{1-\beta_t^{1/2n}}\right)^{2n}, \quad (2)$$

$$\beta_t = 1 - \frac{3\xi_1 t_e + \sqrt{\xi_2 C(1-\alpha)T_{clk}}}{2t_{ox} + \sqrt{Ct}}, \quad (3)$$

$$K_v = \left(\frac{qt_{ox}}{\epsilon_{ox}}\right)^3 K_1^2 C_{ox}(V_{gs} - V_{th})\sqrt{C}\exp\left(\frac{2E_{ox}}{E_{01}}\right), \quad (4)$$

where α and T_{clk} are duty cycle and period of signal, respectively. Remaining parameters and constants are expressed in [10-12].

3. NBTI sensor

This section presents a new on-chip NBTI sensor which consists of a reference inverter, a stressed inverter, and two slew monitoring blocks, as shown in Figure 1(a). Each slew monitoring block consists of a semi-inverter and an integrator. This sensor exploits the fact that the output rise slew-rate of an inverter is a strong function of its pMOS drive strength. Therefore, rise slew rate is an indicator of NBTI effect, while the effect of nMOS is decoupled.

Stress signal is applied to the input of stressed inverter during stress period (Figure 1(b)), while the input of reference inverter is connected to V_{dd}, which makes its pMOS free from device aging. In measurement period, both reference and stressed inverters have the test input signal in Figure 1(b).

In stress period, V_{th} of pMOS in stressed inverter is degraded depending on voltage level, duty cycle and the number of cycles of the applied stress signal.

In measurement period, both inverters conduct test signal with specific transition time (e.g. 20 ps in this work). Because of aging in pMOS of stressed inverter, output rise transition time of stressed inverter

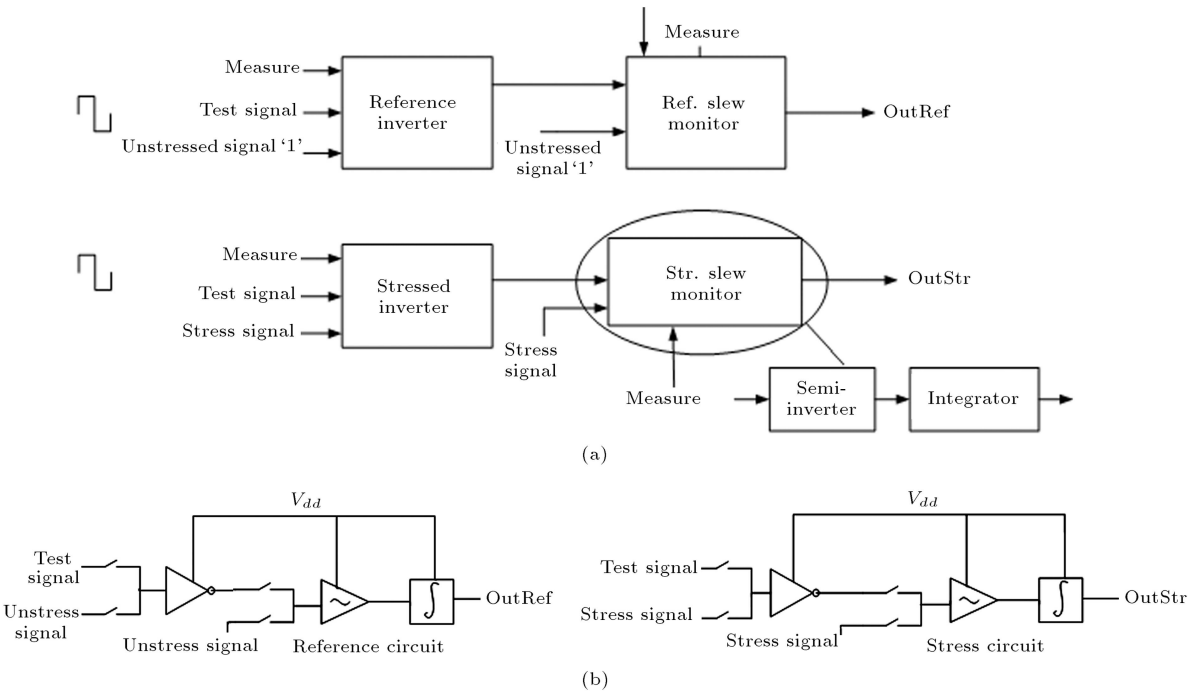

Figure 1. (a) The block diagram of new on-chip NBTI sensor. (b) Input signal control in stress and measurement periods with switch.

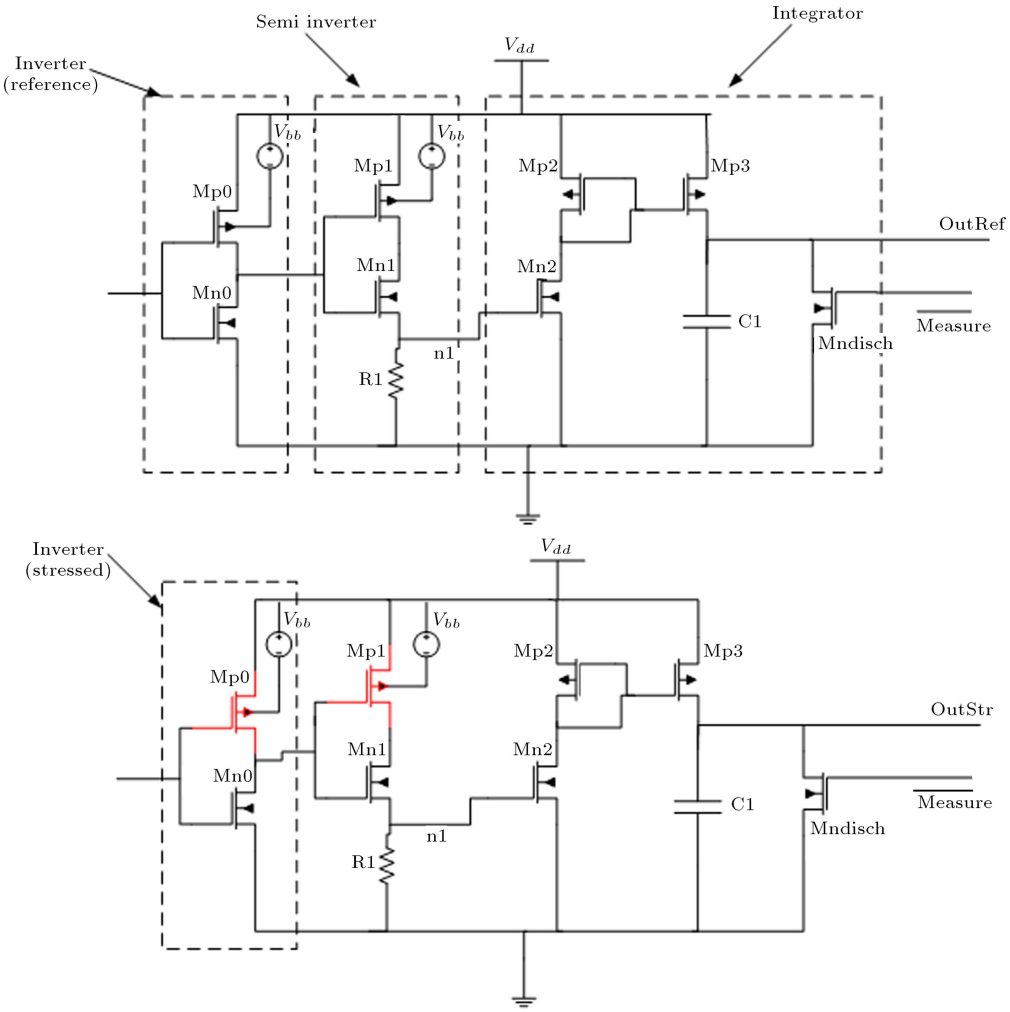

Figure 2. New sensor circuit.

is more than that in reference inverter. To reveal this difference, we propose the new Semi-Inverter circuit (Figure 2), which has a resistor in pull-down network.

When the input of Semi-Inverter switches is high, the transistor Mn1 will turn on. During input rise transition, both short-circuit and dynamic current pass through R1. With an increase in rise transition time due to NBTI, the current amplitude through R1 decreases, thus signal in node n1 of the stressed Semi-Inverter is wider (due to transition time increase) and lower in amplitude (due to current decrease), compared to that in the reference Semi-Inverter.

In the final stage of Figure 2, a simple charge-pump-based integrator [13] is used. The signal generated in Semi-Inverter output controls the on time and drain current of Mn2. When Mn2 switches on, Mp2 and Mp3 also turn on and charge Cl. Therefore, a voltage proportional to signal width, and amplitude of node n1 is generated at C1 in measurement period. Since n1 signal is different in reference circuit and stressed one, the signals OutStr and OutRef are different. This difference is directly related to NBTI effect in inverter.

The integration time constant in integrator depends on C1 and Mp3 currents, and can be tuned as required. In this design, the size of Mp3 and C1 is chosen for a small time constant such that the output would not saturate before the measurement of seven pulses. This issue will be explained further in the next section.

In sizing of Semi-Inverter, it is important to note that the voltage amplitude at n1 should be high enough in order to turn on Mn2. Output of integrator is reset to zero through the transistor Mndisch when stress period starts.

To have an accurate NBTI sensor, aging in pMOS of Semi-Inverter and integrator should be low or under control. This issue has been ignored in the past in the design of NBTI sensors. In this work, we control NBTI in all pMOS transistors by applying proper input signal. In stress period, pMOS of reference Semi-Inverter is in relaxed mode. In measurement period, its input is connected to the output of reference inverter. pMOS of the stressed Semi-Inverter is in stressed phase during stress period, while in measurement period its

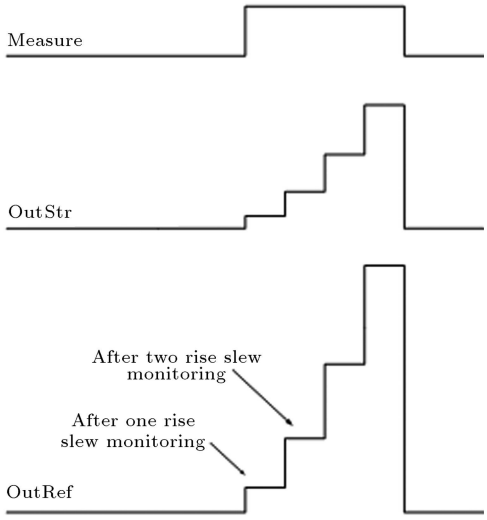

Figure 3. The wave form of stressed and reference circuit output signal and its difference.

gate is connected to the output of stressed inverter to measure the rise slew rate. Most of the time during the stress period, the Semi-Inverter output is low. Therefore, pMOS transistors in stressed integrator do not experience considerable aging effect, because they turn on for very short time when Semi-Inverter input experiences rise transition during stress period.

Although one pulse of the test signal is sufficient to detect the difference in rise slew-rate, more than one pulse is employed to measure the rise transition difference. This improves the sensor sensitivity and gain.

Thus final difference between OutRef and OutStr is the cumulative difference of all measured pulses, as shown in Figure 3. Clearly, the maximum number of pulses is chosen such that the integrator output is prevented from entering saturation. In this work, for sufficient sensitivity, we measure rise slew difference of seven pulses in test signal during each measurement period.

4. Simulation results

The proposed sensor has been designed and simulated using 65 nm Predictive Technology Model (PTM) [14], along with the predictive NBTI model [10-12]. A signal with 200 MHz frequency and 50% duty cycle is utilized for test signal in HSPICE. Figure 4 shows the differential output versus V_{th} change in pMOS of the stressed inverter. With an increase in the number of measured pulses, the sensor gain and sensitivity are increased. This sensor has average gain about 1.0 mV/mV when seven pulses are measured. Its resolution is about 0.5 mV change in V_{th} that causes 1 mV difference in output voltage.

Figure 4 shows the sensor output for 10 years

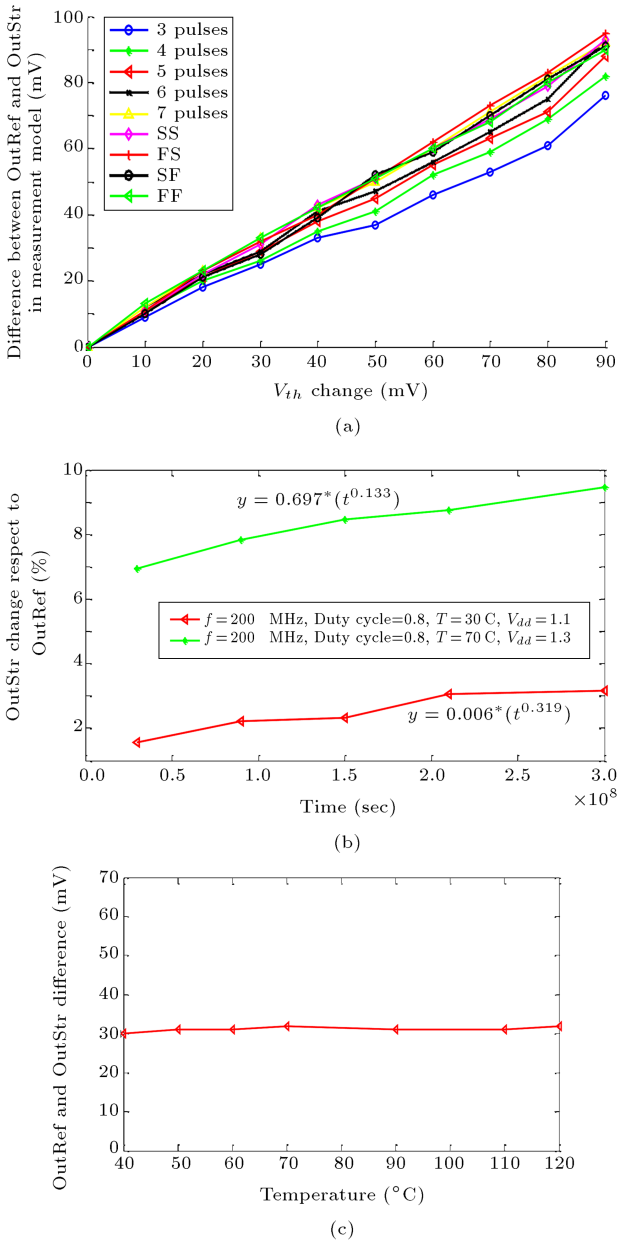

Figure 4. (a) Differential output voltage of the new proposed sensor with respect to V_{th} degradation in different process corners. When rise slew of more pulses is measured, sensitivity increases. (b) Sensor performance in different stress conditions applied in stress period. (c) Temperature variation has negligible effect on sensor performance and sensitivity.

lifetime in two different stress conditions. Since NBTI gets worse with increasing temperature and driving voltage, the difference between OutStr and OutRef of sensor is increased. Similar to threshold voltage, the sensor output voltage has a power-law dependency to time.

To show the weak dependency of this sensor to temperature variation, we changed the temperature when V_{th} degradation due to stress signal is 30 mV.

The temperature variation has negligible effect on the sensor resolution (Figure 4).

To study the effect of variation on this sensor, simulation is performed in five different process corners (SS, FF, NN, FS and SF). The result (Figure 4) confirmed that the sensor has acceptable performance in all corners. Sine both stress and reference circuit use identical structure, that are laid out next to each other, their dependency on process variation will be the same [6]. To account for the variation in supply voltage (10%), channel length, width, V_{th}, resistance and capacitance (5%), we have performed Monte Carlo simulation (1000 runs). Simulation shows a mean value of 1.0 mV/mV for average gain with standard deviation to mean ratio ($\frac{\sigma}{\mu}$) about 1%.

The mismatch in NBTI sensors can cause an initial offset. To cope with this, a solution is to measure the output change due to NBTI, with respect to initial offset [15]. As an alternative for the new sensor, one may utilize four voltage sources, two in reference circuit and two in stressed one, connected between body and source of PMOS transistor in both main inverter and semi-inverter (see V_{bb} in Figure 2). The mismatch in circuit causes the stressed circuit to differ from the stressed one at start point, giving rise to an initial offset (voltage difference) between OutStr and OutRef. The four voltage sources are tuned to change V_{bs} of the PMOS transistors, and hence to tune V_{th} such that the output voltage difference becomes zero. Therefore, by body biasing technique, the mismatch is compensated, and the sensor will accurately measure the NBTI degradation.

Figure 5 shows the layout of the sensor. The proposed NBTI sensor size is 12.3×8.0 μm^2. Table 1 shows the comparison of the new sensor with the recently reported NBTI sensors. It shows that the new sensor has a relatively lower power and area. Also, it can detect 0.5 mV shift in the threshold voltage with a gain of 2.

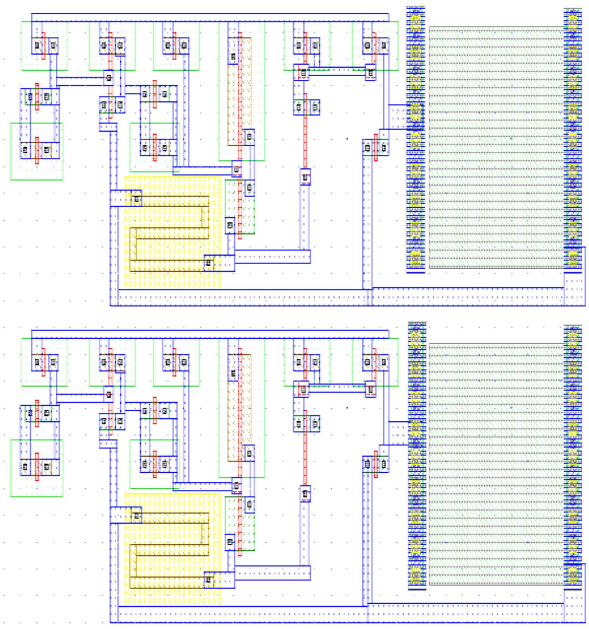

Figure 5. Layout of the proposed NBTI sensor.

5. Conclusions

This paper proposes a new NBTI sensor which measures the difference in rise slew degradation due to NBTI. The differential structure of the sensor limits the effect of environmental variation such as temper-

Table 1. Comparison between reliability monitoring circuits.

NBTI sensor	Tech.	Area (μm^2)	Average power (μW)	Measurement time	Resolution
[1]	45 nm	18.58×7.97	Stress mode: 8.57 Measure mode: 30.86	N/A	1 nsec/10 mV
[2]	130 nm	308	Stress mode: 0.0045 Measure mode: 0.5	N/A	53% (frequency degradation for ΔV_{th}=32mV
[5]	130 nm	265×132	N/A	2 μsec	0.8 ps (frequency resolution)
[7]	65 nm	214×551	N/A	<1 μsec	<1 ps (frequency resolution)
[8]	65 nm	90×90	N/A	N/A	0.25 mV/mV
[9]	130 nm	545×510 (two instances grouped)	N/A	tens of μsec	$\sim$5 (control voltage respect to ΔV_{th}=$\sim$ 10 mv)
This work	65 nm	12.3×8.0	Stress mode: 0.14 Measure mode: 4.54	50 nsec	1 mV/0.5 mV

ature. This sensor support both AC and DC stress measurements in a short time (about 50 nsec). The sensor resolution is about 1 mV for 0.5 mV degradation in V_{th}. Its average power consumption is 0.14 μW in stress mode and 4.54 μW during measurement mode. The implemented layout area is 98.9 μm^2.

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Biographies

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