Scientia Iranica, Vol. 10, No. 4, pp 477–480

SCIENTIA
IRANICA

Research Note

Si/Si, Si/SiO_2 and SiO_2/SiO_2 Fusion Wafer Bonding

A. Motieifar[1] and B. Rashidian*

The wafer bonding process has many applications in the fabrication of microelectronic, optoelectronic, power and micromachined devices. In this article, fusion bonding of silicon wafers and study of their interface are reported for the first time in Iran. Also, the bonding of two silicon wafers, with one (or both) of the wafers having a thermally grown silicon dioxide layer, has been performed and tested.

INTRODUCTION

Wafer bonding is a process by which two polished wafers adhere to each other without any intermediate layer or external force. In the literature, this process is also named as "Direct Wafer Bonding" or "Fusion Bonding". In most cases, the wafers that are bonded to each other consist of semiconductor materials, such as silicon and gallium arsenide, which are used in microelectronics and optoelectronics [1-3].

In this process, two cleaned and dried wafers are brought into contact with each other inside a clean atmosphere. By locally applying a slight pressure to adjacent wafers, two wafers bond to each other at that point and immediately the bonded area spreads laterally over the whole wafer area.

This bonding, achieved at room temperature, is not very strong. The Van der Waals bonds between the atoms of two wafers are weaker than metallic, covalent or ionic bonds in solids. Thus, for most applications, the room temperature bonded wafers have to undergo a heat treatment to strengthen the bonds across the interface. Sometimes voltage or pressure is also applied. During these treatments the bonding between two wafers becomes strong, as described later.

If the two-bonded wafers are made from dissimilar materials, the difference between their thermal expansion coefficients produces stress during the change of temperature, which may harm the bond between them.

Si/Si WAFER BONDING

The interaction forces between two contacted wafers are short range. Thus, to achieve a good bonding, the surfaces of the wafers must be sufficiently smooth, flat, clean and active. The flatness of the wafers must be better than 5μ and their roughness must be less than 10Å [4]. If the wafer does not have sufficient flatness and roughness, it must be polished. The most common method for polishing the wafers is chemo-mechanical polishing. Fortunately, conventional Si and GaAs wafers used for IC fabrication are convenient for bonding and do not need extra polishing. In this work, 2 inch, 250 μ thick n-type $< 111 >$ wafers were used.

For wafer bonding, wafers with clean surfaces, which are free of particle, organic and metallic contamination, are required. This is important because the surface cleanliness has a direct effect on both the structural and electrical properties of the bonding interface as well as on the resulting electrical properties of the bonded materials. The cleaning techniques employed prior to room-temperature wafer bonding must be able to remove all contamination on the surfaces without degrading the surface smoothness. Therefore, the wet chemical wafer cleaner, commonly used in the semiconductor industry, is fully applicable to wafer bonding. However, since the quality of the bonding interface is extremely sensitive to particulate

1. *Department of Electrical Engineering, Sharif University of Technology, P.O. Box 11365-9363, Tehran, I.R. Iran.*
*. *Corresponding Author, Department of Electrical Engineering, Sharif University of Technology, P.O. Box 11365-9363, Tehran, I.R. Iran.*

and organic contamination, additional cleaning techniques may be needed.

The first step in cleaning the wafers is degreasing. It is performed by successive cleaning in TCE, acetone and methanol. Then, the wafers are rinsed with deionized water. The next step is etching the native oxide layer from the surface of the wafers. This step is essential for some applications of wafer bonding such as the transfer of an epitaxial layer or the manufacturing of deep pn junctions. The native oxide is usually removed by a dip in 2% HF, DI water solution for about 30 minutes. The next step in surface cleaning is the most important step and is based on RCA solutions. This cleaning step involves two solutions: RCA1 and RCA2, which are used sequentially. RCA1 solution consists of NH_4OH:H_2O_2:H_2O (1:1:5) volumetric ratio. This solution is used to remove organic contamination by both the dissolving action of the NH_4OH and the oxidizing action of the H_2O_2 at high pH. The compound NH_4OH is also a strong complexing agent for some metals of groups I and II, such as Cu, Ag, Ni, Co and Cd. For washing with RCA1, at first NH_4OH and water are mixed and brought to the temperature of 80°C. Then, H_2O_2 is added and, just after that, the wafer is dipped in the solution. This solution with the wafer in it must boil for 10 minutes at 80°C, which can cause micro-roughening of the Si surface. The mean micro-roughness may increase from 1Å to 5Å. It has been found that it is better to use a modified RCA1 with its NH_4OH mixing ratio reduced to 0.25 [3,5].

After cleaning in RCA1, the wafers are rinsed thoroughly in DI water. RCA2 solution, consisting of HCl:H_2O_2:H_2O (1:1:5), is then used to remove metal and alkali contaminants like Al, Fe, Mg, Au, Cu and Na. The HCl in H_2O_2 forms soluble alkali and metal salts by dissolving or complexing [3]. As NH_4OH, HCl and H_2O_2 can generate gases at room temperature, RCA solutions are prepared immediately before use.

After surface cleaning, the wafers are brought out of the water and blown dry by filtered nitrogen gas. Then the surfaces of the wafers are placed on each other. Since there is a thin layer of gas between them, the top wafer is floating above the other one. When an external pressure is applied onto a small part of the pair (e.g. by tweezers) to push out the intermediate air, a bond is allowed to be formed by surface attraction forces between the wafers at that location. The bonding area spreads laterally over the entire surface of the wafers within a few seconds.

It is noticeable that the time between the last step of cleaning and contacting the wafers must be as short as possible. If this time is more than 5 minutes, the bonding may become difficult, due to contaminants absorbed at the surfaces and decrease of surface reactivation.

Up to this point, the process is reversible and the wafers can be separated from each other. In the next step, the room temperature bonded wafers have to undergo a heat treatment to strengthen the bonds across the interface.

When the wafers are pressed together and heated, the two opposite -OH groups interact forming a HOH and Si-O-Si Siloxane bond. The reaction can be described as:

$$\text{Si-OH} + \text{HO-Si} \rightarrow H_2O + \text{Si-O-Si}.$$

When heating the wafers to about 200°C, the available hydroxyl groups will contribute to the attraction through hydrogen bonds. To achieve a good bonding, annealing must be typically done at 800°C for 1 hour. If this step is performed at a lower temperature, its time must be increased. In reported works, the annealing temperatures for bonding two silicon wafers are between 400°C and 1200°C for a time between 40 h and 1 h.

In addition, experience has proved that an increase in the temperature or time of annealing results in higher quality and bonding strength. Of course, if the wafers are from dissimilar materials, which have different thermal expansion coefficients, the annealing temperature must be lower than 500°C. In this work, wafers in a hydrophilic state are used, using the RCA1 cleaning solution.

There is another approach in which the absence of the native oxide results in a hydrophobic surface. This is achieved mainly by cleaning the wafers in an HF based solution and rinsing in DI water [3]. The hydrophobic state is associated mainly with Si-H, Si-CH_x and Si-F groups. A few hydroxyl groups will also exist on the hydrophobic surface due to the water rinse. In a hydrophobic case, the dehydration of Si-H begins at temperatures around 400°C and very strong covalent Si-Si bonds are formed between the surfaces. In this case, to reach a good bonding, the wafer pair must be annealed at a temperature higher than 1000°C.

Also in a hydrophilic case, if the surface is heated to higher than 850°C, the oxygen atoms are removed and Si-Si bonds are formed.

Si/SiO_2 WAFER BONDING

Direct bonding makes it possible to bury a specific layer e.g. SiO_2 for Silicon-On-Insulator (SOI) applications, which is currently one of the most popular applications of direct bonding.

The method of direct bonding of two wafers in order to obtain a SOI wafer is similar to the bonding of two silicon wafers, except that before bonding, a thin, thermally oxide layer (about 1 micron) must be

grown on one or both of the wafers. Of course, there are some points that must be considered in order to obtain a good SOI wafer.

If the wafers are placed on each other in air, then the major component in the trapped gas is nitrogen. Nitrogen will also react with silicon but the activation energy of nitridation is much higher than that of oxidation. Silicon nitride is an effective diffusion barrier to nitrogen. The volume of trapped gas must be small enough to be consumed in the formation of these silicon compounds. Given this situation, the main approach is to mate the wafers in an oxygen atmosphere. Hydrogen and helium could also be used, since those gases would be able to diffuse through the silicon. Also, the mating of some wafer pairs in a high vacuum has been reported, in order to minimize the trapped gas volume [3].

Wafer bonding occurs when gaseous oxygen trapped between two wafers is converted to silicon dioxide by the oxidation of silicon. The volume occupied by oxygen is decreased by a factor of 4000 at 1000°C. Atmospheric pressure, exerted on the outer surfaces of the wafers, pushes the wafers together. Therefore, no external applied force is necessary to achieve intimate contact between the wafers.

RESULTS

The most difficult problem in performing a direct bonding process is due to contamination. After many unsuccessful attempts, the bonding of Si wafers was performed successfully. Also, wafers with a thin oxide layer on their surface were bonded successfully, all of them in a hydrophilic state.

A SEM photograph of the bonding area between two Si wafers can be observed in Figure 1. In the best conditions, the process yield was about 70%.

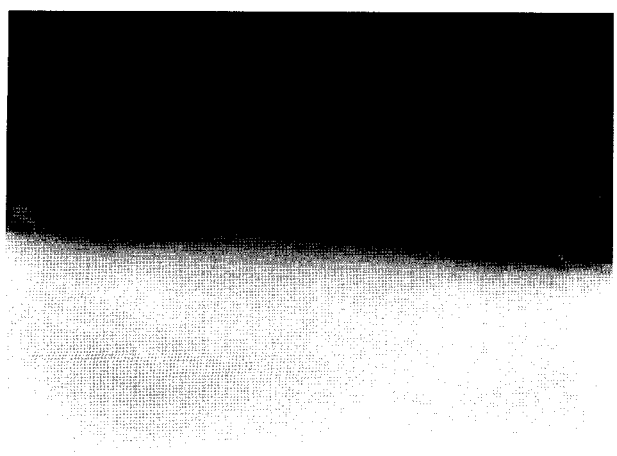

Figure 1. The SEM (Scanning Electron Microscopy) photograph of Si/Si structure's bonding area.

The bonding force in some samples is so high that the wafers cannot be separated by hand. This bonding force is measured with the simple apparatus (illustrated in Figure 2), which shows the bonding force to be 1.5- 3kg/cm^3. In the literature, the bonding force is reported to be between 2-3 kg/cm^3 [3].

The other important study on bonded wafers was the current versus voltage (I-V) characteristics of the Si/Si interface (Figure 3). The reason is the existence of interface energy states or traps that are filled by electrons. This strange behavior is discussed extensively in [6].

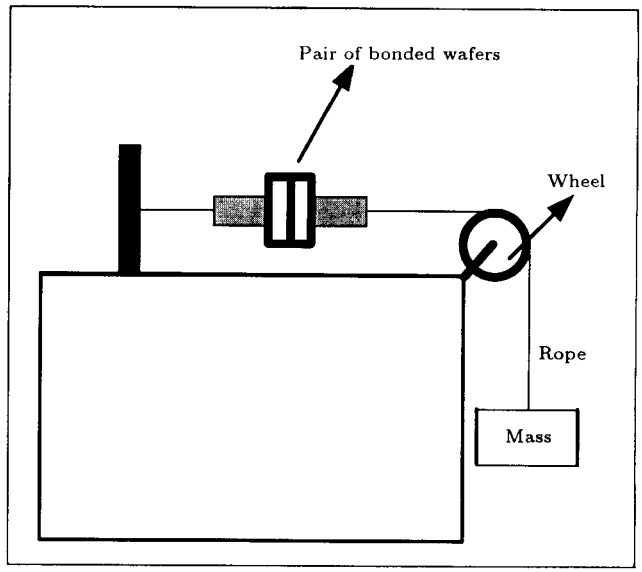

Figure 2. The apparatus used for measuring the bonding force.

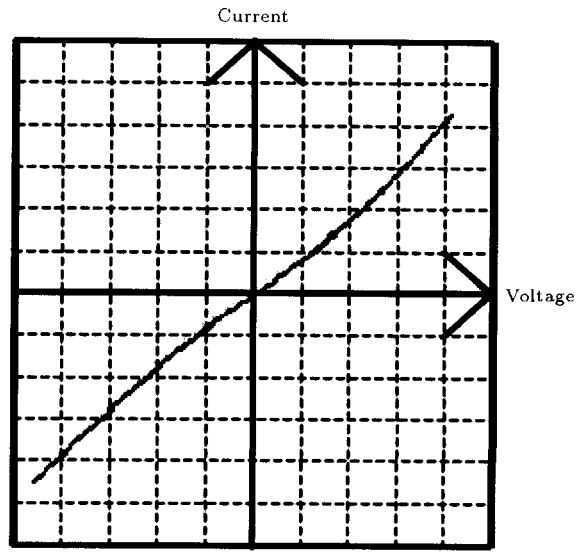

Figure 3. The I-V characteristics of Si/Si bonding interface ($\Delta v = 0.2$ V, $\Delta i = 0.75$ mA).

CONCLUSIONS

In this paper, a direct wafer bonding process has been reported in detail. Using this process, Si/Si and $Si/SiO_2/Si$ structures have been successfully realized for the first time in Iran.

REFERENCES

1. Lasky, J.B. "Wafer bonding for silicon-on-insulator technologies", *Applied Physics Letters*, **48**, pp 78-83 (1986).
2. Shimbo, M., Furukawa, K., Fukuda, K. and Tanazawa, K. "Silicon-to-silicon direct bonding method", *Journal of Applied Physics*, **60**(8), pp 2987-2989 (Oct. 1986).
3. Tong, Q.Y. and Goesele, U., *Semiconductor Wafer Bonding*, John Wiley, New York (1999).
4. Beggans, M., Farmer, K., Federici, J., Digges, T.G., Garofalini, S. and Hensely, D. "Bondability and surface roughness of ultra-thin single crystal silicon wafers", *Proceedings of the Fourth International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications*, Pennington, NJ, USA (1997).
5. Haque, A.S. and Moore, D. "Optimization of surface preparation for direct silicon-silicon bonding", *Proceedings of the 4th IEEE International Conference on Solid-State and Integrated Circuit Technology*, pp 527-529 (1995).
6. Khorasani, S., Motieifar, A. and Rashidian, B. "Dynamics of interface traps in bonded silicon wafers", *Semiconductor Science and Technology*, **17**(5), pp 421-426 (May 2002).