

Design and Realization of an Active-Only Grounded Memristor Emulator Supporting Incremental/Decremental Operations

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Keywords	Abstract
Analog circuit Current conveyor FGMOS CFDITA Pinched hysteresis loop Relaxation oscillator	A novel high-performance, active-only, grounded incremental/decremental memristor emulator is proposed in this research study. It is realized using a single floating-gate metal-oxide-semiconductor (FGMOS) based current follower differential input transconductance amplifier (CFDITA), one MOS-based capacitor, and one MOS-based resistor. The performance of the proposed FGMOS-based CFDITA and memristor emulator is verified through SPICE circuit simulations using 0.18 μm CMOS technology process parameters. The proposed CFDITA has demonstrated high performance, with a current dynamic range of ± 2.5 mA, an operational 3-dB bandwidth of 162 MHz, maximum transconductance of 1.1 mS and power consumption as low as 0.8 mW only. Theoretical analyses, including non-ideal and parasitic analyses of the proposed emulator, are also performed. The proposed emulator offers several desirable features, including a compact structure utilizing only active devices, low operating supply voltages of ± 0.75 V, low power dissipation of 0.8 mW, and a high simulation frequency of 40 MHz. The proposed circuit of emulator is further validated experimentally up to the experimental frequency of 50 kHz using off-the-shelf ICs AD844 and LM13700 with breadboard implementation.

1. Introduction

Currently, as transistor density requirements increase on a chip, technology is continuously being scaled down. Consequently, the threshold voltage of transistors is proportionally scaled down. Nevertheless, the threshold voltage cannot be reduced much further, as this would increase the sub-threshold leakage current. Therefore, in standard CMOS technology, the scaling of the threshold voltage has imposed a serious challenge for the circuit designers. To overcome this problem, numerous conventional and non-conventional techniques [1-9] have been reported. These techniques are extremely useful for realizing low-voltage and low-power (LVLP) CMOS structures. Some of the popular conventional techniques are sub-threshold operation, level shifting and dynamic threshold MOS (DTMOS). On the other hand, non-conventional techniques such as floating gate (FG), bulk-driven (BD), bulk-driven floating gate (BDFG), and quasi-floating gate (QFG) etc. are becoming very popular for designing LVLP active devices. Among these non-conventional techniques, the FG technique is preferably used to develop high-performance active devices in contemporary LVLP circuit design because of its reduced signal path threshold voltage. In many applications, such as FLASH memory, EPROM, and EEPROM, the FG technique has been preferred because of its compatibility with the CMOS technology and lower supply voltage requirements.

Evidently, the development of high-performance active devices is also expected for various applications of VLSI and signal processing. In all these applications, one or more of the four fundamental passive components of the electronic industry namely the resistor, capacitor, inductor, and memristor are utilized to showcase the constitutive relationships among the four fundamental parameters, namely, voltage, current, charge, and flux [10-11]. Among these four aforementioned passive components, only the memristor has the unique properties of a pinched hysteresis loop (PHL), non-linearity, frequency-dependent characteristics, and high-density storage capability. For this reason, some of the applications can only be realized with memristor(s) and not with RLC networks alone. Nonetheless, due to the cost and technical difficulties associated with the fabrication of micro- and nano-scale devices, memristor emulators have gained widespread attention from researchers. As a result, a variety of memristor emulators have been reported in the literature [12-38]. However, these emulators have one or more of the following shortcomings (i) the number of active elements in the emulators designs in [14-15, 18, 20, 22-25, 28, 30, 32] is more than one (excluding MOS) (ii) a larger number of passive components are used in [14, 20, 24, 25, 27, 33-34] (iii) mixed types of active building blocks (ABBs) are used in the works reported in [14-15, 20, 23-25, 28, 30, 32] (excluding MOS) (iv) the operating frequency in the designs of [12-24, 26-34, 36-38] is low (v) the operating supply voltages used in the works of [12-25, 27-28, 30-38] are high (vi) the memristor emulators presented in [22, 27, 32] consume high power (vii) the works reported in [15, 20, 24-25] utilize a multiplier to yield a pinched hysteresis.

This research work provides a complete solution through the proposal of a high performance LVLP active element, namely, a current follower differential input transconductance amplifier (CFDITA) based on the FG approach. The floating gate metal-oxide-semiconductor (FGMOS)-based CFDITA structure is proposed to provide a better alternative to existing MOS-based CFDITA structures [39-40] due to the availability of salient features, such as good dynamic range, low supply voltages and low power consumption. The presented active device, the FGMOS-based CFDITA, is further utilized in the design of a grounded incremental/decremental memristor emulator. The proposed memristor emulator design is simple in structure, as it uses only one FGMOS-based CFDITA, one MOS-based resistor and one MOS-based capacitor only. The detailed ideal and non-ideal analyses of the proposed emulator are included. The functionality of the design is validated using both SPICE simulations and experimental measurements.

2. Overview of FGMOS-based CFDITA

FGMOS devices have recently been used by analog researchers in a variety of emerging applications, including FG memory cells, the digital storage elements in EPROM, EEPROM, and flash memory technologies, neural networks and instrumentation and measurement devices. In contrast to conventional CMOS, which has only one controlling gate (CG), FGMOS includes an additional gate, designated as the FG. It is possible to develop FGMOS using the standard fabrication technique of double-polysilicon CMOS. In this process, the first polysilicon layer is used to create the FG over the channel, and the second layer creates multiple inputs CG. There is no resistive connection between the FG and multiple inputs CG; instead, they are connected capacitively [41]. Figures 1 (a) and (b) show the symbols for two-input p-channel FGMOS and n-channel FGMOS respectively and Figures 2 (a) and (b) show the equivalent circuits for the two-input p-channel FGMOS and n-channel FGMOS respectively. The FG voltage, V_{FG} can be expressed as follows.

$$V_{FG} = \frac{C_{FGD}V_D + C_{FGS}V_S + C_{FGB}V_B + \sum C_{Gi}V_i + Q_0}{C_{eff}} \quad (1)$$

where $i=1, 2$ for the two inputs as shown in the circuits of Figure 2. The voltages V_D , V_S and V_B represent drain, source and bulk voltages respectively. Total capacitance at the gate terminal of FGMOS is C_{eff} as given below.

$$C_{eff} = C_{G1} + C_{G2} + C_{FGD} + C_{FGB} + C_{FGS} \quad (2)$$

where C_{G1} is the capacitance formed between the input V_{G1} and FG; C_{G2} is the capacitance formed between the input V_{G2} and FG. Capacitances C_{FGD} , C_{FGB} and C_{FGS} are the parasitic capacitances between FG and drain, FG and bulk, and FG and source of FGMOS respectively.

The CFDITA symbol as depicted in Figure 3 comprises of three high impedance terminals Z , V and O and one low impedance terminal F . FGMOS structure of CFDITA is elucidated in Figure 4 which consists of bilateral current follower (MOS transistors from $M_1 - M_{18}$, $M_{23} - M_{34}$) followed by an OTA (MOS transistors from $M_9 - M_{22}$). The CFDITA is characterized as given below.

$$\begin{bmatrix} V_F \\ I_Z \\ I_V \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & -g_m & g_m & 0 \end{bmatrix} \begin{bmatrix} I_F \\ V_Z \\ V_V \\ V_O \end{bmatrix} \quad (3)$$

where g_m is the transconductance of OTA stage and it is expressed as follows.

$$g_m = K(V_B - V_{SS} - V_{TH}) \quad (4)$$

In Eq. (4), $K = \frac{\mu C_{ox}}{\sqrt{2}}(W/L)$ and V_{TH} is the threshold voltage of M_{19} transistor. It is noted from Figure 4 that it comprises of two additional terminals Z_C and Z_{C-} which are used in memristor application in next section. The relationships at these terminals are $I_{ZC} = I_F$ and $I_{ZC-} = -I_F$.

The parasitic of CFDITA at different terminals are depicted in Figure 5. The parasitic involved are low parasitic resistance R_F at terminal, F and high parasitic R_Z in parallel with $1/sC_Z$, R_V in parallel with $1/sC_V$, and R_O in parallel with $1/sC_O$ at Z , V , and O terminals respectively.

3. Simulation results of FGMOS-based CFDITA

PSpice simulations using 0.18 μm CMOS technology are carried out for the verification of the proposed device. The supply voltages used are $\pm 0.75\text{V}$. Aspect ratios, $W(\mu\text{m})/L(\mu\text{m})$ of the MOSFETs incorporated in the implementation of proposed FGMOS-based CFDITA are given as follows: $M_{1,2,27,29} = 72/0.36$, $M_3 = 3.6/0.36$, $M_{4,5,9,10,11,12,21,22,33,34} = 36/0.36$, $M_{6,7,14,16,17,23,24,25,26,28,30} = 144/0.36$, $M_{8,15,18} = 0.36/0.36$, $M_{13} = 54/0.36$, $M_{19} = 10.8/0.36$, $M_{20} = 18/0.36$, $M_{31,32} = 108/0.36$. The DC transfer characteristics between terminal F and terminal Z as shown in Figure 6 (a) has dynamic range of the current as -2.5 mA to 2.5 mA . The DC analysis for transconductance, $I_O / (V_V - V_Z)$ with respect to the bias current, I_B for a variation of I_B from 0 to $400\text{ }\mu\text{A}$ is depicted in Figure 6 (b). The maximum transconductance obtained in Figure 6 (b) is 1.1 mS . The frequency response for current gain, is illustrated in Figure 6 (c), where the 3-dB bandwidth is measured as 450 MHz . The frequency response for transconductance gain, $I_O / (V_V - V_Z)$ is depicted in Figure 6 (d) and the 3-dB bandwidth of the transconductance gain is obtained as 162 MHz . The performance characteristic parameters of the proposed FGMOS CFDITA are summarized in Table 1. Additionally, its comparison with other existing FGMOS-based devices [5-8] is illustrated in Table 2. It is observed that the proposed CFDITA performs better in terms of dynamic range, supply voltages and power consumption.

4. Proposed Electronically Tunable Memristor Emulator

The proposed grounded incremental/decremental memristor emulator using single CFDITA, one active MOS resistor and one active MOS capacitor is shown in Figure 7. The MOS transistor M_R realizes a floating resistance, R_M . and MOS transistor M_C realizes a grounded capacitor, C_M . The resistance R_M is electronically tunable via control voltage, V_C . The proposed emulator operates in a decremental mode if the switch is coupled with terminal Z_C and operates in incremental mode if the switch is coupled with terminal Z_{C-} .

4.1 Analysis of Memristor Emulator

The analysis of the decremental memristor emulator is described as follows. The current through the capacitor is obtained as follows.

$$I_C = -V_{in} / R_M \quad (5)$$

The capacitor voltage, V_{CA} is same as the bias voltage of OTA stage, V_B and is given as follows.

$$V_{CA} = V_B = \frac{1}{C_M} \int I_C dt = -\frac{1}{R_M C_M} \int V_{in} dt \quad (6)$$

The expression of flux for the proposed emulator is described as follows.

$$\phi_{in} = \int V_{in} dt \quad (7)$$

The capacitor voltage, V_{CA} can be expressed in terms of ϕ_{in} as given in Eq. (8).

$$V_{CA} = V_B = -\frac{\phi_{in}}{R_M C_M} \quad (8)$$

Substituting V_B in Eq. (4), the transconductance, g_m is now expressed as given below.

$$g_m = K \left(-\frac{\phi_{in}}{R_M C_M} - V_{SS} - V_{TH} \right) \quad (9)$$

The applied input voltage, V_{in} is related to the observed input current, I_{in} as follows.

$$I_{in} = \left(\frac{2}{R_M} + g_m \right) V_{in} \quad (10)$$

Using Eqs. (9)-(10) the flux-controlled memductance, $W(\phi_{in})$ is outlined as follows.

$$W(\varphi_{in}) = \frac{I_{in}}{V_{in}} = \frac{2}{R_M} + K(-V_{SS} - V_{TH}) - K \frac{\varphi_{in}}{R_M C_M} \quad (11)$$

It is significant to note that the power supply, V_{SS} is negative in Eq. (11). It is to be noted that the fixed part of memductance which defines initial memductance, can be controlled electronically via control voltage, V_C . The variable component, on the other hand, is dependent on the input flux, resistor R_M and capacitor C_M . It should be stated that the negative value of variable component indicates a decremental memristor emulator. The voltage, V_{in} is now assumed to be a sinusoidal signal i.e. $V_{in} = V_m \sin \omega t$. The expression of flux is now given as follows.

$$\varphi_{in} = \frac{V_m}{\omega} \cos(\omega t - \pi) \quad (12)$$

Subsequently, the memductance of the memristor emulator is modified as given in Eq. (13).

$$W(\varphi_{in}) = \frac{I_{in}}{V_{in}} = \frac{2}{R_M} + K(-V_{SS} - V_{TH}) - K \frac{V_m \cos(\omega t - \pi)}{\omega R_M C_M} \quad (13)$$

Eq. (13) shows that memductance is reliant on the input signal parameters amplitude and frequency, resistor R_M and capacitor C_M . It is also observed from Eq. (13) that for infinite value of input frequency, the memristor operates as a linear resistor.

Moreover, the memductance represented in Eq. (13) can have a negative value if the frequency becomes low, so it reflects the operation of decremental memristor emulator. The limitation of minimum operating frequency (f_{min}) which prevents the memductance to become negative is given in Eq. (14).

$$f_{min} \gg \frac{KV_m}{2\pi \left(\frac{2}{R_M} + K(-V_{SS} - V_{TH}) \right) R_M C_M} \quad (14)$$

On similar grounds, incremental memristor emulator can be designed if a switch is connected across Z_{C-} and analysis of the circuit yields the following memductance expression.

$$W(\varphi_{in}) = \frac{I_{in}}{V_{in}} = \frac{2}{R_M} + K(-V_{SS} - V_{TH}) + K \frac{V_m \cos(\omega t - \pi)}{\omega R_M C_M} \quad (15)$$

4.2 Non-Ideal Study of Memristor Emulator

The non-ideal model of CFDITA is characterized by the following port relationships.

$$I_Z = \alpha_1 I_F, I_{ZC} = \alpha_2 I_F, I_{ZC-} = \alpha_3 I_F, I_O = \gamma g_m (V_V - V_Z) \quad (16)$$

where α_1 , α_2 and α_3 are the non-ideal current gains and γ is the transconductance inaccuracy. The proposed memristor emulator is analyzed again taking into consideration the non-ideality and parasitic of CFDITA. The observed input current and applied voltage relation is as follows.

$$I_{in} = \left(\frac{1 + \alpha_1}{R_M} + g_m \right) V_{in} \quad (17)$$

The modified transconductance, g_m is now expressed in Eq. (18).

$$g_m = K \left(-\frac{\alpha_2 \varphi_{in}}{R'_M C'_M} - V_{SS} - V_{TH} \right) \quad (18)$$

where $R'_M = R_F + R_M$, $C'_M = C_{ZC} + C_M$.

The modified expression of memductance of the proposed emulator is given as in Eq. (19).

$$W(\varphi_{in}) = \frac{I_{in}}{V_{in}} = \frac{1+\alpha_1}{R'_M} + \gamma K(-V_{SS} - V_{TH}) - \alpha_2 \gamma K \frac{\varphi_{in}}{R'_M C'_M} \quad (19)$$

The memductance of the proposed decremental memristor emulator in terms of amplitude and frequency of the input signal is given in Eq. (20).

$$W(\varphi_{in}) = \frac{I_{in}}{V_{in}} = \frac{1+\alpha_1}{R'_M} + \gamma K(-V_{SS} - V_{TH}) - \alpha_2 \gamma K \frac{V_m \cos(\omega t - \pi)}{\omega R'_M C'_M} \quad (20)$$

Similarly, memductance of the proposed incremental memristor emulator is outlined as follows.

$$W(\varphi_{in}) = \frac{I_{in}}{V_{in}} = \frac{1+\alpha_1}{R'_M} + \gamma K(-V_{SS} - V_{TH}) + \alpha_3 \gamma K \frac{V_m \cos(\omega t - \pi)}{\omega R'_M C'_M} \quad (21)$$

5. Simulation Results of Memristor Emulator

The proposed memristor emulator is verified using PSPICE simulations with ± 0.75 V supply voltages. The W/L ratio of MOS transistor used as a MOS capacitor is selected as $35 \mu\text{m}/50 \mu\text{m}$ to yield a capacitance value of 4 pF. The W/L ratio of MOS transistor used as resistor is selected as $4 \mu\text{m}/2 \mu\text{m}$ to yield a resistance value of 2 k Ω . Control voltage is selected as $V_C = 0.65$ V, input voltage V_{in} is a sinusoidal voltage signal, with an amplitude of 0.3 V and a frequency of 2 MHz. The circuit of decremental memristor emulator is verified first. Figure 8 illustrates the transient responses of the proposed decremental memristor emulator for voltage signal, V_{in} and current signal, I_{in} . A non-linear behavior in memristor current is observed in this. Additionally, the fundamental property of memristor emulator (current signal, I_{in} converges to zero when voltage signal, V_{in} is zero) is also confirmed in this. The PHLs of the proposed memristor emulator for different frequencies (2, 5 and 10 MHz) are shown in Figure 9 (a). It is noted that the relationship in voltage and current is more non-linear at lower frequency. The pinched hysteresis characteristics of the proposed memristor emulator for two distinct values of frequency as well as a capacitor to yield a constant multiplication factor are shown in Figure 9 (b). It has been observed that PHL remains unchanged for a constant multiplication factor irrespective of the change in values of frequency and capacitor. Figure 10 shows the PHLs at 5 MHz frequency for different values of control voltages (0.65, 0.8 and 0.95 V). In this, the resistance R_M decreases with the increment in control voltage and hence increases the memristor current.

The impact of process, voltage, and temperature (PVT) variations on the PHL of the proposed emulator has been thoroughly examined. Figure 11 (a) illustrates the effect of variation in supply voltages on PHL, showing the responses at three different voltage levels: ± 0.65 V, ± 0.75 V, and ± 0.85 V. A slight variation in current amplitude is observed with changes in the supply voltage. Figure 11 (b) presents the PHLs at various temperatures (25°C, 40°C, 55°C, and 70°C), indicating that the pinched characteristics of the proposed emulator are minimally affected by temperature variations. To evaluate the influence of process variations, Monte Carlo (MC) simulations with 100 runs are conducted, incorporating a 1% Gaussian deviation in the threshold voltages and gate oxide thickness of the MOS transistors. The resulting PHLs from these simulations are shown in Figure 12 (a). Figure 12 (b) displays a histogram of the peak memristor current, revealing a mean value of 286 μA (3% deviation from the ideal value). Figure 12 (c) shows the histogram of the memristor current frequency, with a mean value of 1.99 MHz (0.5% deviation from the nominal frequency). The effects of process corners namely, Slow-Slow (SS), Typical-Typical (TT), and Fast-Fast (FF) on the PHL of the proposed emulator have also been investigated. Figure 13 presents the corresponding PHLs under these three process conditions. The results indicate that while there are slight variations in the PHLs due to process corner shifts, the overall characteristics remain largely preserved, demonstrating the robustness of the proposed design against process-induced variations. The proposed decremental memristor emulator is also tested at higher frequencies (20, 30 and 40 MHz) as illustrated in Figure 14 where capacitance value is chosen as 1 pF. The proposed incremental memristor emulator is also verified. The PHLs between voltage and current of the proposed incremental memristor emulator for different frequencies (2, 5 and 10 MHz) are shown in Figure 15. The memory behavior of the proposed incremental and decremental memristor emulators is evaluated using a pulse signal of 80 mV amplitude, with a pulse width of 50 nS and a pulse period of 200 nS. Figures 16 (a) and (b) depict the corresponding transient responses for the incremental and decremental emulators, respectively. As observed, the memristor current increases or decreases during the ON phase of the pulse and retains its last value during the OFF phase, demonstrating the characteristic non-volatile memory behavior of the emulators.

6. Experimental Results

The proposed memristor emulator circuit is verified experimentally using commercially available off-the-shelf ICs AD844, LM13700 and discrete components on a breadboard. The schematic diagram of the proposed memristor emulator is illustrated in Figure 17 (a) along with a picture of the breadboard setup shown in Figure 17 (b). When switch S is set to position 1, it functions as an incremental memristor emulator, while in position 2, it operates as a decremental memristor. It is important to note that an additional resistor R_2 is utilized in the practical circuit to implement the Z_C and Z_{C-} terminals. Resistors R_3 and

R_4 , each valued at $10\text{ k}\Omega$, are utilized to supply bias current to the OTA IC, LM13700. A supply voltage of $\pm 10\text{ V}$ is applied during the experiment. The input sinusoidal voltage signal ($5V_{pp}$) is generated using a RIGOL 200 DG822 function generator, and the resulting waveforms are captured and displayed on a RIGOL DS1104 digital storage oscilloscope (DSO). The capacitor value is selected as $C = 1\text{ nF}$. The current through the memristor is measured according to the method illustrated in Figure 18 (b) of [31]. Figures 18 (a) and (b) respectively display the transient waveforms and PHLs of the incremental memristor at frequencies of 5 kHz and 20 kHz , with resistor values set as $R_1 = R_2 = 10\text{ k}\Omega$. The transient waveforms and PHLs of the incremental memristor at frequencies of 20 kHz and 100 kHz are shown in Figures 19 (a) and (b) respectively when the resistor values are adjusted to $R_1 = R_2 = 1\text{ k}\Omega$ and PHLs are observed to shrink with the increase in frequency. Figures 20 (a) and (b) illustrate the transient waveforms and PHLs of the decremental memristor at frequencies of 5 kHz and 20 kHz respectively.

7. Application as Relaxation Oscillator

The proposed grounded memristor emulator is utilized in the relaxation oscillator to evaluate its reliability. An op-amp-based relaxation oscillator, which is a well-known circuit, serves to assess the usefulness of the proposed memristor emulator. The grounded resistance in the circuit is substituted with the introduced memristor emulator as shown in Figure 21. A thorough mathematical derivation explaining the operation of the relaxation oscillator with the memristor emulator can be found in [42]. The parameters used to analyze the performance of the relaxation oscillator incorporating the memristor emulator, are given as follows: Externally connected components $R_0 = 50\text{ k}\Omega$, $R_1 = 10\text{ k}\Omega$ and $C = 100\text{ nF}$. The simulation parameters for the emulator are taken as $R_M = 4\text{ k}\Omega$ and $C_M = 100\text{ nF}$. A Zener diode of 10 V is included to restrict the output voltage of the square wave. The simulation results show the output square voltage (V_s), capacitor voltage (V_C) and memristor voltage (V_M), as illustrated in Figure 22. The output square voltage has a magnitude of 1.1 V with oscillation frequency of 350 Hz . In contrast to [42], which incorporates six active blocks and nine passive components in its memristor emulator, the relaxation oscillator depicted in Figure 21 utilizes a more streamlined memristor emulator comprising only one active block and two passive elements.

8. Comparison Study

This section provides a comparison of the proposed memristor emulator with the relevant previously reported emulators as summarized in Table 3. The comparison is based on the number of active elements, the number of passive components, the use of similar types of active elements, operating frequency, supply voltages, power consumption, and the use of an analog multiplier (AM). It is observed from the table that the proposed design uses only one ABB, along with one MOS-based capacitor and one MOS-based resistor, offers good operating frequency (40 MHz), low supply voltages ($\pm 0.75\text{ V}$) and low power consumption (0.8 mW). The proposed memristor emulator can be utilized in various analog signal processing applications, such as filters and chaotic oscillators, in neuromorphic applications, and in IoT as a motion detector system [43–45]. A recent trend in analog circuit design is to extend the memristor emulator circuits to realize the memcapacitor and meminductor emulators [46–49].

9. Conclusion

In this research work, an active device based on FG technology, namely, the CFDITA is presented. This proposed device is proven to be a high-performance device with a current dynamic range of $\pm 2.5\text{ mA}$, an operational bandwidth of 162 MHz , a maximum transconductance of 1.1 mS and a power consumption as low as 0.8 mW only. This high-performance device is further used to realize a grounded incremental/decremental memristor emulator. The proposed memristor emulator design supports modern integration technology due to the use of only MOS transistors and exhibits the non-linear behavior in the absence of a complex multiplier. The detailed ideal and non-ideal analyses of the proposed design are included in this research study. The performance of the proposed design is validated through SPICE simulations. The designed memristor emulator exhibits a high operational simulation frequency of 40 MHz , low power consumption of 0.8 mW and low supply voltages of $\pm 0.75\text{ V}$. The proposed memristor emulator is also experimentally verified using commercial ICs AD844 and LM13700 and operational experimental frequency is observed to be 50 kHz . All the results are in good agreement with the theoretical analysis.

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Conflicts of interest

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Authors' Credit

Atul Kumar. Investigation; Validation; Supervision; Project administration;

Bhartendu Chaturvedi. Conceptualization; Writing – Review & Editing; Supervision

Shafali Jagga. Data curation; formula analysis; Methodology; Resources; Software; Visualization; Roles/ Writing; Original draft;

REFERENCES

1. Behir, M., Aloui, I. and Hassen, N. "A bulk-driven quasi-floating gate FVF current mirror for low voltage, low power applications", *Integration*, 74, pp. 45-54 (2020) <https://doi.org/10.1016/j.vlsi.2020.04.002>
2. Ferri, G. and Guerrini, N.C. "Low-voltage low-power CMOS current conveyors", *Springer Science & Business Media*, (2003) https://doi.org/10.1007/0-306-48720-9_5
3. Minaei, S., Sayin, O.K. and Kuntman, H. "A new CMOS electronically tunable current conveyor and its application to current-mode filters", *IEEE Transactions on Circuits and Systems I: Regular Papers*, 53(7), pp. 1448-57 (2006) <https://doi.org/10.1109/TCSI.2006.875184>
4. Khateb, F., Kulej, T., Veldandi, H., et al. "Multiple-input bulk-driven quasi floating-gate MOS transistor for low-voltage low-power integrated circuits", *AEU-International Journal of Electronics and Communications*, 100, pp. 32–38 (2019) <https://doi.org/10.1016/j.aeue.2018.12.023>
5. Aggarwal, B. and Gupta, A. "QFGMOS and FGMOS based low-voltage high performance MI-OTA", *International Journal of Information Technology*, 13(2), pp. 415-22 (2021) <https://doi.org/10.1007/s41870-020-00541-6>
6. Rana, C., Prasad, D. and Afzal, N. "Low voltage floating gate MOSFET based current differencing transconductance amplifier and its applications", *Journal of Semiconductors*, 39(9), p. 094002 (2018) <https://doi.org/10.1088/1674-4926/39/9/094002>
7. Arora, Y., Aggarwal, B. and Kaur, J. "Low Voltage High Performance Floating Gate and Quasi Floating Gate CDTA", *Journal of Engineering. Research ICAPIE Special Issue*, pp. 144-52 (2022) <https://doi.org/10.36909/jer.ICAPE.15045>
8. Prasad, P., Gautam, S. and Aggarwal, B. "FGMOS based Gain Tunable and Low Power OTRA Circuit", in *International Conference on Computing, Power and Communication Technologies (GUCON)*, pp. 139-143. IEEE (2019) ISBN: 978-93-5351-098-5
9. Algueta-Miguel, J.M., De La Cruz Blas, C.A. and Lopez-Martin, A.J. "Balanced Gm-C filters with improved linearity and power efficiency", *International Journal of Circuit Theory and Applications*, 43 (9), pp. 1147-1166 (2015) <https://doi.org/10.1002/cta.2001>
10. Chua, L.O. "Memristor-The missing circuit element", *IEEE Transactions on Circuit Theory*, 18 (5), pp. 507–519 (1971) <https://doi.org/10.1109/TCT.1971.1083337>
11. Strukov, D.B., Snider, G.S., Stewart, D.R., et al. "The missing memristor found", *Nature*, 453, pp. 80–83 (2008) <https://doi.org/10.1038/nature06932>
12. Yesil, A. "Floating Memristor Employing Single MO-OTA with Hard-Switching Behavior", *Journal of Circuits, Systems and Computers*, 28 (2), p. 1950026 (2019) <https://doi.org/10.1142/S0218126619500269>
13. Yesil, A., Babacan, Y. and Kacar, F. "Electronically tunable memristor based on VDCC", *AEU International Journal of Electronics and Communications*, 107, pp. 282–290 (2019) <https://doi.org/10.1016/j.aeue.2019.05.038>
14. Ranjan, R.K., Sagar, S., Roushan, S., et al. "High frequency floating memristor emulator and its experimental results", *IET Circuits, Devices & Systems*, 13 (3), pp. 292-302 (2019) <https://doi.org/10.1049/iet-cds.2018.5191>
15. Cam Taskiran, Z.G. Ayten, U.E. and Sedef, H. "Dual-output operational transconductance amplifier based electronically controllable memristance simulator circuit", *Circuits, Systems, and Signal Processing*, 38, pp. 26-40 (2019) <https://doi.org/10.1007/s00034-018-0856-y>
16. Yesil, A. and Babacan, Y. "Design of memristor with hard-switching behavior employing only one CCCII and one capacitor", *Journal of Circuits, Systems and Computers*, 30 (09), p. 2150151 (2021) <https://doi.org/10.1142/S0218126621501516>

17. Prasad, S.S. Kumar, P. and Ranjan, R.K. "Resistorless Memristor Emulator Using CFTA and Its Experimental Verification", *IEEE Access*, 9, pp. 64065-75 (2021) <https://doi.org/10.1109/ACCESS.2021.3075341>
18. Bhardwaj, K. and Srivastava, M. "New electronically adjustable memelement emulator for realizing the behaviour of fully-floating meminductor and memristor", *Microelectronics Journal*, 114, p. 105126 (2021) <https://doi.org/10.1016/j.mejo.2021.105126>
19. Gul, F. and Babacan, Y. "A novel OTA-based circuit model corroborated by an experimental semiconductor memristor", *Microelectronic Engineering*, 194, pp. 56–60 (2018) <https://doi.org/10.1016/j.mee.2018.03.012>
20. Cam, Z.G. and Sedef, H. "A New floating memristance simulator circuit based on second generation current conveyor", *Journal of Circuits, Systems and Computers*, 26(2), p. 1750029 (2017) <https://doi.org/10.1142/S0218126617500293>
21. Yesil, A., Babacan, Y. and Kacar, F. "Electronically tunable memristor based on VDCC", *AEU International Journal of Electronics and Communication*, 107, pp. 282–90 (2019) <https://doi.org/10.1016/j.aeue.2019.05.038>
22. Sagar. Raj, N. Verma, V.K. and Ranjan, R.K. "Electronically Tunable Flux-Controlled Resistor-less Memristor Emulator", *IEEE Canadian Journal of Electrical and Computer Engineering*, 45(3), pp. 311-17 (2022) <https://doi.org/10.1109/ICJECE.2022.3182711>
23. Sagar. Ranjan, R.K. and Kang, S.M. "Resistorless Floating / Grounded Memristor Emulator Model with Electronic Tunability", *IEEE Transactions on Circuits and Systems II, Express Briefs*, 70(7), pp. 2340-44 (2023) <https://doi.org/10.1109/TCSII.2023.3242301>
24. Pu, Y. and Yu, B. "A large dynamic range floating memristor emulator with equal port current restriction", *IEEE/CAA Journal of Automatica Sinica*, 7(1), pp. 237-43 (2020) <http://dx.doi.org/10.1109/JAS.2019.1911849>
25. Cao, H. and Wang, F. "Spreading operation frequency ranges of memristor emulators via a new sine-based method", *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, 29 (4), pp. 617-30 (2020) <https://doi.org/10.1109/TVLSI.2021.3056472>
26. Thomas, S.A. Vohra, S.K, Kumar, R., et al. "Analysis of Parasitic Effects in a Crossbar in CMOS Based Neuromorphic System for Pattern Recognition Using Memristive Synapses", *IEEE Transactions on Nanotechnology*, 21, pp. 380-389 (2022) <https://doi.org/10.1109/TNANO.2022.3190903>
27. Kumar, P. Makhdoomi, B.S. Verma, J.S., et al. "Experimental validation of a high-frequency memristor emulator based on CCCCTA framework and its application in chaos circuit", *AEU - International Journal of Electronics and Communications*, 190, p. 155624 (2025) <https://doi.org/10.1016/j.aeue.2024.155624>
28. Raj, A. Singh, S. and Kumar, P. "Dual mode, high frequency and power efficient grounded memristor based on OTA and DVCC", *Integrated Circuits and Signal Processing*, 110, pp. 81-89 (2022) <https://doi.org/10.1007/s10470-021-01949-1>
29. Ananda, Y.R. Raj, N. and Trivedi, G. "A MOS-DTMOS Implementation of Floating Memristor Emulator for High-Frequency Applications", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 31(3), pp. 355-368 (2023) <https://doi.org/10.1109/TVLSI.2022.3227201>
30. Yadav, N. Rai, S.K. and Pandey, R. "New grounded and floating memristor emulators using OTA and CDBA", *International Journal of Circuit Theory and Applications*, 48(7), pp. 1154-79 (2020) <https://doi.org/10.1002/cta.2774>
31. Kumar, A. Chaturvedi, B. and Mohan, J. "Minimal realizations of integrable memristor emulators", *Journal of Computational Electronics*, 22(1), pp. 504-18 (2023) <https://doi.org/10.1007/s10825-022-01963-0>
32. Sharma, P.K., Kumar, P. and Ranjan, R.K. "A High-Frequency Flux Controlled Grounded Memristor Emulator", in *2022 14th International conference on information technology and electrical engineering (ICITEE)*, pp. 64-67 (2022) <https://doi.org/10.1109/ICITEE56407.2022.9954099>

33. Ranjan, R.K. Raj, N. Bhuwal, N., et al. "Single DVCCTA based high frequency incremental decremental memristor emulator and its application", *AEU-International Journal of Electronics and Communications*, 82, pp. 177–190 (2017) <https://doi.org/10.1016/j.aeue.2017.07.039>
34. Prasad, S.S. Dutta, S. Choubey, C.K., et al. "Tunable floating and grounded memristor emulator model", *International Journal of Electronics*, 112(1), pp. 1–18 (2023) <https://doi.org/10.1080/00207217.2023.2267218>
35. Gupta, R.K., Choudhry, M.S., Saxena, V., et al. "A Single MOS-Memristor Emulator Circuit". *Circuits Systems and Signal Processing* 43, 54–73 (2024). <https://doi.org/10.1007/s00034-023-02500-5>
36. Petrović, P. and Mijalović, V. "Incremental/decremental memristor utilizing solely a voltage controlled second-generation current conveyor", *Integration*, 105, p. 102528 (2025) <https://doi.org/10.1016/j.vlsi.2025.102528>
37. Petrović, P.B. "Charge-controlled grounded memristor emulator circuits based on Arbel-Goldminz cell with variable switching behaviour", *Analog Integrated Circuits and Signal Processing*, 113(3), pp. 373-81 (2022) <https://doi.org/10.1007/s10470-022-02042-x>
38. Petrović, P. "An Incremental/Decremental Memristor Emulator Realized Using a Voltage-Controlled Second-Generation Current Conveyor (VC-CCII) and Its Application as an Artificial Synaptic Device" *International Journal of Electrical Engineering and Computer Science*, 7, pp.150-158 (2025) <https://doi.org/10.37394/232027.2025.7.16>
39. Kumar, A. and Chaturvedi, B. "Novel CMOS CFDITA and its application as electronically tunable bistable multivibrator", in *International Conference on Signal Processing and Communication (ICSC)*, pp. 374-379, (2016) <https://doi.org/10.1109/ICSPCOM.2016.7980609>
40. Chaturvedi, B. and Kumar, A. "Novel CMOS MO-CFDITA based fully electronically controlled square/triangular wave generator with adjustable duty cycle", *IET Circuits, Devices & Systems*, 12(6), pp. 817-826, (2018) <https://doi.org/10.1049/iet-cds.2017.0553>
41. Rodriguez-Villegas, E. "Low power and low voltage circuit design with the FGMOS transistor", *Institution of Engineering and Technology, London, U.K.*, 20 (2006).
42. Yu, D. Iu, H.H.C. Fitch, A.L., et al. "A Floating Memristor Emulator Based Relaxation Oscillator", in *IEEE Transactions on Circuits and Systems I: Regular Papers*, . 61(10), pp. 2888-2896, (2014) <https://doi.org/10.1109/TCSI.2014.2333687>
43. Babacan, Y., Yesil, A. and Kacar, F. "Memristor emulator with tunable characteristic and its experimental results", *AEU-International Journal of Electronics and Communications*, 81, pp. 99-104 (2017) <https://doi.org/10.1016/j.aeue.2017.07.012>
44. Bhuwal, N. Majumder, M.K. and Gupta, D. "Floating/grounded charged controlled memristor emulator using DVCCTA", *Journal of Computational Electronics*, 23(4), pp. 899-909 (2024) <https://doi.org/10.1007/s10825-024-02176-3>
45. Nune, P. Mandal, S. Saha, A., et al. "A generic simple model of synaptic memristor with local activity for neuromorphic applications", *Journal of Computational Electronics*, 22 (2), pp. 612-25 (2023) <https://doi.org/10.1007/s10825-023-02007-x>
46. Singh, A. and Rai, S.K. "OTA and CDTA-based new memristor-less meminductor emulators and their applications", *Journal of Computational Electronics*, 21(4), pp. 1026-37 (2022) <https://doi.org/10.1007/s10825-022-01889-7>
47. Petrović, P.B. "Electronically adjustable grounded memcapacitor emulator based on single active component with variable switching mechanism" *Electronics*, 11(1), p. 161 (2022) <https://doi.org/10.3390/electronics11010161>
48. Tatovic, M. and Petrovic, P.B. "Single Active Block-Based Emulators for Electronically Controllable Floating Meminductors and Memcapacitors" *Radioengineering*, 32(4), pp. 568-582 (2023) <https://doi.org/10.13164/re.2023.0568>

49. Kumar, A. and Chaturvedi, B. "Fractional Order Mem-Inductor and Mem-Capacitor Mutator using Single DXCCTA" *Indian Journal of Pure & Applied Physics*, 63, pp. 1044-51 (2025)
<https://doi.org/10.56042/ijpap.v63i11.23350>

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- (b) *n*-channel FGMOS

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(a) 5 kHz

(b) 20 kHz

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Figure 22. Output transient waveforms of oscillator at $f = 350 \text{ Hz}$

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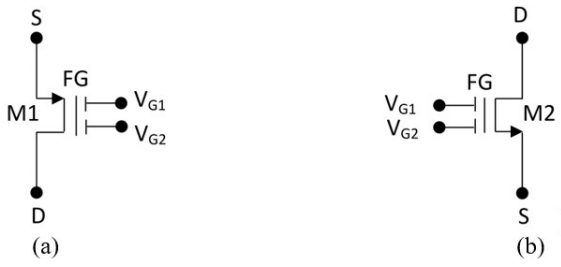


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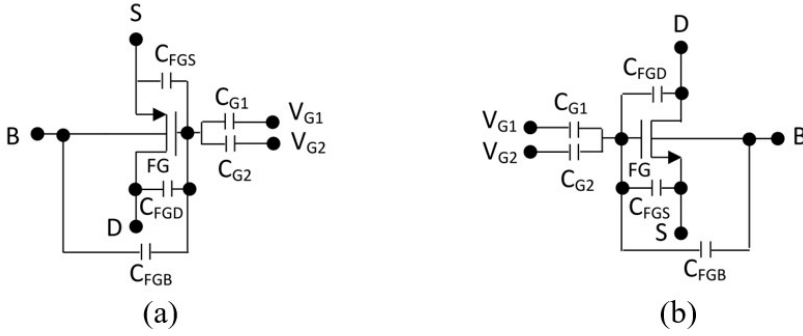


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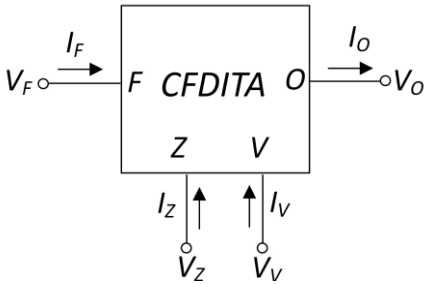


Figure 3. Symbol of CFDITA

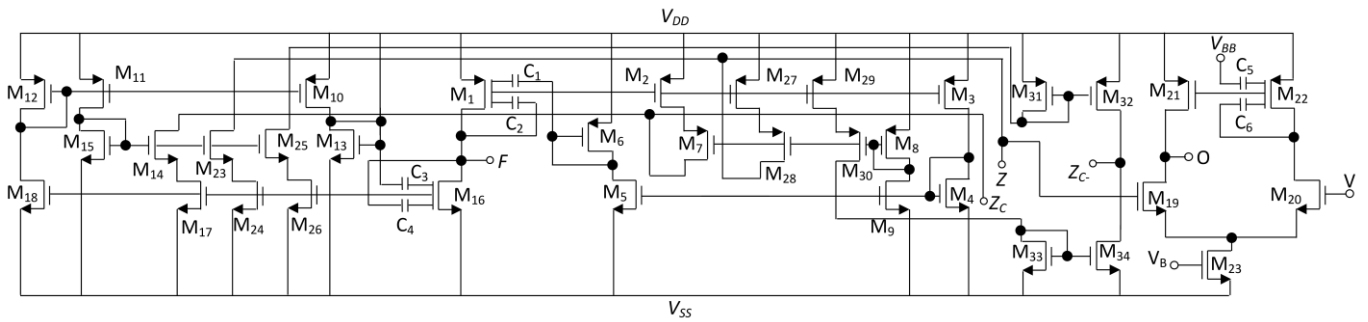


Figure 4. Implementation of FGMOS-based CFDITA

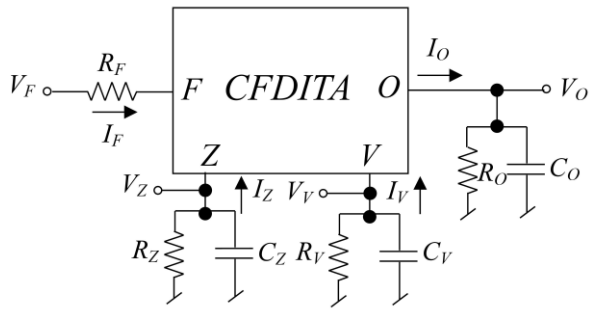


Figure 5. Parasitic of CFDDTA

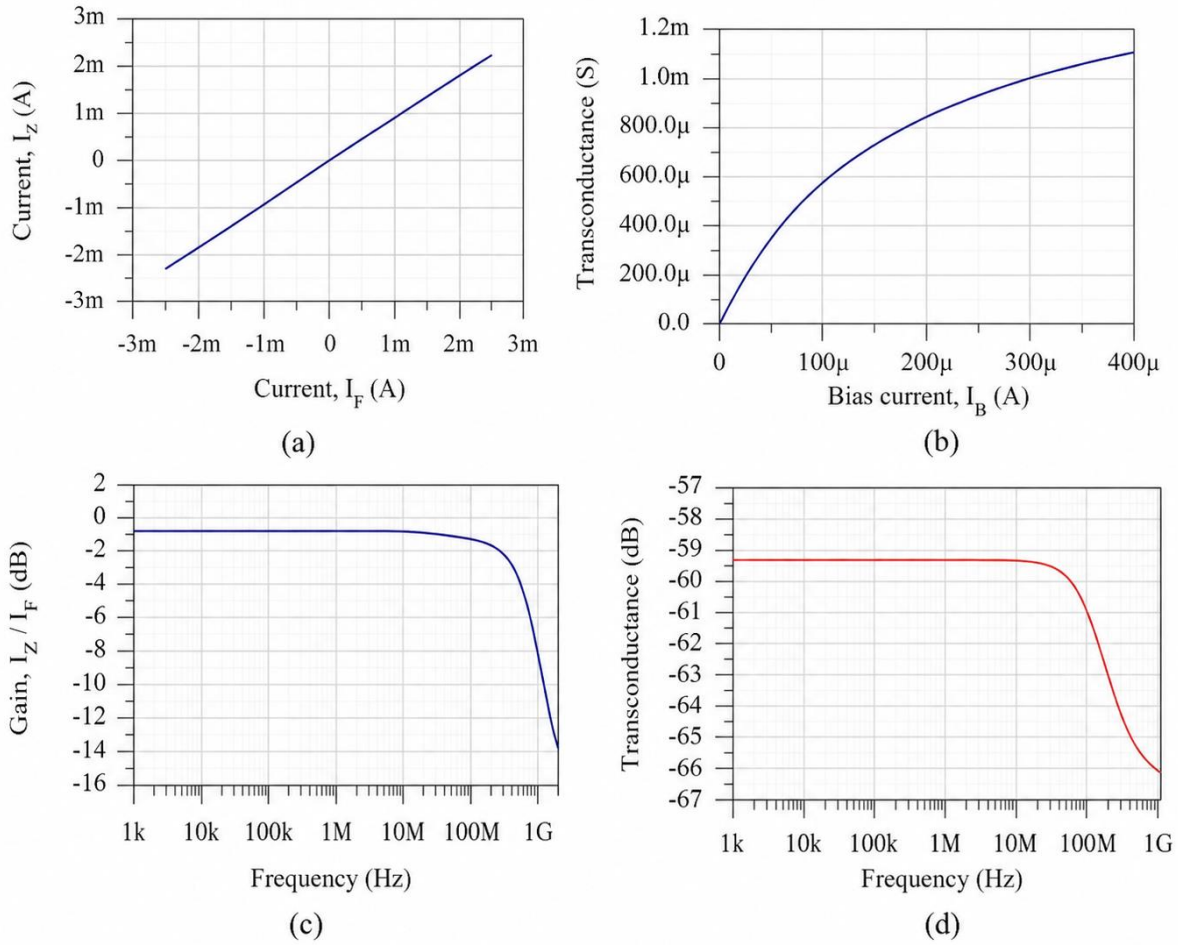


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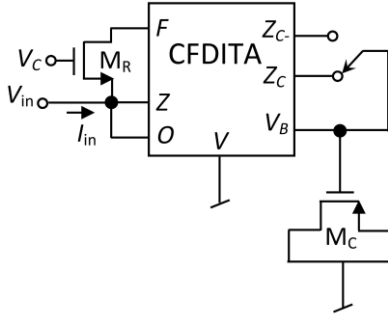


Figure 7. Proposed incremental/decremental grounded memristor emulator

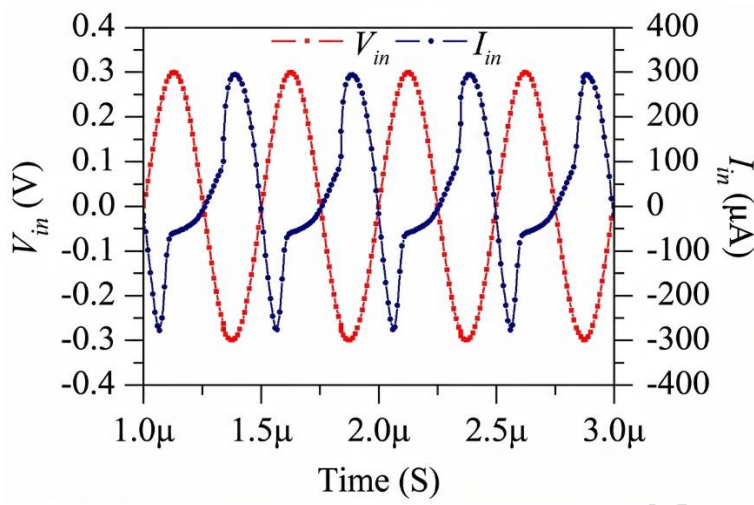


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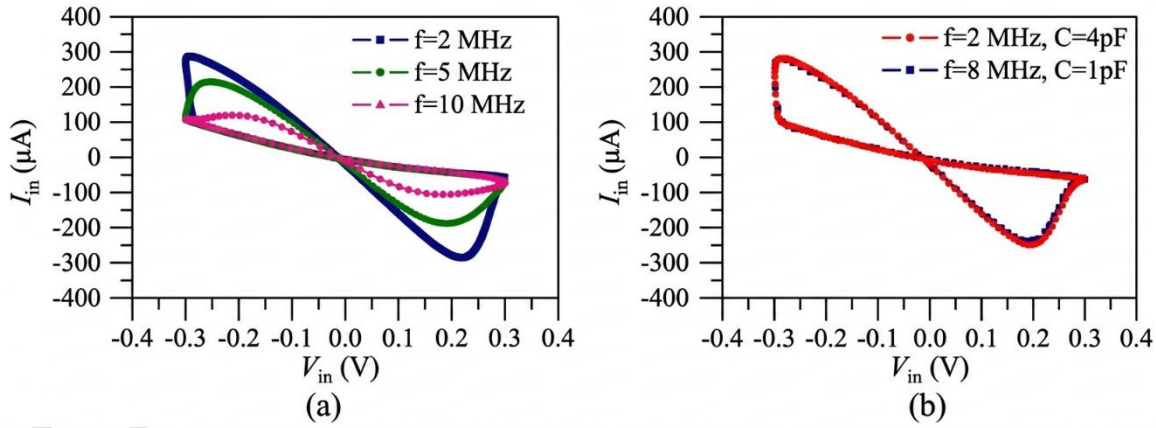


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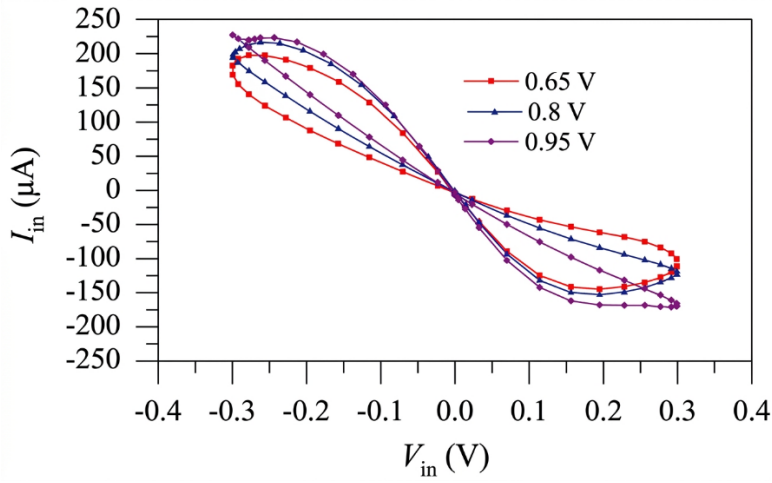


Figure 10. PHLs of the proposed emulator at 5 MHz frequency for different control voltages

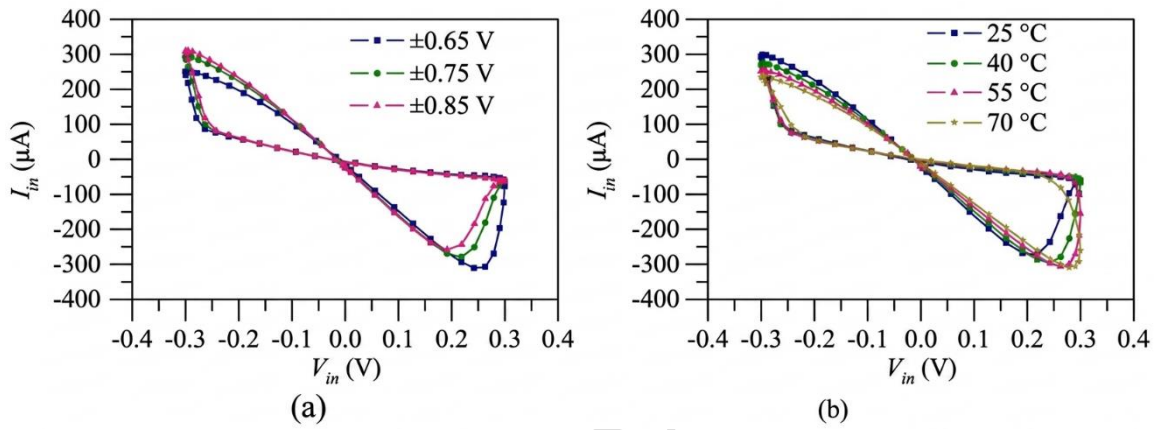


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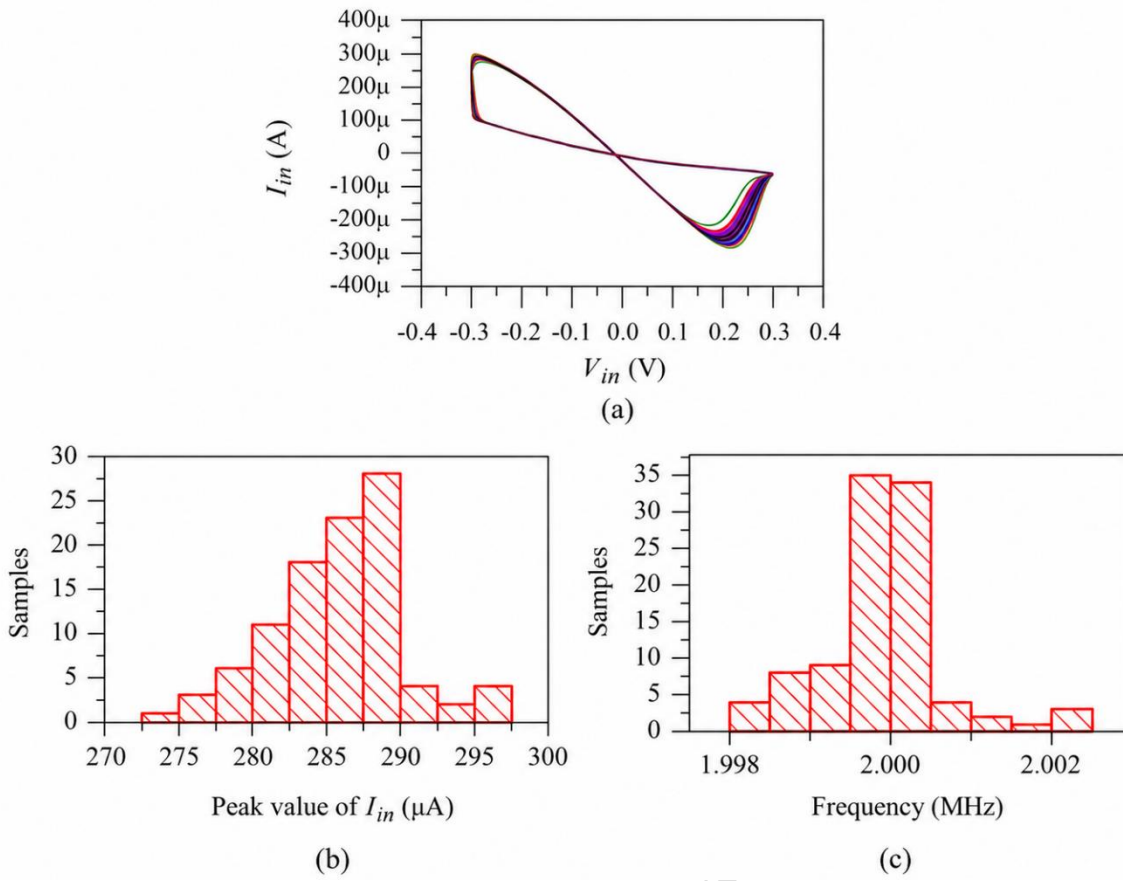


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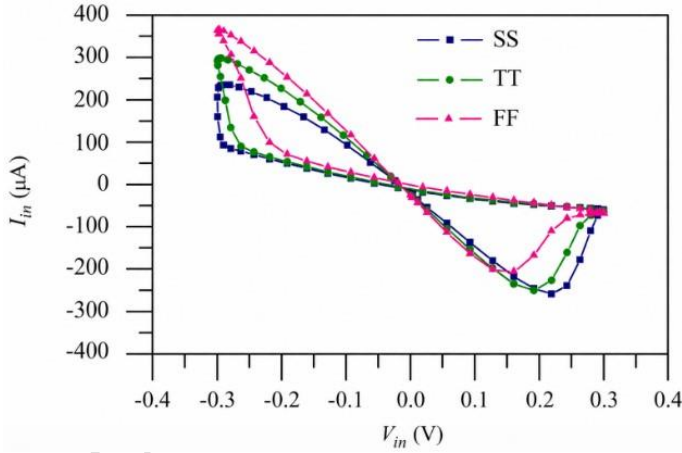


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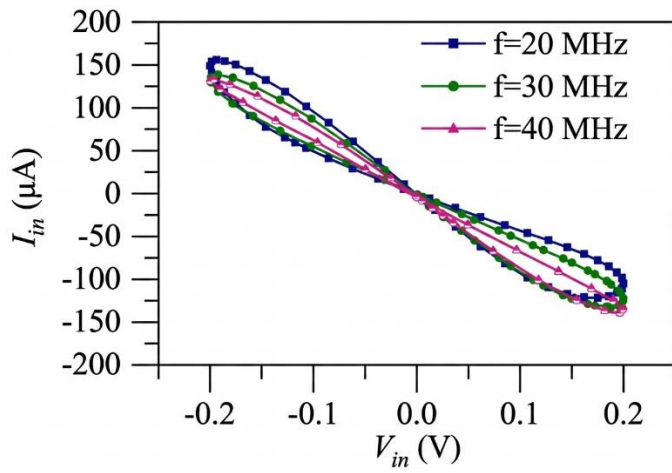


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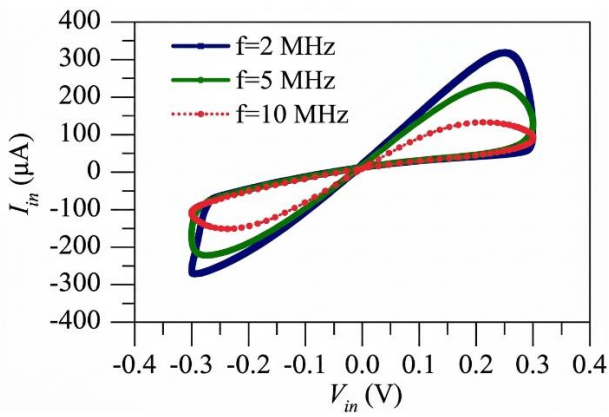


Figure 15. PHLs of the proposed incremental memristor emulator at different frequencies

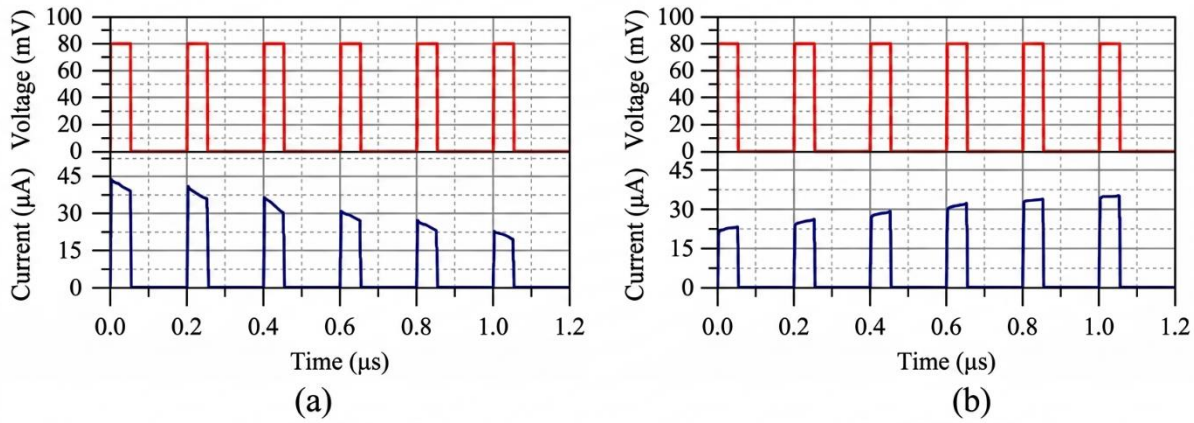


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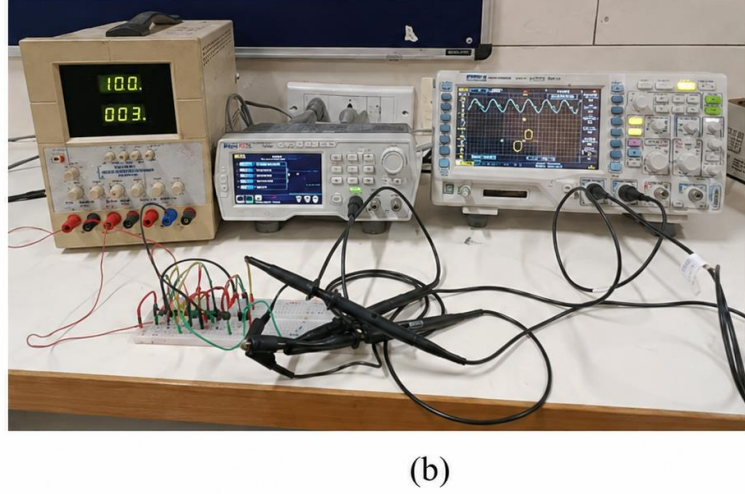
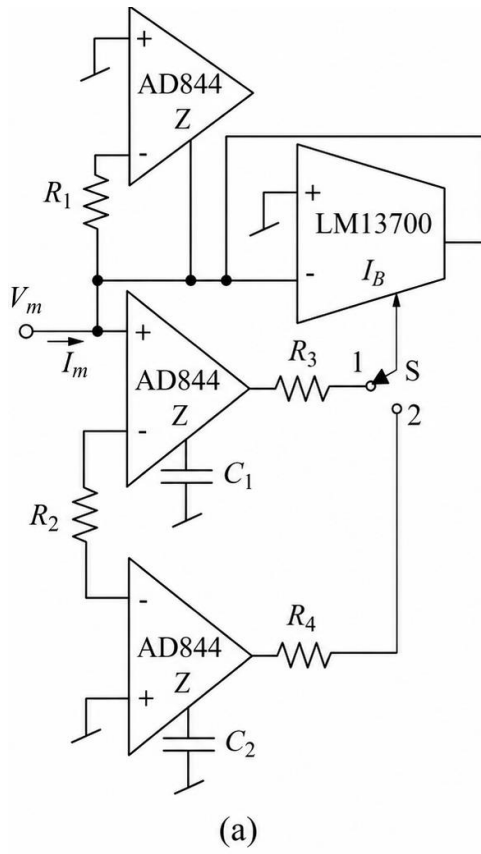


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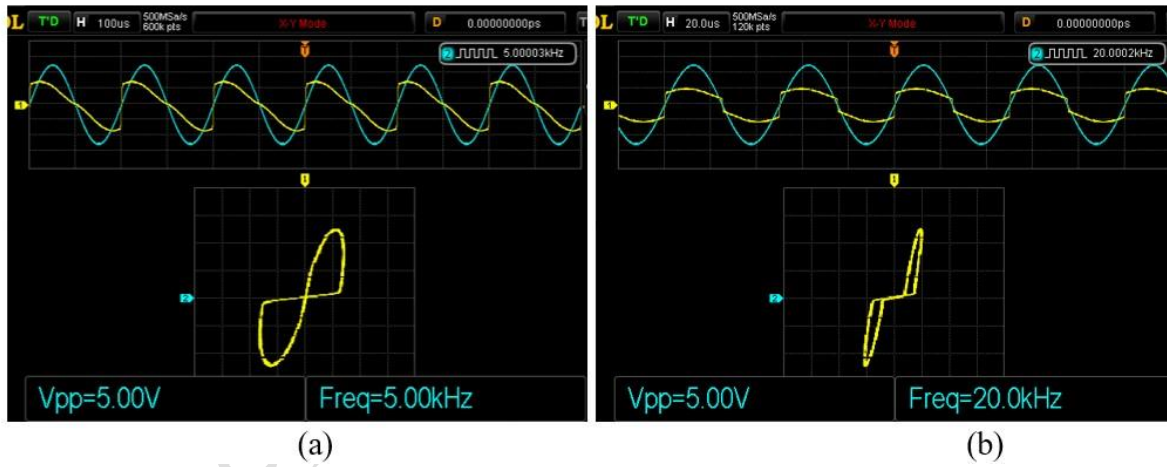


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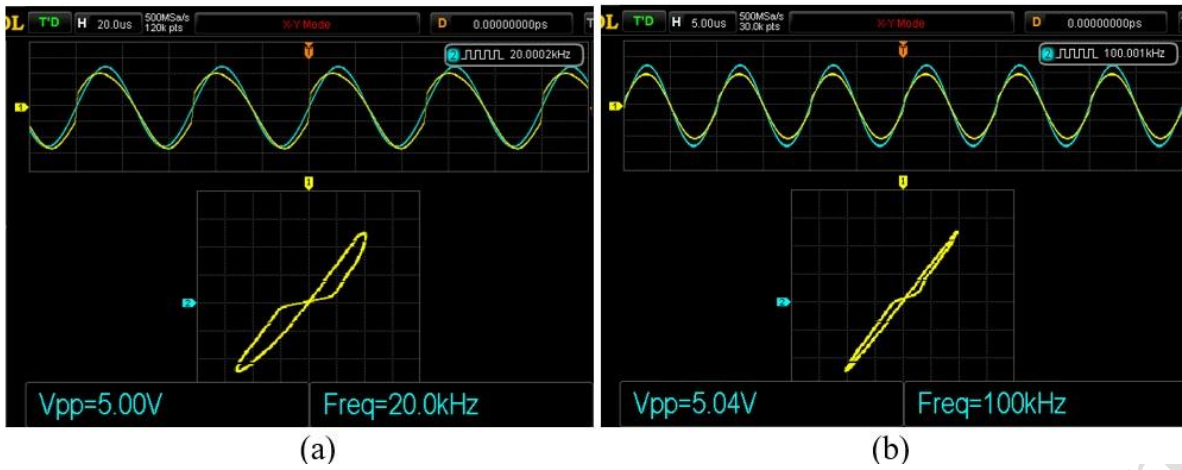


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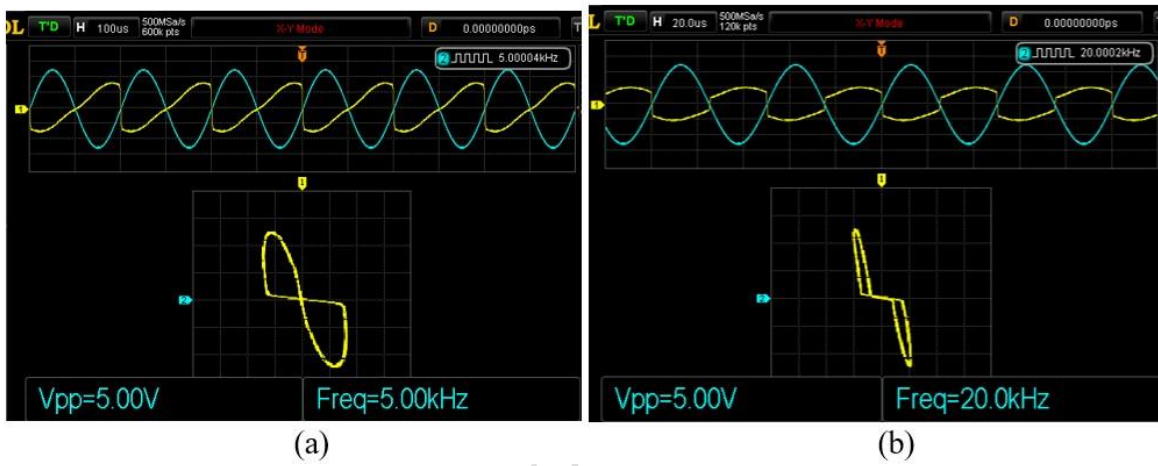


Figure 20. Experimentally observed PHLs of decremental memristor for $C = 1 \text{ nF}$, $R_1 = R_2 = 10 \text{ k}\Omega$ at
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 (b) 20 kHz

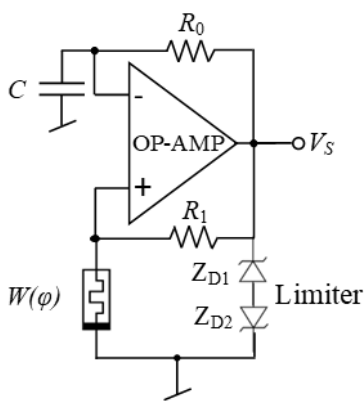


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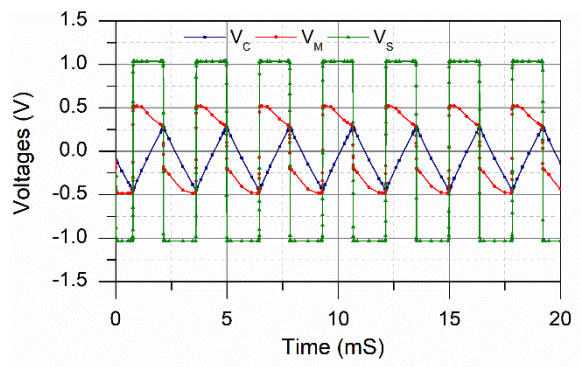


Figure 22. Output transient waveforms of oscillator at $f = 350$ Hz

Tables

Table 1: Performance parameters of the proposed CFDITA

Table 2: Comparison of performance parameters of the proposed FGMOS-CFDITA with other FGMOS-ABBs

Table 3: Comparison among the proposed memristor emulators with existing emulators

Table 1: Performance parameters of the proposed CFDITA

Performance Parameters	Simulated Values
Supply voltages	± 0.75 V
Power dissipation	0.8 mW
Input current dynamic range	-2.5 mA to 2.5 mA
Maximum transconductance for I_O	1.1 mS
3-dB bandwidth for current gain, I_Z / I_F	450 MHz
3-dB bandwidth for transconductance gain, $I_O / (V_V - V_Z)$	162 MHz
Parasitic resistance at F terminal, R_F	168 Ω
Parasitic resistance at Z terminal, R_Z	600 k Ω
Parasitic resistance at V terminal, R_Z	1.00×10^{20} Ω
Parasitic resistance at O terminal, R_O	132 k Ω

Table 2: Comparison of performance parameters of the proposed FGMOS-CFDITA with other FGMOS-ABBs

Reference	[5]	[6]	[7]	[8]	Proposed
ABB	MI-OTA	CDTA	CDTA	OTRA	CFDITA
Supply Voltages	± 1 V	± 1.4 V	± 1 V	± 0.6 V	± 0.75 V
Dynamic Range	-0.6 to 0.6 V	-130 to 130 mA	-78 to 78 μ A	--	-2.5 to 2.5 mA
Power Dissipation	1.47 mW	2.6 mW	1.1 mW	37.3 nW	0.8 mW
Operational 3-dB bandwidth	127 MHz	82 MHz	33 MHz	118 kHz	162 MHz.

Table 3: Comparison among the proposed memristor emulators with existing emulators

Ref.	ABB/count	Resistor(s) and capacitor(s) count	One kind of active element	Floating (F) or grounded (G)	Technology (μm)	Simulation frequency (Hz)	Experimental frequency (Hz)	Supply voltages (V)	Power consumption
[12]	MO-OTA/1	1 C	Yes	F	0.18	1 M	--	± 0.9	--
[13]	VDCC/1, MOS/2	1 C	No	G	0.18	2 M	48 k	$\pm 0.9, \pm 12^*$	--
[14]	CCTA/1, CCII/1	3 R, 1 C	No	F	0.25	5 M	100 k	$\pm 1.5, \pm 10^*$	--
[15]	DO-OTA/2, AM/1	1 R, 1 C	No	F	0.18	180 k	2 k	± 1.5	--
[16]	CCCII/1	1 C	Yes	G	0.18	7.5 M	--	± 0.9	--
[17]	CFTA/1	1 C	Yes	G	0.18	9 M	960 k	$\pm 1.2, \pm 10^*$	--
[18]	VDTA/2	1 R, 1 C	Yes	F	0.18	1.5 M	10 k	$\pm 0.9, \pm 10^*$	--
[19]	OTA/1, MOS/3	2 C	Yes	F	0.18	24	--	± 1.25	--
[20]	CCII/4, AM/1	3 R, 1 C	No	F	--	40 k	500	$\pm 10, \pm 10^*$	--
[21]	VDCC/1, MOS/2	1 C	Yes	G	0.18	2 M	48 k	$\pm 0.9, \pm 12^*$	--
[22]	VDIBA/2	1 C	Yes	G	0.18	12.7 M	820 k	$\pm 1, \pm 10^*$	1.34 mW
[23]	VDCC/1, OTA/1	1 C	No	F	0.18	8 M	100 k	$\pm 0.9, \pm 10^*$	--
[24]	VCLR/1, AM/1 OPAMP/2	5 R, 1 C	No	F	--	150	150	$\pm 10^*$	--
[25]	SG/2, OPAMP/7, AM/2	15 R, 1 C	No	G	--	5 G	1.3 M	$\pm 15^*$	--
[26]	MOS/5	1 C	Yes	F	0.18	66 k	--	--	6.8 μW
[27]	CCCCTA/1	2 R, 1 C	Yes	G	0.18	1 M	700 k	$\pm 1.1, \pm 4.7^*$	2.2 mW
[28]	OTA/1, DVCC/1		No	G	0.18	1 M	--	± 1.2	--
[29]	DTMOS/1, MOS/3	1 C	Yes	F	0.18	3 M	500 k	--	8.24 μW
[30]	OTA/1, CDBA/1	1 C	No	F	0.18	1 M	--	± 0.9	--
[31]	CFDITA/1	1 C	Yes	F	0.18	10 M	100 k	$\pm 1.25, \pm 10^*$	--
[32]	CCII/1, VDIBA/1	1R, 1C	No	G	0.18	25 M	--	± 0.9	2.4 mW
[33]	DVCCTA/1	3R, 1C	Yes	G	0.18	1 M	100 k	$\pm 1.25, \pm 8^*$	--
[34]	DDCCTA/1	2R, 1C	Yes	F	0.18	6 M	58 k	$\pm 0.9, \pm 10^*$	--
[35]	P-MOSFET/1	1R, 1C	Yes	F	0.045	80 M	500 k	0	7.751 pW
[36]	VCCC/1	1R, 1C	Yes	G	0.18	150 M	3 k	$\pm 0.9, \pm 12^*$	2.12 μW
[37]	AG cell-OTA	1 C	Yes	G	0.18	100 M	100 k	$\pm 0.9, \pm 5^*$	0.46 mW
[38]	VCCCII/1	1 C	Yes	G	0.18	150 M	--	± 0.9	2.12 μW
This Work	CFDITA/1	1 R _M , 1 C _M	Yes	G	0.18	40 M	50 k	$\pm 0.75, \pm 10^*$	0.8 mW

Abbreviations: MO-OTA: Multiple-output operational transconductance amplifier; VDCC: voltage differencing current conveyor; CCTA: current conveyor transconductance amplifier; CCII: second-generation current conveyor; DO-OTA: dual-output OTA; AM: analog multiplier; CCCII: current controlled second generation current conveyor; CFTA: current follower transconductance amplifier; VDTA: voltage differencing transconductance amplifier; VDIBA: voltage differencing inverting buffered amplifier; VCLR: voltage controlled linear resistor; OPAMP: operational amplifier; SG: sine wave generator; CC: current conveyor; CCCCTA: current controlled current conveyor transconductance amplifier; DVCC: differential voltage current conveyor; VDTA: voltage differencing transconductance amplifier; DTMOS: dynamic threshold voltage MOSFET; CDBA: current differencing differential amplifier, CF: current follower, DVCCTA: differential voltage current conveyor transconductance amplifier, DDCCTA: differential difference current conveyor transconductance amplifier, P-MOSFET: P-channel metal oxide semiconductor field effect transistor; VCCC: voltage controlled current conveyor; AG cell: Arbel-Goldminz cell; VCCCII: second-generation voltage-controlled current conveyor; * indicates experimental supply voltages.