A Nine-Level Quadratic Boost Common Ground Inverter Topology with Reduced Voltage Stress on Switches

John Britto Pitchai[1]*, Vijayarajan Periyasamy[2]

[1]*Department of Electrical and Electronics Engineering, J.J. College of Engineering and Technology, Tiruchirappalli, India.*
[2]*Department of Electrical and Electronics Engineering, University College of Engineering BIT Campus, Tiruchirappalli, India.*

Abstract

Transformerless multilevel inverters (TMLIs) are emerging as a highly attractive solution for grid-connected solar photovoltaic (PV) systems. However, in TMLIs, leakage current will flow due to the absence of galvanic isolation between the PV DC side and the grid AC side. This article proposes a nine-level transformerless direct ground connection type inverter employing three switched capacitors (SCs) to generate a multilevel output waveform. This single-stage topology delivers a quadratic boost and a multilevel output suitable for grid connection while maintaining a common ground connection to suppress leakage current. Due to the self-balancing nature of the capacitor voltages, the proposed topology does not require sensor monitoring or dedicated control circuits. The voltage stress on utilised semiconductors and SCs is within the output voltage, which reduces the inverter's size and cost. In addition, the lower total standing voltage per unit and capacitor voltage diversity factor are also less than those of the other recent topologies. Further, a detailed comparison is needed to show the merits of the proposed inverter over other recent alternatives, including its leakage current removal and boosting factor. Simulations were conducted at an 895 W output power level using the MATLAB/PLECS tools to assess the practical applicability of the proposed inverter. These simulations were further validated through a laboratory experimental setup and presented with the corresponding results.

Keywords: Common ground; leakage current; multilevel inverter; switched-capacitor; nine-level.

1. Introduction

Driven by rising energy demand and growing environmental awareness, renewable energy sources, particularly solar photovoltaic (PV), have witnessed remarkable growth in recent decades. Power electronics converters play a pivotal role in integrating solar PV systems into the grid [1]. Multilevel inverters have gained prominence for their ability to produce high-

quality output waveforms, reduced harmonic distortion, and improved efficiency compared to traditional two-level inverters. Several multilevel inverter topologies exist, with the most prevalent being the diode-clamped inverter, the flying capacitor (FC), and the cascaded H-bridge (CHB) inverter [2]. Traditionally, a bulky transformer is used in the source or grid side for galvanic isolation between the DC and AC sides. However, the emergence of transformerless inverters has paved the way for new opportunities and challenges in grid-connected PV systems. Without galvanic isolation, transformerless inverters pose the risk of leakage currents flowing between the DC and AC sides. This can have implications for safety and compliance with grid interconnection standards such as VDE 0126-01-01, electromagnetic interference, increased current harmonics, and higher power losses [3]. While existing inverter topologies like DC and AC decoupling topologies [4], [5] and NPC configurations [6], [7] achieve leakage current reduction, complete elimination remains unachievable. Moreover, these solutions often require additional power components with non-boosting capabilities. This necessitates further boost stages in non-boosting inverters for grid-connected solar PV systems, which results in increases in the overall cost and power losses, reduces the efficiency, and also increases complexity. To obtain the voltage-boosting ability, SC-based topologies [8]-[11], and hybrid type (HBT) [12-14] are proposed. However, the leakage current is still present in those topologies. To suppress the leakage current completely, along with voltage boosting ability to support a limited operating voltage range for grid-connected solar PV systems, several SC-based DGT topologies are familiar [15]. The DGT topologies use the same ground point for one terminal of the PV input and the AC ground. This circuit configuration eliminates the high-frequency common mode voltage (CMV) effects and completely suppresses the reduced leakage current compared to non-DGT structures [16]. A few 9L topologies [17]-[22] have been proposed in this family. The topology proposed in [17] uses 11 switches, 2 diodes, and 3 SCs with a boost factor (BF) of 2. Another topology with a boost factor of 2 is proposed in

[18], which uses fewer switches than the topology in [17]. However, the maximum number of conducting switches (Max_{CS}) is high. In [19] and [20], a few other 9L DGT topologies with a BF of 2 are presented with slightly more total power components than the topologies [17] and [18]. In [21], the authors proposed a 9L DGT structure with a BF of 4, at the cost of a very high maximum blocking voltage per unit ($MBV_{p.u.}$) and total standing voltage per unit ($TSV_{p.u.}$). Also, they utilise high-voltage rating capacitors to obtain a quadratic boost. In [22], a 9L-QB with a dynamic voltage boosting topology is presented. However, this is possible with a higher number of power components with high $TSV_{p.u.}$ To address the above shortcomings, such as leakage current suppression and high voltage boost, a nine-level quadratic boost common ground inverter (9L-QB-CG) topology with a reduced number of switches with low voltage stress on switches is proposed. The key features are,

(1) It requires only 10 switches, 3 diodes, and 3 capacitors.

(2) BF is 1:4.

(3) SCs are inherently self-voltage balanced.

(4) Reduced voltage stress on switches, i.e., $v_o/2$.

(5) Lower total standing voltage per unit $TSV_{p.u.}$ i.e., 4.5.

(6) Lower cost function (CF).

(7) Leakage current is completely suppressed due to the DGT configuration.

The remaining sections of the paper are organised as follows. In section 2, the circuit demonstration, description of operating states, and selection of passive components of the proposed 9L-QB inverter are explained in detail. Section 3 details the power loss analysis, followed by a comparative analysis in Section 4 to show the benefits of the proposed inverter with other recent topologies. To verify the feasibility, simulation and experimental results are discussed in Section V. Finally, the article is concluded in Section 5.

2. Proposed Nine-Level Quadratic Boost Inverter Topology

2.1. Circuit Demonstration

The proposed inverter topology is configured using a single source, 10 switches (S_1-S_{10}), three SCs (C_1-C_3), and three diodes (D_1-D_3), as shown in Figure 1(a). It has two units: namely, the source unit and the cross-connected unit. The source unit is formed using a single source, three switches (S_1-S_3), and one SC C_1. The switches S_1 and S_3 in the source unit do not need an anti-parallel diode. The cross-connected unit comprises four switches (S_4-S_7) and two diodes (D_2 and D_3). The voltage across the SCs V_{C1} and V_{C2} is self-balanced at V_{dc}, and the SC V_{C3} is balanced at $2V_{dc,}$ respectively. The proposed inverter topology is capable of generating a nine-level output voltage with a boost factor of 4 at the inverter output terminals by utilising the source voltage and SC voltages (V_{C1}-V_{C3}). The proposed inverter topology can suppress the leakage current to ~0 due to its direct ground connection between the source negative and the grid neutral.

2.2. Description of operation States

The nine-level output voltage waveform of the proposed 9L-QB is generated using the switch sequences given in Table 1. Figure 1(b) to (j) depicts the active switches, capacitor charging and discharging, and load current path while generating nine output voltage waveforms. Each of the nine distinct output voltage levels is described as follows:

2.2.1. State I:

The terminal denoted as '*x*' and the positive terminal '*p*' of the PV source are connected through the SCs C_1 and C_3 and the switches S_2, S_4, S_6, and S_8 to obtain the output voltage of v_o=+4V_{dc}. The SC C_2 is charged to a voltage of V_{dc} because the input source is connected in parallel via *p*-S_2-D_1-*n*, as shown in Figure 1(b).

2.2.2. State II:

The PV source and the SC C_3 are connected in series to generate the output voltage of v_o=+3V_{dc}. As shown in Figure 1(c), the switches S_1, S_4, S_6, and S_8 connect the terminals '*p*' and '*x*'. The SC C_1 is charged to a voltage of V_{dc} because the input source is connected in parallel via *p*-S_1-S_3-*n*.

2.2.3. State III:

In this state, the output voltage v_o=+2V_{dc} is achieved through the series connection of the PV source and the SC C_1. Here, the SCs C_2 and C_3 are charged to V_{dc} and 2V_{dc} via *p*-S_2-D_1-*n* and *p*-S_2-S_4-D_2-D_3-S_5-D_1-*n*, as illustrated in Figure 1(d).

2.2.4. State IV:

The output voltage v_o=+V_{dc} is obtained via the PV source due to the active switches S_1-S_4-S_8. Further, the switches S_3 and S_5 are also switched ON to charge the SCs C_1 and C_3 to V_{dc} and 2V_{dc}, via *p*-S_1-S_3-*n* and *p*-S_1-S_4-D_2-D_3-S_5 as depicted in Figure 1(e).

2.2.5. State V:

During this state, the switches S_5 and S_9 are ON, shorting the terminals '*n*' and '*x*' as shown in Figure 1(f). Since the output terminals are shorted, the output voltage in this state is v_o=0. The SC C_2 is charged to V_{dc} via the *p*-S_2-D_1-*n*, and the other two SCs, as shown in Figure 1(f).

2.2.6. State VI:

This is the first negative voltage level generation state, i.e., v_o=-V_{dc}, achieved due to the discharging of the SC C_2. The switches S_1, S_3, and S_4 are switched ON to charge the SCs C_1 and C_3 to V_{dc} and 2V_{dc}, respectively, via *p*-S_1-S_3-D_1-*n and p*-S_1-S_4-D_2-D_3-S_5 as illustrated in Figure 1(g).

2.2.7. State VII:

In this state, the switches S_5, S_7 and S_9 are switched ON, and thus the negative terminal of the SC C_3 is connected with '*x*'. Hence, the SC C_3 discharges to obtain the load voltage of $v_o=V_{C3}=-2V_{dc}$. The SC C_2 is charged to V_{dc} via p-S_2-D_1-n, as shown in Figure 1(h).

2.2.8. State VIII:

Here, the SCs C_2 and C_3 discharge to generate the output voltage of $v_o= V_{C2}+V_{C3}=-3V_{dc}$. In addition to the active switches S_5, S_7, and S_9 to obtain $-3V_{dc,}$ the switches S_1 and S_3 are also turned ON to charge the SC C_1 to V_{dc}, as shown in Figure 1(i).

2.2.9. State IX:

During this state, all three SCs are discharging to obtain the peak negative voltage of $v_o= V_{C2}+V_{C2}+V_{C3}=-4V_{dc}$. The active switches are S_5, S_7, S_9 and S_{10} as illustrated in Figure 1(j).

Figure 2 shows the maximum blocking voltage ($MBV_{p.u.}$) of switches V_{S1} -V_{S10}, diodes V_{D1}-$V_{D3,}$ and SCs V_{C1}-V_{C3} of the proposed inverter topology. It can be seen that the MBV of eight out of 10 switches is equal to half of the output voltage, i.e. $v_o/2$ or $2V_{dc}$, and the remaining two switches are equal to the input voltage V_{dc}. Using $MBV_{p.u.}$ of switches, the total standing voltage per unit of the proposed inverter topology is calculated in Eq. (1) as follows [24],

$$TSV_{p.u.} = \sum_{X=1}^{10} V_{SX} \Big/ 4V_{dc} = \frac{18V_{dc}}{4V_{dc}} = 4.5 \quad (1)$$

3. Self-Balancing Mechanism and Passive Component Selection (C_1-C_3 and L_f)

The voltage across capacitors has to be balanced to ensure that the output voltage terminals of the inverter generate a constant voltage. The inherent self-voltage balancing capability of SC-based inverter topologies eliminates the need for additional voltage or current sensors, thereby

simplifying the control strategy and minimising both hardware complexity and overall cost [23], [25]. In the proposed 9L-QB topology, the switched capacitors C_1-C_3 achieve self-voltage balancing through a series-parallel configuration, which is one of the key features of the design. As illustrated in Fig. 1(b)-(j), capacitor C_1 is connected in parallel with the input source during the output voltage levels of $\pm V_{dc}$ and $\pm 3V_{dc}$, thereby charging to the input voltage V_{dc}. It discharges when connected in series with the source during the output levels of $+2V_{dc}$ and $\pm 4V_{dc}$. Similarly, capacitor C_2 is connected in parallel with the input source during the output levels 0, $\pm 2V_{dc}$, and $+4V_{dc}$, allowing it to charge to V_{dc}. At $+V_{dc}$, it discharges and, together with C_1, contributes to charging capacitor C_3. At $-V_{dc}$, $-3V_{dc}$, and $-4V_{dc}$, C_2 discharges to generate the corresponding output voltages. Capacitor C_3 is charged to $2V_{dc}$ (i.e., $V_{C1}+V_{C2}$) through the parallel connection involving switches S_4, D_2, D_3, and S_5. As it is connected in series with the source, C_3 discharges during the output levels $-2V_{dc}$, $\pm 3V_{dc}$, and $\pm 4V_{dc}$ to contribute to the output voltage generation. Due to the presence of the load in the discharging path, the effective RC time constant of the discharge loop becomes significantly larger than that of the charging loop. This higher time constant restricts the rapid drop in capacitor voltage during discharge. In the subsequent charging cycle, the capacitors restore their charge, maintaining consistent voltage levels. Consequently, over a complete fundamental period, the voltages of C_1, C_2, and C_3 stabilise at V_{dc}, V_{dc}, and $2V_{dc}$, respectively. Therefore, considering the respective largest continuous maximum discharging time span for the capacitors (MDT), a permissible voltage ripple of 10% [23], and the operating frequency of the inverter structure are all factors that can be considered to achieve this objective. The PWM method and nine-level output voltage waveform of the proposed nine-level inverter topology are shown in Figure 3, and the charging and discharging status of capacitors C_1-C_3 during all nine levels of output voltage (v_o) is listed in Table 1. Considering the MTD for C_1 is t_a to t_b, C_2 is t_b to π-t_b, and C_3 is t_a to π-t_a. From Table 1 and Figure 1(b) to (j), the capacitance of C_1-C_3 is derived as

follows Eq. (2) to Eq. (4),

$$C_1 = \frac{2I_{mx}}{\omega \times \%Ripple \times V_{dc}} \left[\cos(\omega t_a) - \cos(\omega t_b)\right] \quad (2)$$

$$C_2 = \frac{2I_{mx}}{\omega \times \%Ripple \times V_{dc}} \left[\cos(\omega t_b) - \cos(\omega T/4)\right] \quad (3)$$

$$C_3 = \frac{2I_{mx}}{\omega \times \%Ripple \times V_{dc}} \left[\cos(\omega t_a) - \cos(\omega T/4)\right] \quad (4)$$

The current flowing through the filter inductor over a complete cycle can be expressed in Eq. (5),

$$i_{L_f}(t) = i_{L_f}(0) + \frac{1}{L_f} \int_0^t V_{Lf}\, dt \quad (5)$$

From Eq. (4), the inductance of L_f can be derived in Eq. (6),

$$L_f = \frac{1}{f_{sw} \times \Delta i_{L_f}} \left[7V_{mx} \sin \omega t - 12V_{dc} - \frac{V_{mx}^2 \sin^2 \omega t}{V_{dc}}\right] \quad (6)$$

The inductor filter (L_f) value is obtained as given in Eq. (7) by considering the maximum current ripple of an inductor.

$$L_f = \frac{1}{f_{sw} \times \Delta i_{L_f,mx}} \left[7V_{mx} - 12V_{dc} - \frac{V_{mx}^2}{V_{dc}}\right] \quad (7)$$

4. Power Loss Analysis

The total power loss of the proposed 9L-QB topology, which depends on conduction loss, switching loss, and capacitor ripple loss, is calculated in this section.

4.1. Conduction Loss:

The heat dissipation in switching devices and capacitors, known as conduction losses, is determined by factors such as the on-state resistances of the switch ($R_{n,\,S}$), the on-state resistances of the diode ($R_{n,\,D}$), and the equivalent series resistance ($R_{esr,\,C}$). The conduction

losses for the proposed nine-level inverter topology are computed for the output voltage levels using their equivalent circuits, as given in Table 2. Further, the total conduction loss is expressed in Eq. (8),

$$P_{T,C} = P_{C_{+4}} + P_{C_{+3}} + P_{C_{+2}} + P_{C_{+1}} + P_{C_{zero}} + P_{C_{-1}} + P_{C_{-2}} + P_{C_{-3}} + P_{C_{-4}} \tag{8}$$

4.2. Switching Loss:

Switching losses are the losses caused by the switching of semiconducting devices during turn-on and turn-off transitions [20]. Considering energy dissipation during the turn-on and turn-off periods,

$$P_{s,on,k} = \int_0^{T_{on}} V(t)' \; I(t)\, dt = \frac{V_{sw,k}' \; I_k' \; T_{on}}{6} \tag{9}$$

$$P_{s,off,k} = \int_0^{T_{off}} V(t)' \; I(t) dt = \frac{V_{sw,k}' \; I_k' \; T_{off}}{6} \tag{10}$$

where I_k and I'_k are the currents flowing through the k^{th} switch at the time of switching ON and before switching OFF, respectively. $V_{sw,k}$ is the voltage of the switch in the OFF state. Using Eq. (9) and Eq. (10), the total switching loss is estimated using Eq. (11):

$$P_{SW} = \frac{1}{6T} \sum_{k=1}^{10} \left(\sum_{i=1}^{N_{on}} P_{s,on,k,i} + \sum_{i=1}^{N_{off}} P_{s,off,k,i} \right) \tag{11}$$

where N_{on} and N_{off} denote the number of turns ON and turned OFF during one fundamental cycle.

4.2. Ripple Loss:

The ripple loss in the capacitor during its cyclic charging and discharging due to the variation of its voltages is expressed as [26],

$$P_{RIP} = f_o \left(\sum_{x=1}^{3} C_x' \; \Delta V_{Cx} \right) \tag{12}$$

The total loss can be computed through Eq. (8) to Eq. (12) as Eq. (13),

$$P_{Loss} = P_{T,C} + P_{SW} + P_{RIP} \quad (13)$$

The efficiency is calculated as Eq. (14),

$$\eta = P_o / (P_o + P_{Loss}) \quad (14)$$

5. Comparative Analysis

A comparative analysis to showcase the benefits of the proposed inverter with other single-source nine-level topologies that have recently been published is presented in this section. The following metrics, as given in Table 3, have been taken into consideration for the comparison: the number of switches, gate drivers, diodes, capacitors, inductors (N_S, N_G, N_D, N_C, N_L), boost factor (*BF*), the ratio of level to the number of semiconductors (*LSC*), the ratio of number of switches to levels (*SPL*), maximum blocking voltage per unit ($MBV_{p.u.}$), total standing voltage per unit ($TSV_{p.u.}$), cost factor (*CF*), maximum conducting switches (Max_{CS}), leakage current (*LC*), self-balancing ability of capacitors (C_{SBA}), capacitor voltage diversity factor (*CVDF*), maximum voltage stress of capacitor (*MVSC*), efficiency (η). Table 3 is divided into four categories: switched capacitor-based (*SCB*) topologies [8]-[11], and hybrid type (*HBT*) topologies [12]-[14], active neutral-point clamped (*ANPC*) topology [7], and direct ground type topologies [17]-[22]. Further, *CF* is calculated [25] using Eq. (15) given below,

$$CF = N_S + N_G + N_D + N_C + N_L + \left\lceil \alpha \times TSV_{p.u.} \right\rceil \quad (15)$$

where α is the balancing factor.

5.1 In terms of N_s, LSC and BF:

To attain inverters with increased voltage levels using a reduced number of components, various inverter topologies have been proposed, as listed in Table 3. It is evident that the proposed nine-level inverter topology requires fewer N_S than the topologies [8], [9], [11], [12],

[14], [17], [20], [22]. Although the topologies [7], [19], [21], along with the proposed nine-level inverter topology, use the same N_S, the former have a *BF* of 2, except for topologies [21] and the proposed topology, which has a *BF* of 4. While the topology [13] employs a slightly lower N_S than the proposed topology, it is worth noting that their *BF* is only 2, in contrast to the proposed topology, which has a *BF* of 4.

5.2 In terms of $MBV_{p.u.}$, $TSV_{p.u.}$ and Max_{CS}:

Within the DGT family, the $MBV_{p.u}$ of [17], [20] align with their output voltage at $2V_{dc}$. In contrast, the proposed topology and those in [19], [22] have an $MBV_{p.u.}$ equivalent to half of the output voltage. Meanwhile, the $MBV_{p.u.}$ for the topology introduced in [21] is twice the output voltage. Moving to the *TSVp.u.*, the proposed topology and the ANPC type topology from [7] have a lower value than all other considered topologies. In terms of Max_{CS}, the proposed topology ranks as the second lowest in the comparison table.

5.3 In terms of CF and CVDF:

Utilising equation (1), the calculation of the *CF* for all topologies has been conducted, considering balancing factors α=0.5 and α=1, as listed in Table 3. For both α values, it is observed that the *CF* of the proposed topology is the lowest among the DGT family of topologies, except [18]. However, it's noteworthy that despite its superior *CF* at α=0.5 and lower N_s, the proposed topology exhibits lesser $TSV_{p.u.}$ in comparison to [18]. Even though the *CF* of topology [13] is lower than that of the proposed topology, it's crucial to consider that their BF and $TSV_{p.u.}$ are the drawbacks in comparison. The proposed topology, on the other hand, excels in maintaining a favourable *CF* while managing a higher *BF* and the least $TSV_{p.u.}$ than some of its counterparts. By decreasing the voltage rating of the capacitors and N_C, the cost and size of the inverter may be significantly reduced.

Considering this, *CVDF* for '*n*' number of capacitors is calculated using Eq. (16) given below,

$$CVDF = \frac{\sum_{x=1}^{n} V_{Cx}}{v_{o,mx}} \quad (16)$$

Except for [18] and [21], the *CVDF* of all other topologies in the DGT family is lower. Similarly, [8]-[11] from the SCB topologies and [13] from the HBT topologies, the *CVDF* is low.

5.4 Leakage current:

The topologies [8]-[11], suggested in SCB and [12], [13] in *HBT*, exhibit a significant LC value as a result of their topological configuration or used PWM. Consequently, these topologies are unsuitable for connecting the solar PV system with the utility grid. Even while the ANPC structure [7] and the topology [14] can decrease *LC*, it should be noted that they do not suppress it completely. Topologies in DGT [17]-[22], and the proposed topology can suppress the LC completely due to the direct connection between the source and the grid neutral. However, the topologies [17]-[20] have the *BF* of 2, which is significantly lower than the proposed topology and those in [21], [22]. The proposed topology shows better characteristics in terms of the $MBV_{p.u.}$, $TSV_{p.u.}$, *CF*, and *CVDF* when compared with [21]. Furthermore, compared to [22], the proposed topology excels in terms of fewer N_S, less $TSV_{p.u.}$, and reduced *CF*. According to the findings of the comparative study, it can be concluded that the suggested topology, which has a reduced number of N_S, a four-fold *BF*, the lowest $TSV_{p.u.}$, a lowered Max_{CS} and *CF*, better *CVDF*, and the ability to suppress *LC*, is a more feasible alternative for a grid-connected solar PV system.

6. Result and Discussion

6.1 Simulation results

The proposed 9L-QB was simulated in MATLAB/Simulink ™ and PLEXIM simulation tools,

and the respective results are presented in this section. The simulation parameters are listed in Table 4.

Figure 4 shows the inverter output voltage (v_o), grid voltage (v_g), current (i_g), and current stress (i_{C1}-i_{C3}) of SCs C_1-C_3 while injecting a grid current of ~4A. It is seen that nine levels of output voltage with four-fold, i.e., 400 V, are achieved at unity power factor condition (UPF) while the input is 100 V. The operation of the proposed topology is further tested with 0.62 lagging and leading power factors, and the respective inverter output voltage (v_o), along with grid voltage (v_g), and current (i_g), are illustrated in Figure 5. Further to verify the performance during the dynamic operating condition, the reference current is boosted from 4 A to 5.5 A, and the respective waveforms are depicted in Figure 6. Further, to check the self-balancing ability, the input is varied from 90 V to 100 V, and the respective results are shown in Figure 7. It is seen that the SCs C_1 and C_2 are balanced at ~100 V, and the SC C_3 is balanced at ~200 V.

6.2 Experimental results

To assess the practicality of the suggested 9L-QB topology, a scaled-down prototype of 895 W has been developed, as shown in Figure 8(a), and various examinations have been carried out. The closed-loop control scheme for the grid-connected operation is done using a proportional-resonant (*PR*) current controller and a proportional-integral (*PI*) voltage controller, as depicted in Figure 8(b). The controller TI Launchpad TMS 320F28379D has been used to control the proposed inverter topology. The experimental results are obtained for the input voltage of V_{dc}=100 V, RMS value of the grid voltage v_g=230 V, SCs and filter inductor (L_f) values as per Eqns (2)-(4) and (7) as C_1=1100 μF, C_2=2700 μF, C_3=3300 μF, and L_f=6.8 mH.

Figure 9(a) shows the inverter output voltage (v_o), the voltage across the SCs (V_{C1}, V_{C2} and

V_{C3}). It shows that the inverter generates a 9L voltage during steady-state operation with UPF, with a maximum value of 400V, with each level increasing by 100V. The SCs V_{C1}/V_{C2} and V_{C3} are balanced at 100 V and 200 V, respectively. Figure 9(b) shows the result of varying the input voltage (V_{dc}) from 90 V to 100 V, as well as the voltages of the SCs (V_{C1}-V_{C3}) and the output voltage (v_o). As the input voltage is varied, the voltages of the SCs (V_{C1}/ V_{C2} and V_{C3}) remain balanced at ~100 V and ~200 V. Figure 9(c) shows the experimental results while injecting an active power of ~ 891 W. The reactive power handling ability of the proposed topology is tested, and the respective results of 0.62 lag and 0.62 lead pf conditions are depicted in Figure 9(d and e). The dynamic behaviour of the inverter topology is then verified by varying the reference current ($i_{g,\,ref}$) between 2.5 A to 5.5 A and the respective results, such as grid voltage (v_g) and the injected current (i_g), along with the capacitor voltage ripple of SCs (V_{C1}-V_{C3}), are depicted in Figures (f) and (g). The experimental results of the capacitor current stress (i_{C1}-i_{C3}) waveform, MBV (V_{S1}-V_{S10}), and switch current stress (i_{S1}-i_{S10}) waveforms are depicted in Figure 10(a to f). The thermal model of the proposed 9L-QB topology is simulated in the PLECS simulation tool to determine the power loss distribution of the employed semiconductor devices, and the corresponding results are depicted in Figure 11(a). Further, Figure 11(b) shows the efficiency for different output powers. It can be seen that the maximum measured efficiency is ~96.4% at an output power of 200 W, whereas it is ~94.3% for the rated power.

7. Conclusion

A nine-level quadratic boost transformerless direct ground connection type inverter is proposed in this article. Since both the PV side negative terminal and the grid side neutral are connected to the same ground point, the leakage current is suppressed completely. It uses three SCs with self-voltage balancing to generate a nine-level output voltage waveform. The circuit demonstration, all the operation states, and the selection of utilised passive components were

explained. The obtained results confirm that the maximum blocking voltage of the switches is within the output voltage, i.e., $v_o/2$, and the total standing voltage is less than that of other recent counterparts. Different 9L MLIs are compared with the proposed 9L-QB inverter in terms of quantitative, $MBV_{p.u.}$, $TSV_{p.u.}$, BF, etc., and are analysed. The simulation and experimental results, such as steady state, input change, reference current change, etc., validated the performance and feasibility of the proposed topology under different power factor conditions. The measured efficiency of 96.4 % is obtained, close to its simulation efficiency of 97.6% at ~200 W. The distinctive attributes, including higher voltage levels with high voltage boosting, self-balancing of SCs, and direct ground connection configuration, position the proposed 9L-QB topology as a highly competitive choice for a grid-connected solar PV system.

Disclosure statement

No potential conflict of interest was reported by the author(s).

References

1. Kibria, M. F., Ahmad, M., Hossain, M. A., et al. "A Hybrid Single-Phase Transformerless Solar Photovoltaic Grid-Connected Inverter With Reactive Power Capability and Reduced Leakage Current", *IEEE Access.*, **13**, 39235–39247(2025). https://doi.org/10.1109/ACCESS.2025.3546670
2. Anand, V., & Singh, V. "A 13-Level Switched-Capacitor Multilevel Inverter With Single DC Source", *IEEE J. Emerg. Sel. Topics Power Electron.*, **10**(2), pp. 1575–1586 (2022). https://doi.org/10.1109/JESTPE.2021.3077604
3. Anand, V., Singh, V., & Mohamed Ali, J.S. "Dual Boost Five-Level Switched-Capacitor Inverter With Common Ground", *IEEE Trans. Circuits Syst. II, Exp. Briefs.*, **70**(2), pp. 556–560 (2023). https://doi.org/10.1109/TCSII.2022.3169009
4. Cedieu, S., Grigoletto, F. B., Lee, S. S., et al. "A Five-Level Common-Ground Inverter With Reduced Switch Count for Transformerless Grid-Tied PV Applications", *IEEE Trans. Ind. Appl.*, **60**(5), 7061–7075 (2024). https://doi.org/10.1109/TIA.2024.3412051
5. Shahabadini, M., Moeini, N., Bahrami-Fard, M., et al. "HERIC-Based Cascaded H-Bridge Inverter for Leakage Current Suppression in PV Systems", *IEEE Trans. Power Electron.*, **38**(3), pp. 4005–4014 (2023). https://doi.org/10.1109/TPEL.2022.3218634
6. Sathik M, J., Siddique, M. D., Sandeep, N., et al. "1ϕ-Dual Boost ANPC Type Inverter Topology with High Voltage Gain", *IEEE Trans. Ind. Appl.*, **60**(2), pp. 1–9 (2024). https://doi.org/10.1109/TIA.2024.3350011
7. Mohamed Ali, J. S. "A Nine-Level ANPC Boost Type Inverter Topology With Reduced Component Stress", *IEEE Trans. Circuits Syst. II, Exp. Briefs.*, **71**(1), pp. 380–384 (2023). https://doi.org/10.1109/TCSII.2023.3305230
8. Siddique, M. D., Karim, M. F., Mekhilef, S., et al. "Single-Phase Boost Switched-Capacitor-Based Multilevel Inverter Topology With Reduced Switching Devices", *IEEE J. Emerg. Sel. Topics Power Electron.*, **10**(4), pp. 4336–4346 (2022). https://doi.org/10.1109/JESTPE.2021.3129063

9. Islam, S., Siddique, M. D., Iqbal, A., et al. “A 9- and 13-Level Switched-Capacitor-Based Multilevel Inverter With Enhanced Self-Balanced Capacitor Voltage Capability”, *IEEE J. Emerg. Sel. Topics Power Electron.*, **10**(6), pp. 7225–7237 (2022). https://doi.org/10.1109/JESTPE.2022.3179439
10. Varesi, K., Esmaeili, F., & Deliri, S. “Single-Input Quadruple-Boosting Switched-Capacitor Nine-Level Inverter With Self-Balanced Capacitors”, *IEEE Access*, **10**, pp. 70350–70361 (2022). https://doi.org/10.1109/ACCESS.2022.3187005
11. Siddique, M. D., Mekhilef, S., Shah, et al. “A New Single Phase Single Switched-Capacitor Based Nine-Level Boost Inverter Topology with Reduced Switch Count and Voltage Stress”, *IEEE Access*, **7**, pp. 174178–174188 (2019). https://doi.org/10.1109/ACCESS.2019.2957180
12. Sandeep, N., & Yaragatti, U. R. “Operation and Control of an Improved Hybrid Nine-Level Inverter”, *IEEE Trans. Ind. Appl.*, **53**(6), pp. 5676–5686 (2017). https://doi.org/10.1109/TIA.2017.2737406
13. Lin, W., Zeng, J., Hu, J., et al. “Hybrid Nine-Level Boost Inverter with Simplified Control and Reduced Active Devices”, *IEEE J. Emerg. Sel. Topics Power Electron.*, **9**(2), pp. 2038–2050 (2021). https://doi.org/10.1109/JESTPE.2020.2983205
14. Dhara, S., & Somasekhar, V. T. “A Nine-Level Transformerless Boost Inverter With Leakage Current Reduction and Fractional Direct Power Transfer Capability for PV Applications”, *IEEE J. Emerg. Sel. Topics Power Electron.*, **10**(6), pp. 7938–7949 (2022). https://doi.org/10.1109/JESTPE.2021.3074701
15. Anand, V., Singh, V., Sathik, J., et al. “Single-stage Five-level Common Ground Transformerless Inverter with Extendable Structure for Centralized Photovoltaics”, *CSEE J. Power Energy Syst.*, **9**(1), pp. 37–49 (2023). https://doi.org/10.17775/CSEEJPES.2022.02700
16. Sandeep, N., Sathik, M. J., Yaragatti, U. R., et al. “Common-Ground-Type Five-Level Transformerless Inverter Topology with Full DC-Bus Utilization”, *IEEE Trans. Ind. Appl.*, **56**(4), pp. 4071–4080 (2020). https://doi.org/10.1109/TIA.2020.2996152
17. Gopinath, N. P., & Vijayakumar, K. “*Common Ground Nine-Level Boost Inverter for Grid-Connected PV Applications”*, *Front. Energy Res.*, **10**, 922786 (2022). https://doi.org/10.3389/fenrg.2022.922786
18. Jakhar, A., Sandeep, N., & Verma, A. K. “A Nine-Level Common-Ground-Type Boost Inverter for PV Applications”, *IEEE J. Emerg. Sel. Topics Power Electron.*, **5**(3), 1080–1088 (2024). https://doi.org/10.1109/JESTIE.2023.3307000
19. Almakhles, D. J. & Sathik, M. J. “Single-phase transformerless nine-level inverter with voltage boosting ability for PV-fed AC microgrid applications”, *Sci. Rep.* **12**, pp. 13442 (2022). https://doi.org/10.1038/s41598-022-16057-x
20. Sarwer, Z., Anwar, M. N., & Sarwar, A. “A nine-level common ground multilevel inverter (9L-CGMLI) with reduced components and boosting ability”, *Int. J. Circuit Theory Appl.*, **51**(8), pp. 3826–3840 (2023). https://doi.org/10.1002/cta.3550
21. Srivastava, A., & Seshadrinath, J. “Design and Implementation of a New Nine-Level Boost Inverter for Transformerless Grid-Tied PV Application”, *IEEE Trans. Energy Convers.*, **38**(4), pp. 2298–2309 (2023). https://doi.org/10.1109/TEC.2023.3292147
22. Gopinath, N. P., & Vijayakumar, K. “Dual-ground transformerless nine-level dynamic voltage boosting inverter topology”, *Int. J. Electron.*, **111**(4), pp. 677-696 (2023). https://doi.org/10.1080/00207217.2023.2173808
23. Mohamed Ali, J. S., Gopinath N.P., Hota, A., et al. “Improved Dual Boost Mid-Point Clamped Five-Level Inverter Topology”, *IEEE Trans. Circuits Syst. II, Exp. Briefs.*, **71**(6), pp. 3221-3225 (2024). https://doi.org/10.1109/TCSII.2024.3356171
24. Mohamed Ali, J. S., Almakhles, D. J., & Elmorshedy, M.F. “High Boost Seventeen-Level Switched Capacitor Inverter Topology With Continuous Input Current”, *IEEE J. Emerg. Sel. Topics Power Electron.*, **11**(3), 2742–2754 (2023). https://doi.org/10.1109/JESTPE.2022.3230047
25. Anand, V., Singh, V., & Dwivedi, R. “Seventeen Level Switched Capacitor Inverters with the Capability of High Voltage Gain and Low Inrush Current”, *IEEE J. Emerg. Sel. Top. Ind. Electron.*, **4**(4), 1138–1150 (2023). https://doi.org/10.1109/JESTIE.2023.3291996
26. Gopinath, N. P., Azhagumurugan, R., Sathik, M. J., et al. “Low Cost and Compact Six Switch Seven Level Grid Tied Transformerless PV Inverter”, *Sci. Rep.*, **15**, 8841(2025). https://doi.org/10.1038/s41598-025-89848-7

Figure Captions

Figure 1. (a) Proposed 9L-QB topology, (b)-(j) Output voltage levels from $+4V_{dc}$ to $-4V_{dc}$.

Figure 2. Maximum blocking voltage of switches and diodes, and capacitor voltage details of the proposed 9L-QB topology.

Figure 3. Modulation method along with capacitor voltage and nine-level output voltage waveforms of the proposed direct ground type inverter topology.

Figure 4. Simulation results of the proposed 9L-QB topology at UPF.

Figure 5. Simulation results of proposed 9L-QB topology at (a) 0.62 Lead PF, and (b) 0.62 Lag PF.

Figure 6. Simulation waveforms of the proposed 9L-QB topology when the reference grid current ($i_{g,\,ref}$) is changed from 4 A to 5.5 A.

Figure 7. Simulation waveforms of the proposed 9L-QB topology when the input voltage (V_{dc}) is changed from 90 V to 100 V.

Figure 8. (a) Experimental setup and (b) Closed-loop control scheme of 9L-QB topology.

Figure 9. Experimental results. (a) v_o (350 V/div), V_{C1}, V_{C2} (10 V/div), and V_{C3} (20 V/div) at UPF, (b) v_o (350 V/div), V_{C1}, V_{C2} (10 V/div), and V_{C3} (20 V/div) when input is changed from 90 V to 100 V at UPF, (c)-(e) V_{dc} (100 V/div), v_o (500 V/div), v_g (300 V/div), and i_g (5 A/div) at UPF, 0.62 Lag PF, 0.62 Lead PF, (f) v_g (300 V/div), i_g (6 A/div), V_{C1}, and V_{C2} (10 V/div) when i_{ref} changed from 2.5 A to 5.5 A at UPF, (g) v_g (300 V/div), i_g (6 A/div), and V_{C3} (10 V/div) when i_{ref} changed from 2.5 A to 5.5 A at UPF.

Figure 10. Experimental results at 895 W output power. (a) Capacitor current stress i_{C1}, i_{C2}, and i_{C3} (20 A/div), (b) Switch voltage and current stress V_{S1} (100 V/div), i_{S1} (20 A/div), V_{S3} (100 V/div), and i_{S3} (20 A/div), (c) Switch voltage and current stress V_{S2} (200 V/div), i_{S2} (20 A/div), V_{S10} (200 V/div), and i_{S10} (10 A/div), (d) Switch voltage and current stress V_{S4} (200 V/div), i_{S4} (20 A/div), V_{S5} (200 V/div), and i_{S5} (20 A/div), (e) Switch voltage and current stress V_{S6} (200 V/div), i_{S6} (5 A/div), V_{S7} (200 V/div), and i_{S7} (5 A/div), (f) Switch voltage and current stress V_{S8} (200 V/div), i_{S8} (5 A/div), V_{S9} (200 V/div), and i_{S9} (5 A/div).

Figure 11. Power loss analysis with (a) PLECS loss breakdown of semiconductors, (b) Efficiency curve for various output power.

Table Captions

Table 1. Switching Sequence of 9L-QB

Table 2. Expression for conduction loss equations for 9L-QB topology

Table 3. Comparative analysis of the proposed single nine-level inverter topology

Table 4. Parameters for 9L-QB Inverter

List of Figures with Figure number

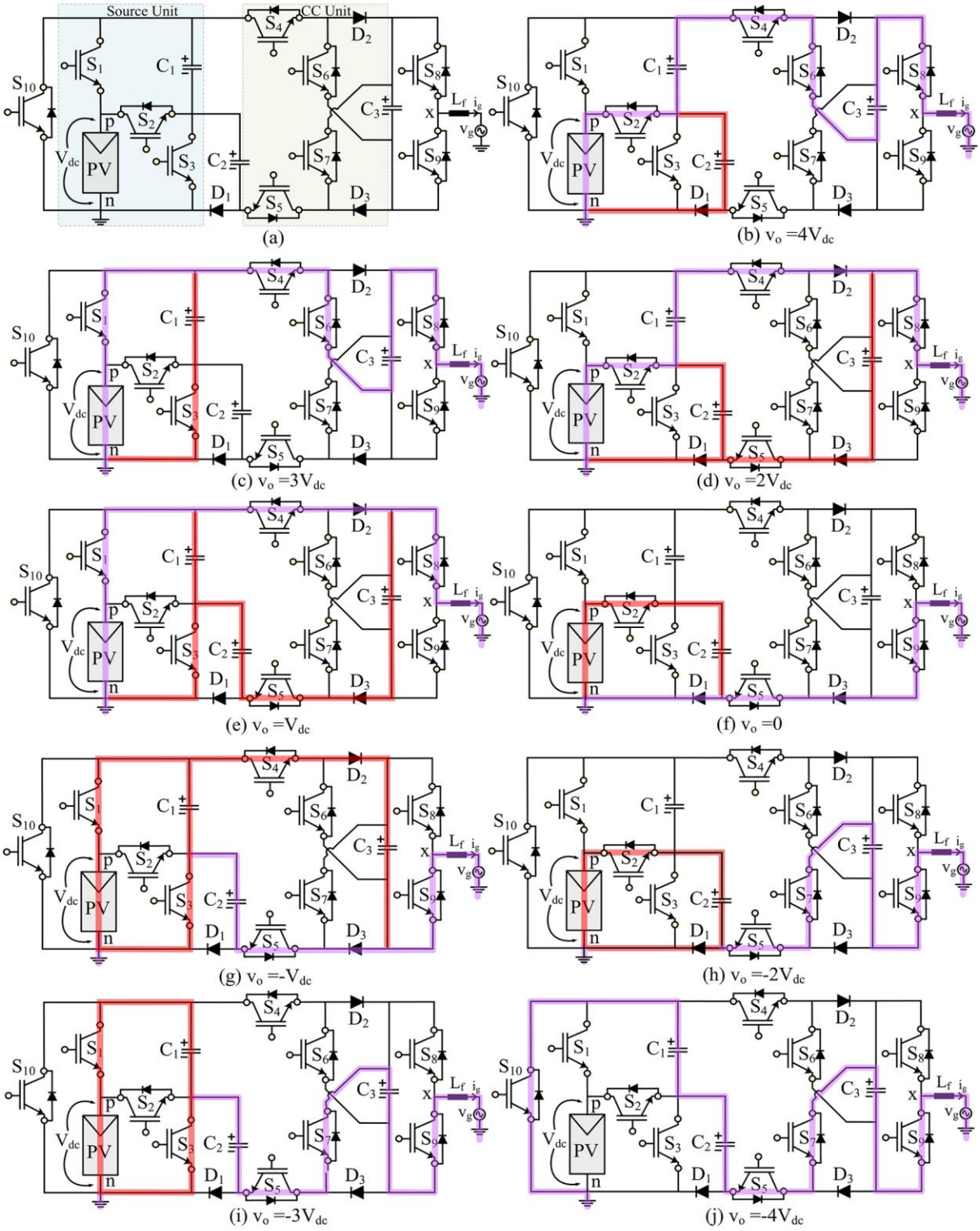


Figure 1. (a) Proposed 9L-QB topology, (b)-(j) Output voltage levels from +4V_{dc} to -4V_{dc}.

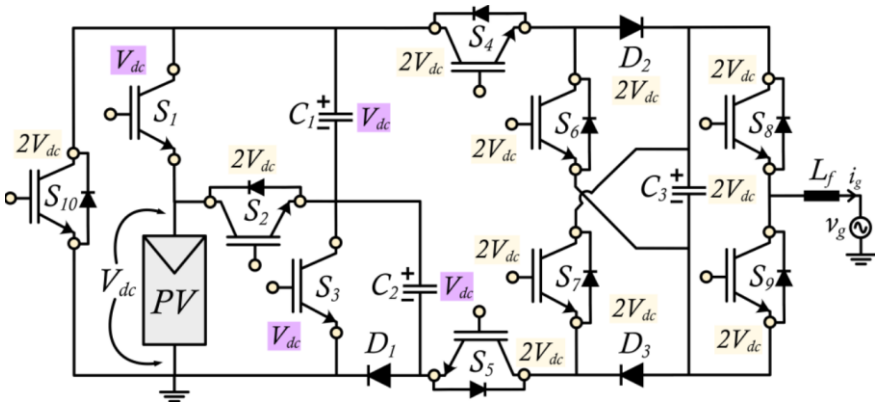


Figure 2. Maximum blocking voltage of switches and diodes, and capacitor voltage details of the proposed 9L-QB topology.

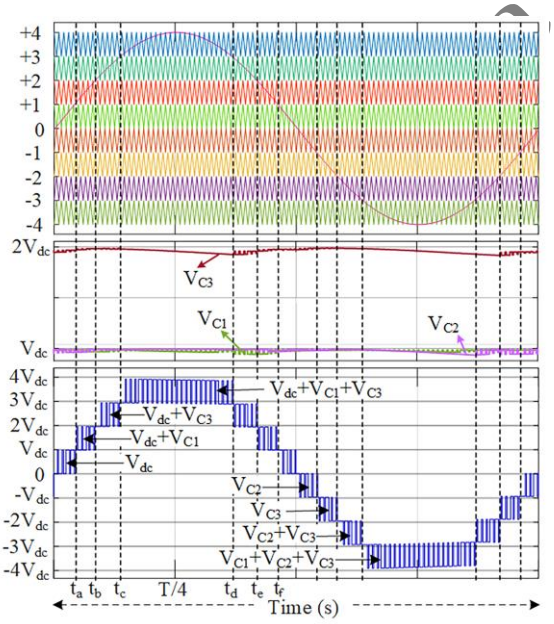


Figure 3. Modulation method along with capacitor voltage and nine-level output voltage waveforms of the proposed direct ground type inverter topology.

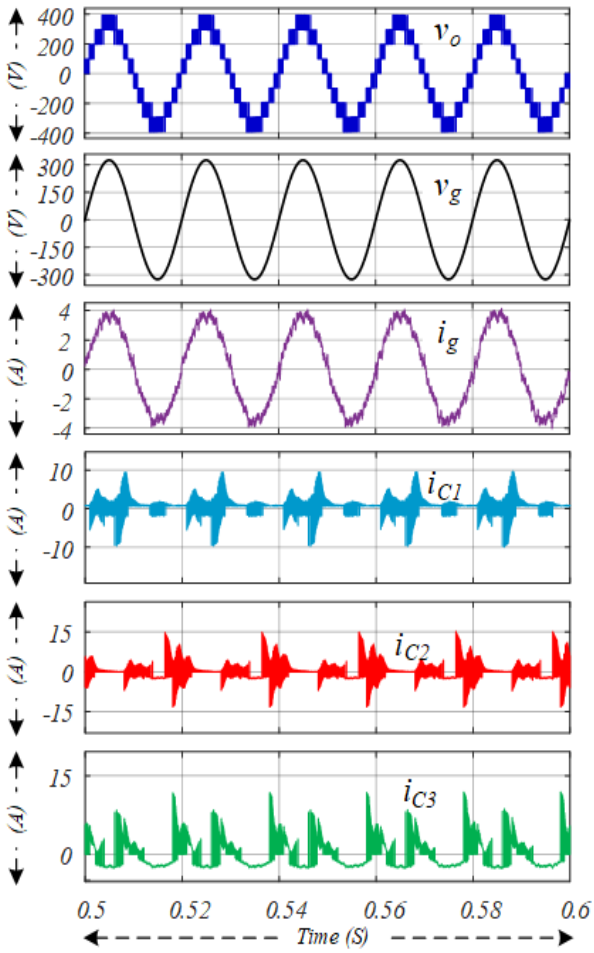


Figure 4. Simulation results of the proposed 9L-QB topology at UPF.

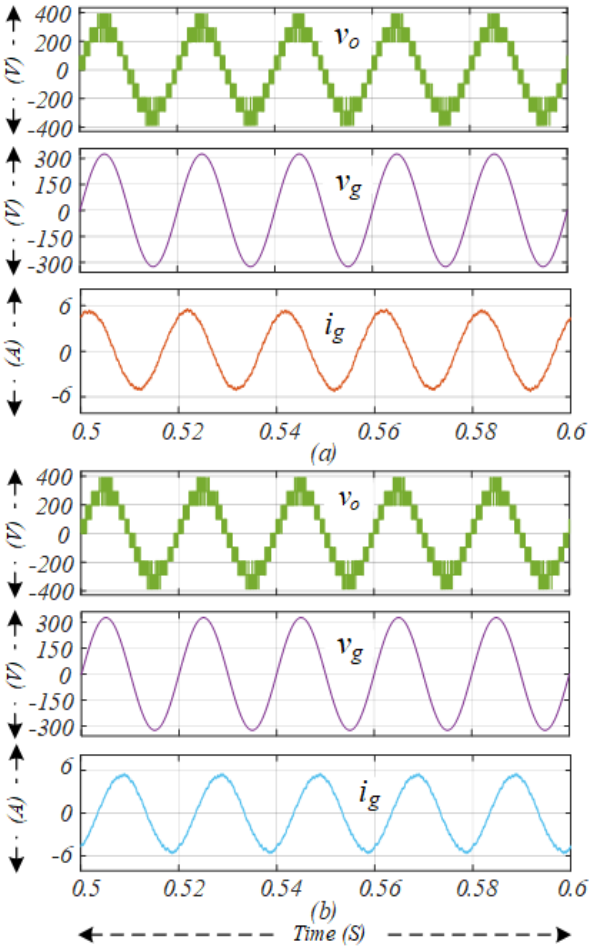


Figure 5. Simulation results of proposed 9L-QB topology at (a) 0.62 Lead PF, and (b) 0.62 Lag PF.

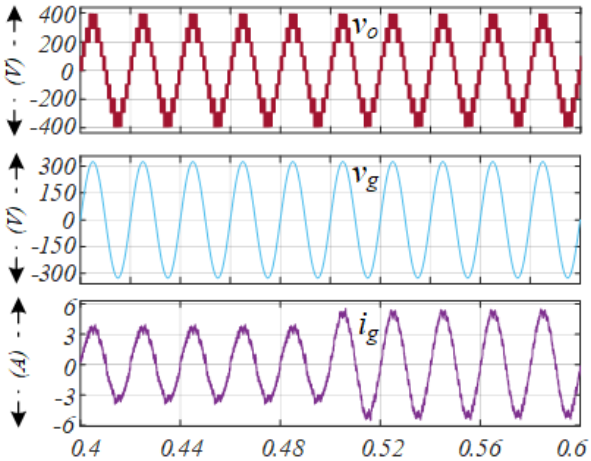


Figure 6. Simulation waveforms of the proposed 9L-QB topology when the reference grid current ($i_{g,\,ref}$) is changed from 4 A to 5.5 A.

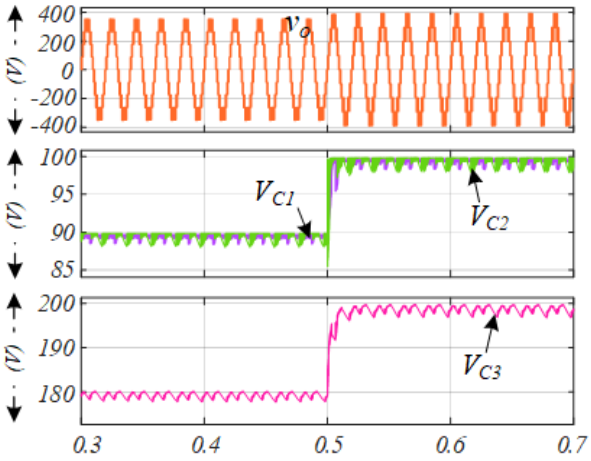


Figure 7. Simulation waveforms of the proposed 9L-QB topology when the input voltage (V_{dc}) is changed from 90 V to 100 V.

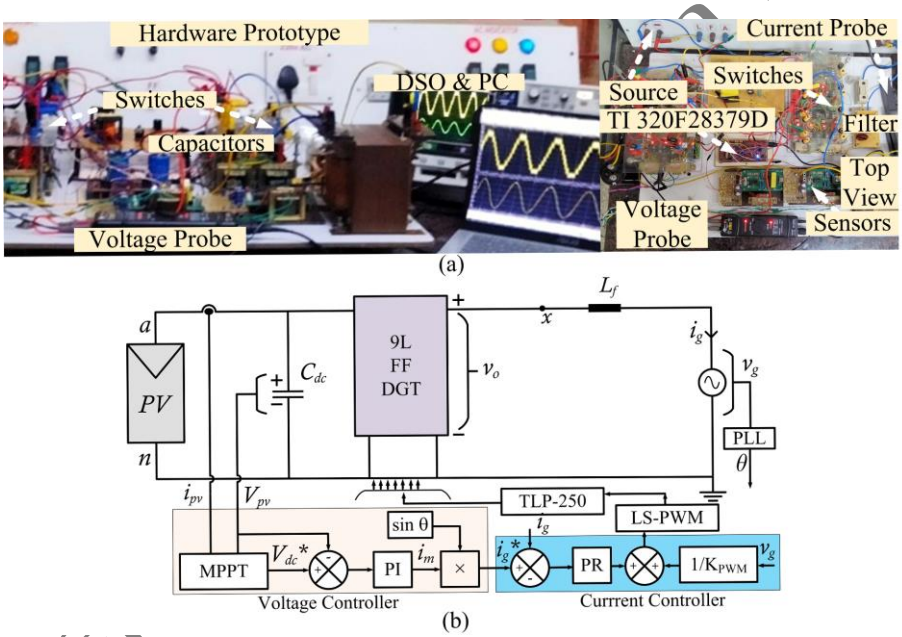


Figure 8. (a) Experimental setup and (b) Closed-loop control scheme of 9L-QB topology.

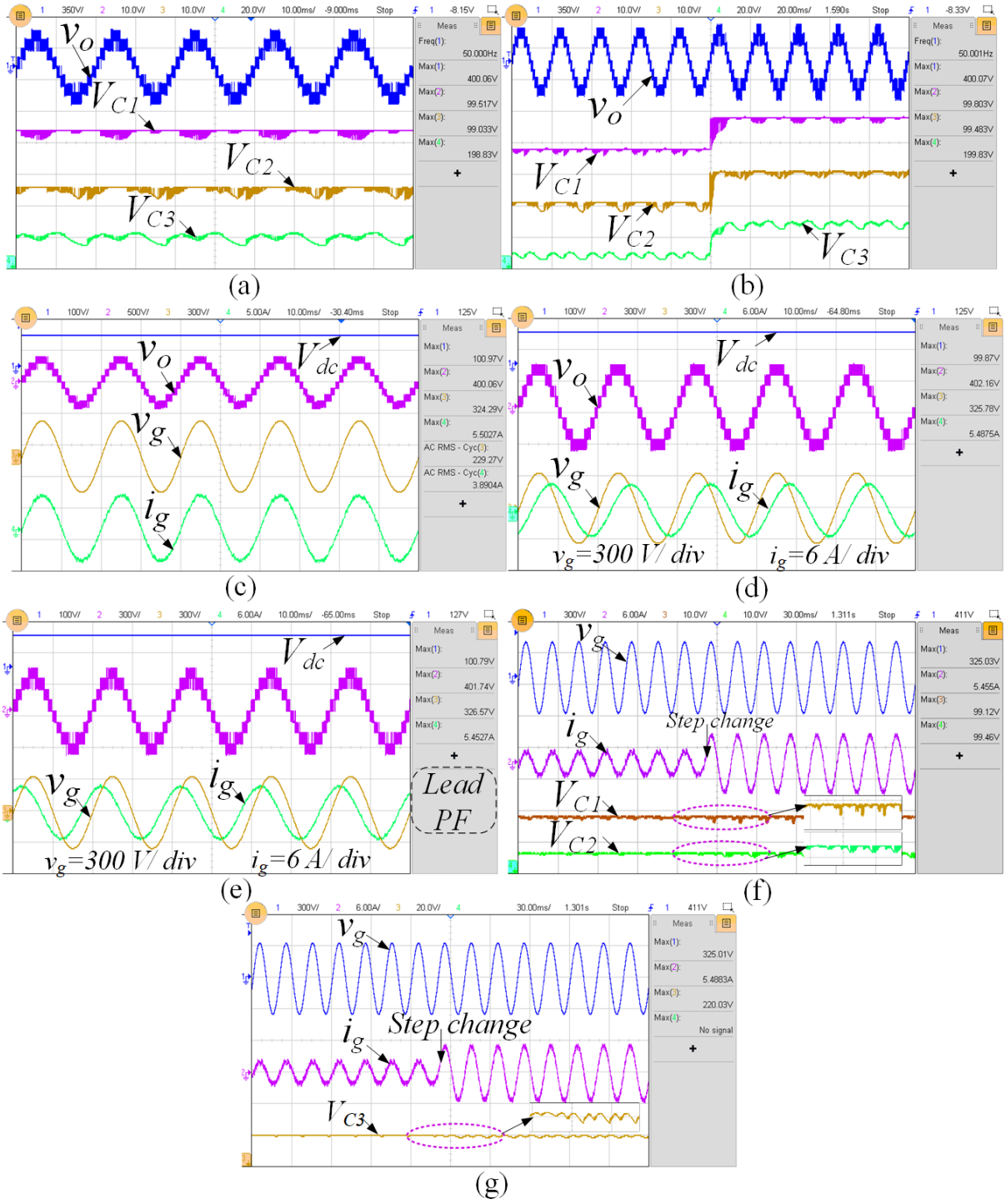


Figure 9. Experimental results. (a) v_o (350 V/div), V_{C1}, V_{C2} (10 V/div), and V_{C3} (20 V/div) at UPF, (b) v_o (350 V/div), V_{C1}, V_{C2} (10 V/div), and V_{C3} (20 V/div) when input is changed from 90 V to 100 V at UPF, (c)-(e) V_{dc} (100 V/div), v_o (500 V/div), v_g (300 V/div), and i_g (5 A/div) at UPF, 0.62 Lag PF, 0.62 Lead PF, (f) v_g (300 V/div), i_g (6 A/div), V_{C1}, and V_{C2} (10 V/div) when i_{ref} changed from 2.5 A to 5.5 A at UPF, (g) v_g (300 V/div), i_g (6 A/div), and V_{C3} (10 V/div) when i_{ref} changed from 2.5 A to 5.5 A at UPF.

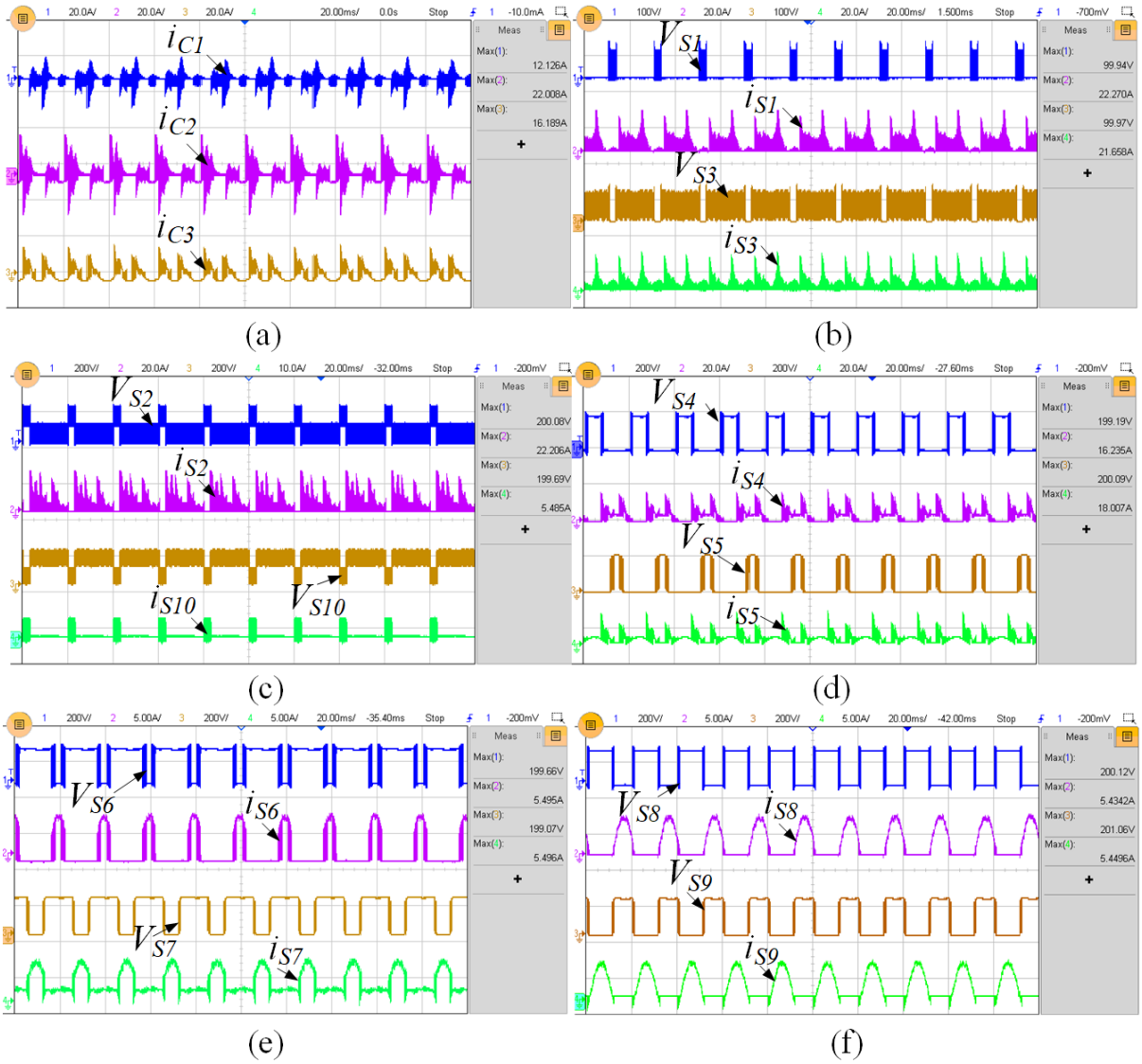


Figure 10. Experimental results at 895 W output power. (a) Capacitor current stress i_{C1}, i_{C2}, and i_{C3} (20 A/div), (b) Switch voltage and current stress V_{S1} (100 V/div), i_{S1} (20 A/div), V_{S3} (100 V/div), and i_{S3} (20 A/div), (c) Switch voltage and current stress V_{S2} (200 V/div), i_{S2} (20 A/div), V_{S10} (200 V/div), and i_{S10} (10 A/div), (d) Switch voltage and current stress V_{S4} (200 V/div), i_{S4} (20 A/div), V_{S5} (200 V/div), and i_{S5} (20 A/div), (e) Switch voltage and current stress V_{S6} (200 V/div), i_{S6} (5 A/div), V_{S7} (200 V/div), and i_{S7} (5 A/div), (f) Switch voltage and current stress V_{S8} (200 V/div), i_{S8} (5 A/div), V_{S9} (200 V/div), and i_{S9} (5 A/div).

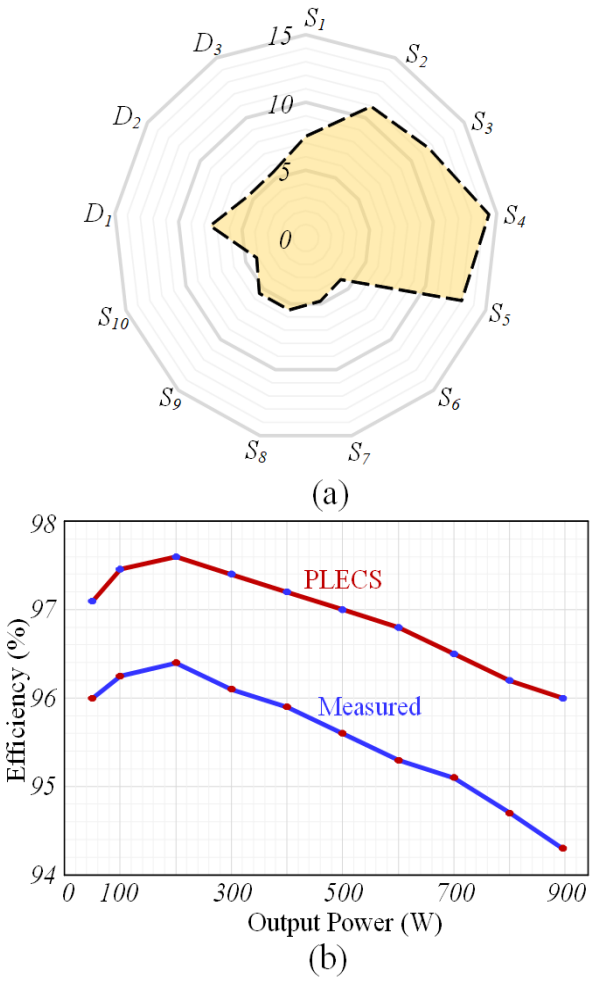


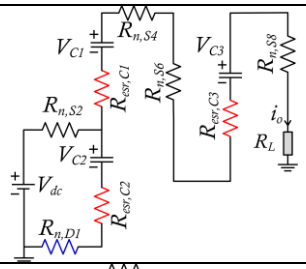
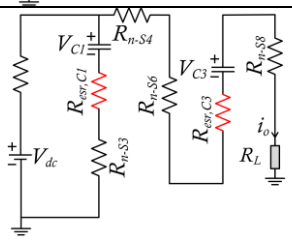
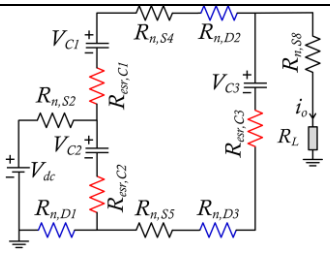
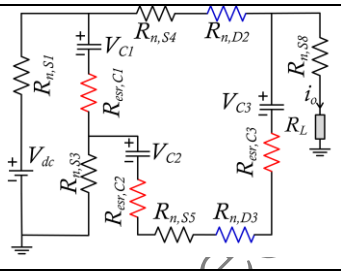
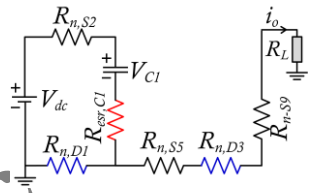
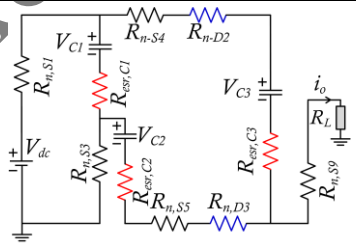
Figure 11. Power loss analysis with (a) PLECS loss breakdown of semiconductors, (b) Efficiency curve for various output power.

List of Tables with Table numbers

Table 1. Switching Sequence of 9L-QB

v_o	S_1 - S_{10}	C_1	C_2	C_3
$+V_{dc}$	S_1, S_3, S_4, S_5, S_8	↑	↓	↑
$+2V_{dc}$	S_2, S_4, S_5, S_8	↓	↑	↑
$+3V_{dc}$	S_1, S_3, S_4, S_6, S_8	↑	-	↓
$+4V_{dc}$	S_2, S_4, S_6, S_8	↓	↑	↓
0	S_2, S_5, S_9	-	↑	-
$-V_{dc}$	S_1, S_3, S_4, S_5, S_9	↑	↓	↑
$-2V_{dc}$	S_2, S_5, S_7, S_9	-	↑	↓
$-3V_{dc}$	S_1, S_3, S_5, S_7, S_9	↑	↓	↓
$-4V_{dc}$	S_5, S_7, S_9, S_{10}	↓	↓	↓
↑-Capacitor Charging, ↓-Capacitor Discharging, - No Change				

Table 2. Expression for conduction loss equations for 9L-QB topology

v_o	Equivalent circuit	Expression for conduction loss of the proposed nine-level inverter topology
$+4V_{dc}$		$P_{C+4} = \left(I_{S2,RMS}\right)^2 \cdot R_{n,S2} + \left(I_{S4,RMS}\right)^2 \cdot R_{n,S4} + \left(I_{S6,RMS}\right)^2 \cdot R_{n,S6} + \left(I_{S8,RMS}\right)^2 \cdot R_{n,S8} + \left(I_{D1,RMS}\right)^2 \cdot R_{n,D1} + \left(I_{C2,RMS}\right)^2 \cdot R_{esr,C2} + \left(I_{C3,RMS}\right)^2 \cdot R_{esr,C3}$
$+3V_{dc}$		$P_{C+3} = \left(I_{S1,RMS}\right)^2 \cdot R_{n,S1} + \left(I_{S3,RMS}\right)^2 \cdot R_{n,S3} + \left(I_{S4,RMS}\right)^2 \cdot R_{n,S4} + \left(I_{S6,RMS}\right)^2 \cdot R_{n,S6} + \left(I_{S8,RMS}\right)^2 \cdot R_{n,S8} + \left(I_{C1,RMS}\right)^2 \cdot R_{esr,C1} + \left(I_{C3,RMS}\right)^2 \cdot R_{esr,C3}$
$+2V_{dc}$		$P_{C+2} = \left(I_{S2,RMS}\right)^2 \cdot R_{n,S2} + \left(I_{S4,RMS}\right)^2 \cdot R_{n,S4} + \left(I_{S5,RMS}\right)^2 \cdot R_{n,S5} + \left(I_{S8,RMS}\right)^2 \cdot R_{n,S8} + \left(I_{D1,RMS}\right)^2 \cdot R_{n,D1} + \left(I_{D2,RMS}\right)^2 \cdot R_{n,D2} + \left(I_{D3,RMS}\right)^2 \cdot R_{n,D3} + \left(I_{C1,RMS}\right)^2 \cdot R_{esr,C1} + \left(I_{C3,RMS}\right)^2 \cdot R_{esr,C3}$
$+V_{dc}$		$P_{C+1} = \left(I_{S1,RMS}\right)^2 \cdot R_{n,S1} + \left(I_{S3,RMS}\right)^2 \cdot R_{n,S3} + \left(I_{S4,RMS}\right)^2 \cdot R_{n,S4} + \left(I_{S5,RMS}\right)^2 \cdot R_{n,S5} + \left(I_{S8,RMS}\right)^2 \cdot R_{n-S8} + \left(I_{D2,RMS}\right)^2 \cdot R_{n,D2} + \left(I_{D3,RMS}\right)^2 \cdot R_{n,D3} + \left(I_{C1,RMS}\right)^2 \cdot R_{esr,C1} + \left(I_{C2,RMS}\right)^2 \cdot R_{esr,C2} + \left(I_{C3,RMS}\right)^2 \cdot R_{esr,C3}$
0		$P_{C_{zero}} = \left(I_{S2,RMS}\right)^2 \cdot R_{n,S2} + \left(I_{S5,RMS}\right)^2 \cdot R_{n,S5} + \left(I_{S9,RMS}\right)^2 \cdot R_{n,S9} + \left(I_{D1,RMS}\right)^2 \cdot R_{n,D1} + \left(I_{D3,RMS}\right)^2 \cdot R_{n,D3} + \left(I_{C2,RMS}\right)^2 \cdot R_{esr,C2}$
$-V_{dc}$		$P_{C-1} = \left(I_{S1,RMS}\right)^2 \cdot R_{n,S1} + \left(I_{S3,RMS}\right)^2 \cdot R_{n,S3} + \left(I_{S4,RMS}\right)^2 \cdot R_{n,S4} + \left(I_{S5,RMS}\right)^2 \cdot R_{n,S5} + \left(I_{S9,RMS}\right)^2 \cdot R_{n,S9} + \left(I_{D2,RMS}\right)^2 \cdot R_{n,D2} + \left(I_{D3,RMS}\right)^2 \cdot R_{n,D3} + \left(I_{C1,RMS}\right)^2 \cdot R_{esr,C1} + \left(I_{C2,RMS}\right)^2 \cdot R_{esr,C2} + \left(I_{C3,RMS}\right)^2 \cdot R_{esr,C3}$

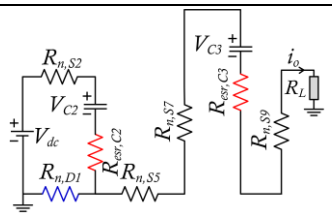
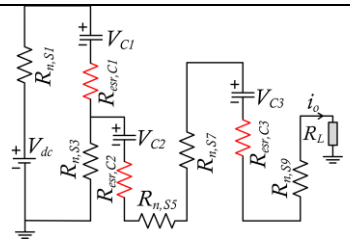
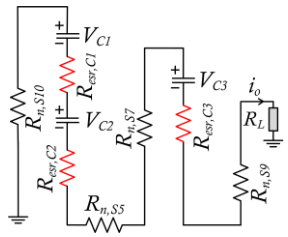
$-2V_{dc}$		$P_{C\_2} = \left(I_{S2,RMS}\right)^2 R_{n,S2} + \left(I_{S5,RMS}\right)^2 R_{n,S5} + \left(I_{S7,RMS}\right)^2 R_{n,S7} + \left(I_{S9,RMS}\right)^2 R_{n,S9} + \left(I_{D1,RMS}\right)^2 R_{n,D1} + \left(I_{C2,RMS}\right)^2 R_{esr,C2} + \left(I_{C3,RMS}\right)^2 R_{esr,C3}$
$-3V_{dc}$		$P_{C\_3} = \left(I_{S1,RMS}\right)^2 R_{n,S1} + \left(I_{S3,RMS}\right)^2 R_{n,S3} + \left(I_{S5,RMS}\right)^2 R_{n,S5} + \left(I_{S7,RMS}\right)^2 R_{n,S7} + \left(I_{S9,RMS}\right)^2 R_{n,S9} + \left(I_{C1,RMS}\right)^2 R_{esr,C1} + \left(I_{C2,RMS}\right)^2 R_{esr,C2} + \left(I_{C3,RMS}\right)^2 R_{esr,C3}$
$-4V_{dc}$		$P_{C\_4} = \left(I_{S5,RMS}\right)^2 R_{n,S5} + \left(I_{S7,RMS}\right)^2 R_{n,S7} + \left(I_{S9,RMS}\right)^2 R_{n,S9} + \left(I_{S10,RMS}\right)^2 R_{n,S10} + \left(I_{C1,RMS}\right)^2 R_{esr,C1} + \left(I_{C2,RMS}\right)^2 R_{esr,C2} + \left(I_{C3,RMS}\right)^2 R_{esr,C3}$

Table 3. Comparative analysis of the proposed single nine-level inverter topology

Ref		SCB				HBT			ANPC	DGT						
		[8]	[9]	[10]	[11]	[12]	[13]	[14]	[7]	[17]	[18]	[19]	[20]	[21]	[22]	[P]
N_S		12	13	14	11	12	8	12	10	11	9	10	11	10	12	**10**
N_G		11	13	12	10	12	8	11	10	10	9	9	10	9	11	**10**
N_D		0	3	1	0	0	2	2	2	2	3	3	2	2	1	**3**
N_C		3	3	2	3	3	3	4	5	3	3	3	3	3	3	**3**
N_L		0	0	0	0	0	0	0	0	0	0	1	0	0	1	**0**
BF		2	4	4	2	1	2	2	2	2	2	2	2	4	4	**4**
LSC		0.6	0.47	0.53	0.64	0.6	0.69	0.5	0.53	0.56	0.6	0.53	0.56	0.6	0.53	**0.56**
SPL		1.3	1.4	1.5	1.2	1.3	0.89	1.3	0.9	1.2	1	0.9	1.2	0.9	1.3	**0.9**
$MBV_{p.u.}$		V_{dc}	$2V_{dc}$	$4V_{dc}$	V_{dc}	$2V_{dc}$	$2V_{dc}$	$2V_{dc}$	V_{dc}	$2V_{dc}$	$2V_{dc}$	V_{dc}	$2V_{dc}$	$8V_{dc}$	$2V_{dc}$	$\mathbf{2V_{dc}}$
$MBV_{p.u.}/BF$		$0.5V_{dc}$	$0.5V_{dc}$	V_{dc}	$0.5V_{dc}$	$2V_{dc}$	V_{dc}	V_{dc}	$0.5\ V_{dc}$	V_{dc}	V_{dc}	$0.5\ V_{dc}$	V_{dc}	$2V_{dc}$	0.5	$\mathbf{0.5V_{dc}}$
$TSV_{p.u.}$		5.5	5.25	7.5	5	5	5.75	6	4.5	5.5	7	5	5.5	10	5.5	**4.5**
$TSV_{p.u}/N_{Le}$		0.61	0.58	0.83	0.56	0.56	0.64	0.67	1.1	0.61	0.78	0.56	0.61	1.1	0.61	**1.1**
CF	***α=.5***	28.75	34.6	32.8	26.5	29.5	23.8	32	29.25	28.75	27.5	28.5	28.75	29	30.7	**28.25**
	α=1	31.5	37.25	36.5	29	32	26.7	35	31.5	31.5	31	31	31.5	34	33.5	**30.5**
Max_{CS}		4	7	6	6	6	7	6	5	5	5	5	5	5	6	**5**
H-Bridge		No	No	Yes	No	No	No	Yes	No	No	No	No	No	Yes	No	**No**
LC		High	High	High	High	High	High	Low	Low	~0	~0	~0	~0	~0	~0	**~0**
C_{SBA}		S-L	S-L	S-L	S-L	S-B	S-L	S-L	S-L	S-L	S-L	S-L	S-L	S-L	S-L	**S-L**
CVDF		1	0.75	0.75	1	1.25	1	1.5	2	1	1.5	1	1	1.75	1	**1**
MVSC		V_{dc}	V_{dc}	$2V_{dc}$	V_{dc}	$0.5V_{dc}$	V_{dc}	V_{dc}	V_{dc}	V_{dc}	$2V_{dc}$	V_{dc}	V_{dc}	$7V_{dc}$	$2V_{dc}$	$\mathbf{2V_{dc}}$
η		95	97.3*#	*NA*	97.5*	*NA*	96.4	94.7	95.8	96.2	96.2	96.3	97.3*	95	95	**95.6**

***S-L*:** Sensor-less, ***S-B*:** Sensor-based, η**:** Efficiency @ 500 W**. #**-Efficiency % other than 500 W, ***:** Simulation efficiency, ***NA*:** Not available.

Table 4. Parameters for 9L-QB Inverter

Components	Values
Input Voltage (V_{dc})	100 V
Output Voltage ($v_{o,\,peak}$)	400 V
RMS Grid Voltage (v_g)	230 V
Output Power (P_o)	895 W
Frequency (f_o / f_{sw})	50 Hz / 5 kHz
Capacitor (C_1, C_2 & C_3)	1100 μF, 2700 μF, 3300 μF
Filter Inductor (L_f)	6.8 mH

Biographies:

John Britto Pitchai received the B.Tech. degree in Electrical and Electronics Engineering from the National Institute of Technology, Tiruchirappalli, India, in 2005, and the M.E. degree in Power Electronics and Drives from J.J. College of Engineering and Technology, Tiruchirappalli, India, in 2010. He is currently an Assistant Professor with the Department of Electrical and Electronics Engineering, J.J. College of Engineering and Technology, Tiruchirappalli. His research interests include multilevel inverter topologies and electrical drives.

Vijayarajan Periyasamy was born in Tittagudi in 1981. He completed his graduate programme in Electrical and Electronics Engineering from the University of Madras in 2003 and his post-graduate programme M.E (Power System Engineering) from Annamalai University in 2005. He completed a PhD degree program from the Faculty of Electrical Engineering at Anna University, Chennai, Tamil Nadu, India, in 2018. Since 2009, he has been working as an Assistant Professor in the Department of Electrical and Electronics Engineering, Anna University, BIT Campus, Tiruchirappalli. He has 18 years of experience in teaching and has published several papers in reputed international journals and national conferences. He is a Fellow of IEE and a Life Member of ISTE. His research interests include power systems, Application of power electronics converters in renewable energy systems, multilevel inverters and IOT applications to smart Electrical energy systems.