



Analysis and Hardening of Combinational Standard Cells Against Transient Faults Using Device-Level Simulations

Ali Zarei, Hamid R. Zarandi*, and Amir M. Hajisadeghi

Department of Computer Engineering, Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran

KEYWORDS

Soft Error;
Transient Fault;
Combinational Standard Cell;
Hardening;
Probability of Failure;
Device-Level Simulation.

ABSTRACT

This paper presents hardened standard cells against transient faults using device-level 3D-TCAD simulation insights. First, at the device level vulnerable zones in common standard cells—including NAND, NOR, and INV cells—are precisely identified under different strike energy, angle, and location scenarios. Then, transistor-level hardened NAND, NOR, and INV cell designs are proposed based on the vulnerable zones from device-level investigations, achieving high resilience to faults. Finally, the proposed hardened designs are reevaluated extensively using both device-level and circuit-level simulations, demonstrating full immunity against SETs and high immunity against single-event multiple transients on adjacent cells. Compared to related hardening methods, the designs achieve a significantly lower probability of failure up to 94.8%, while incurring moderate overheads in terms of area and power consumption, and achieving improved delay. Our device-level analysis reveals that NAND cells exhibit the highest vulnerability to particle strikes, while among adjacent-cell combinations, NAND-INV pairs show the highest vulnerability to multiple transients. In contrast, NOR-INV combinations demonstrate the lowest vulnerability. These findings underscore the effectiveness of leveraging device-level insights to develop highly reliable designs for soft error mitigation in safety-critical applications.

1. Introduction

Advances in CMOS technology have significantly improved the performance and density of digital circuits. However, these advancements come at the cost of increased susceptibility to transient faults, particularly soft errors induced by particle strikes [1]. Scaling down transistor sizes and reducing supply voltages have led to heightened challenges, as circuits become more vulnerable to single-event transients (SETs) and charge-sharing effects between adjacent nodes lead to multiple-event transients (METs) [2]. These phenomena pose a significant threat to the reliability of digital circuits, especially in cyber-physical systems (CPSs) operating in mission-critical environments [3, 4].

Soft errors in combinational circuits, caused by high-energy particle strikes, are particularly problematic as they can propagate through the system, potentially corrupting the final outputs [5]. Moreover, the effects of single-event multiple transients have become increasingly critical due to charge-sharing between closely placed transistors [1, 6]. Although various circuit and gate level fault analyses and accordingly cell hardening methods have been presented, a lack of layout and device level information is an essential defect [7, 8].

* Corresponding author.

E-mail address: h_zarandi@aut.ac.ir

In this context, several studies focusing on device-level abstraction have attempted to evaluate the impact of particle strikes on standard cells [9-12]. However, most of these studies fail to consider all key investigation parameters simultaneously in their assessments. Research conducted in [9] utilized device-level simulations for standard cells to examine whether NOR (NAND) gates exhibit lower SEU cross-sections compared to their equivalent composition gates, OR-INV (AND-INV). Nevertheless, this research did not account for the effects of particle angles or energies. Although the study in [10] on standard cells aimed to understand particle track behavior for designing fault-tolerant standard cells, it overlooked the influences of particle angles and cell adjacency. Another investigation [11] simulated ambipolar diffusion and bipolar amplification at the device level but disregarded the angular effect. Addressing these issues at the device level provides a unique opportunity to design more robust circuits by identifying and mitigating fault-prone areas before integration into larger systems [4, 13].

Standard cell hardening has emerged as a vital approach to enhancing circuit reliability against soft errors. While prior methods often rely on space or transistor redundancies introduced at the layout or circuit level [6, 14], these techniques can incur significant overhead and are highly dependent on design-specific considerations [6, 14, 15]. Alternatively, leveraging device-level analysis allows for precise identification of fault-sensitive zones, enabling targeted hardening with optimized trade-offs between reliability and resource utilization [13].

In particular, 3D-TCAD simulations play a pivotal role in enabling high-resolution investigations of particle strike effects, including the energy and angular dependencies of charge-sharing phenomena. The 3D-TCAD simulations provide insight into the physical interactions within transistor structures, facilitating the identification of vulnerable zones with precision [4, 13]. This capability enables the design of hardened cells that are both effective and resource-efficient, minimizing unnecessary redundancies while maintaining high fault tolerance.

In this paper, we build on work [4] by extending the investigation of transient faults vulnerabilities in standard cells to include the design and evaluation of hardened NAND, NOR, and INV cells. Through comprehensive 3D-TCAD simulations, we analyze the physical effects of particle strikes, including various energy levels and angles, to determine the most sensitive regions within each cell. Based on these findings, hardened designs are proposed by incorporating transistor-level modifications to mitigate transient faults effectively. The proposed transistor-level hardened cell designs are evaluated at both device and circuit levels, considering their immunity to single and multiple transients as well as their impact on delay and power consumption.

Our study demonstrates that the newly designed hardened standard cells achieve substantial improvements in transient fault tolerance. Experimental results confirm that these cells provide full immunity against SETs and high tolerance against multiple transient faults in adjacent cells while maintaining acceptable overheads. The main observations and contributions of this paper are summarized as follows:

- Comprehensive device-level analysis involving a detailed investigation of particle strike effects, including energy levels, strike angles, and charge-sharing phenomena, to pinpoint fault-prone regions in standard cells.
- Analysis at the device level reveals that among the examined cells, the NAND cell exhibits the highest susceptibility to particle strikes.
- Analysis at the device level reveals that among the various cell compositions examined, NOR-INV cells exhibit the lowest vulnerability, while NAND-INV cells show the highest susceptibility as adjacent cells.
- Presenting hardened design of NAND, NOR, and INV cells against transient faults.
- Verification of the proposed designs in cross-layer simulations, ensuring high resilience under various fault scenarios.

The rest of this paper is organized as follows: Section 2 is dedicated to reviewing previous works in fault analysis and cell hardening methods. Section 3 comprehensively investigates the device-level analysis in different fault conditions. Section 4 presents the hardened cells' design and their evaluation. Finally, Section 5 concludes the paper.

2. Related Work

Fault tolerance analysis of combinational circuits under particle strikes has been extensively studied across different abstraction levels. These studies focus on fault localization, error propagation, and mitigation techniques. Gate-level approaches have been particularly effective for the rapid estimation of soft error rates by leveraging logical, electrical, and timing masking factors. For instance, [16] presents a fault propagation probability model that considers some essential factors,

while [17] employs graph-based restructuring and circuit partitioning to improve circuit reliability. These methods, while efficient, are limited in addressing detailed physical effects like charge sharing and sensitive zone interactions.

At the transistor and layout levels, several techniques have been developed to alleviate this limitation. These methods [5, 18–20] identify and mitigate sensitive areas within standard cells, achieving notable reductions in multiple-event occurrences. For example, [5] reports around a 20% reduction in METs by refining layout design, and [19] models METs with greater accuracy than gate-level simulations, showing that optimized cell placement significantly impacts fault resilience. Additionally, [20] demonstrates that sensitive area analysis and guard rings can effectively mitigate SETs.

Work [21] presented a selective-transistor redundancy (STR) approach for fault tolerance in combinational circuits. This technique identifies sensitive transistors based on their probability of soft error detection and applies duplication and scaling selectively to meet reliability or area constraints. It also introduces a novel gate-level reliability evaluation framework, demonstrating a substantial reduction in computational time compared to transistor-level simulations. Work [22] evaluated two radiation-hardening techniques for standard cells: gate sizing and transistor stacking. The study examines their impact on the area, power consumption, and SET mitigation. Gate sizing, by increasing transistor dimensions, achieves a better trade-off between reliability and performance, though it increases power consumption. Transistor stacking provides lower power consumption but exhibits higher sensitivity to input variations. The analysis highlights that while both techniques reduce SET cross-section at lower energy levels, gate sizing generally outperforms stacking in terms of robustness and overall efficiency.

Recent advancements in 3D-TCAD simulations have further refined device-level investigations, enabling precise characterization of particle strike effects, including charge-sharing phenomena and MET scenarios. For instance, research [4] analyzes different configurations—such as isolated cells and cells placed adjacent to others—using both circuit- and device-level simulations, demonstrating the significance of low-level evaluations and the notable differences in failure rates between abstraction levels. Similarly, the LBSEVEA method in [11] combines device-level and SPICE-level simulations to analyze ambipolar diffusion and bipolar amplification, providing detailed insights into fault propagation. This paper leverages comprehensive 3D-TCAD simulations to identify fault-prone zones and inform the design of hardened standard cells. By targeting critical vulnerabilities and minimizing the need for redundancies, the proposed approach achieves enhanced fault tolerance while maintaining efficiency.

3. Device-Level Analysis

The estimation of SET and MET rates in large-scale integrated circuits can be challenging due to the dependency of particle strike characteristics on various factors, such as particle LET (linear energy transfer), strike location, and strike angle [1, 5, 15]. To evaluate these effects on the vulnerability of standard cells, this study conducts simulations at two abstraction levels: device-level and circuit-level.

At the device level, a particle strike on the silicon surface transfers energy to the circuit, potentially causing an instantaneous current at sensitive nodes. Simulations at this level analyze the effects of particle tracks, strike angles, and collected charge. Additionally, to extend the analysis to adjacent cells, circuit-level simulations incorporate the effects observed in device-level analysis. These simulations enable the characterization of the most and least sensitive combinations of standard cells in both identical and non-identical adjacency configurations.

Device-level simulations were conducted using 3D-TCAD tools [23, 24], with wide experiments performed to ensure robustness and circuit-level evaluations were done using HSPICE. In this regard, the 45nm FreePDK and 45nm NanGate open-cell libraries are utilized [25] to model three universal standard cells: INV, NOR, and NAND. To simulate particle strikes, parameters such as strike location, angle, and LET were varied systematically. Fault injection simulations employed five types of ions with varying energies (10 to 150 MeV.cm²/mg) and strike angles ranging from 0° to 90° to NMOS and PMOS transistors. Table 1 summarizes the particle characteristics used in the experiments [26, 27].

To evaluate the effects of charge sharing, 3D simulations assessed the impact of particle strikes on both identical and non-identical adjacent cells. The cells were chosen at the minimum size (X1) from the standard library to reflect realistic usage in circuits. The collected charge was recorded for each node to determine the extent of charge-sharing effects. Layout information was extracted to the GDML file format for detailed analysis, and metallization and substrate thickness were provided by the process. Circuit-level simulations were performed using exhaustive input stimulus combinations to support robust statistical analysis. This allowed the evaluation of failure probabilities for the victim and adjacent cells under various input states and configurations.

To create a 3D-TCAD model of standard cells, the process begins by defining the standard cell at the transistor level. The layout is then extracted from the library, and the final model is generated using 3D-TCAD tools, as illustrated in Fig. 1. To evaluate the interactions between identical and non-identical cell adjacencies, different arrangements of cells across three consecutive layout rows are analyzed. As shown in Fig. 2(a), the standard cells, such as INV, are placed to study charge-sharing effects. Adjacent cells are electrically isolated to ensure the worst-case scenario since electrical connections could reduce the impact of particle strikes. Each cell is independently connected to the power supply and ground. In this configuration, three rows of cells are used, with three adjacent standard cells per row.

Charge-sharing effects on non-identical cells are analyzed by rearranging the cells. Specifically, three rows of identical cells are used, but the central cell in each configuration is replaced with a non-identical one. An example setup is shown in Fig. 2(b), where an INV cell is surrounded by eight NOR cells, illustrating the placement for evaluating the charge-sharing effects.

3.1. Particle Track Analysis

Due to the differences in the design of NMOS and PMOS transistors, ion collisions exhibit diverse behaviors. For instance, when a particle strikes the drain of an off-state PMOS transistor, charge sharing can occur, potentially impacting adjacent off-state NMOS transistors. This increases the probability of node corruption in neighboring cells. To understand these dynamics, particle injections were conducted for both NMOS and PMOS transistors.

Tables 2 and 3 summarize the maximum particle track lengths for standard cells surrounded by identical and non-identical neighboring cells under varying LETs and particle angles in PMOS and NMOS transistors, respectively. The tables detail energy levels, particle strike characteristics, and the behavior of the center cell when interacting with its surroundings. For example, under a 10 MeV.cm²/mg LET, the particle track for a NAND cell surrounded by identical NAND cells is longer compared to when the same NAND cell is surrounded by NOR or INV cells. Several observations from the data are: 1) Among identical adjacent cells, the NAND-NAND configuration exhibits the greatest sensitivity due to its longer particle track, making it the most vulnerable combination. 2) For non-identical adjacent cells, the NAND-INV configuration shows the highest susceptibility. 3) The effect of particle tracks on non-identical adjacent cells is asymmetric. For instance, under a 10 MeV.cm²/mg LET, the particle track for a NAND cell surrounded by INV cells is shorter compared to an INV cell surrounded by NAND cells. This highlights the non-linear interaction between cell types. 4) The NOR-INV combination is the least vulnerable among the investigated non-identical configurations, showing the shortest particle tracks. These results provide valuable insights into the interplay between particle strikes and charge sharing, offering critical information for designing fault-tolerant cells.

3.2. Particle Angles Analysis

The angle of a particle strike significantly influences its impact on transistor surfaces, often increasing the probability of charge sharing. This occurs for two main reasons: 1) angular strikes can simultaneously affect multiple charge-sharing sources, such as depletion region drift, diffusion charge collection, well-collapse source injection, and parasitic bipolar enhancement [28]; and 2) angular strikes can hit two adjacent nodes at the same time, exacerbating charge-sharing effects [29]. For instance, as illustrated in Fig. 3, a particle following track D can simultaneously affect nodes 3 and 4, a scenario not observed with vertical tracks like B and C. Although such simultaneous hits are rare, angular strikes generally increase the probability of charge sharing.

Table 4 shows the most disruptive angles (i.e., the angle at which the largest charge is collected) for the adjacent cells. Our results indicate that the largest charge collection in a single cell occurs when the particle strikes the drain of the victim transistor at a vertical angle (0° W-E). However, in the presence of adjacent cells, the most disruptive angles fall between 30° and 60°. Simulations conducted with angular increments of 5° reveal that angles near 60° consistently result in the highest charge collection in adjacent cells, making them particularly vulnerable. Moreover, the collected charge across the 30° to 60° range remains substantial, highlighting this interval as critical for charge-sharing effects.

While angular strikes within this range induce significant charge sharing, they typically collect less charge at the victim cell's transistor compared to normal incidence. However, this reduced charge is often sufficient to disrupt output nodes, emphasizing the importance of considering angular effects in fault-tolerant design. These findings underscore the need for robust evaluation of angular strikes to ensure the resilience of standard cell configurations.

3.3. Collected Charge Analysis

The evaluation of cells was conducted both with and without adjacent cells to measure the collected charge in each configuration. Table 5 presents the collected charge values for NAND, NOR, and INV gates under different LETs when their PMOS or NMOS transistors were struck by particles. All data were obtained at a 0° particle strike angle. Results revealed that higher LET particles resulted in greater charge collection in the cells. Notably, when particles struck the NMOS transistor of a NOR cell, the largest charge was collected, while a similar observation was made for NAND cells when their PMOS transistors were struck. In the case of INV cells, collected charge levels were comparable for both PMOS and NMOS strikes. Across all scenarios, PMOS transistors consistently collected more charge than NMOS transistors.

Figure 4 depicts the collected charge in adjacent cells when particles struck the center cell under various angles (0° to 80° W-E) and LET values. These results include all possible configurations of NAND, NOR, and INV cells as both center and adjacent cells. In all cases, the center cell was designated as the victim cell, experiencing particle strikes on either its PMOS or NMOS transistors.

Higher LET values, particularly those exceeding $100 \text{ MeV.cm}^2/\text{mg}$, significantly increased the collected charge in adjacent nodes, often surpassing 200 fC . The most sensitive angular range for charge sharing was identified between 30° and 60° W-E, where the collected charge reached its peak. This phenomenon is attributed to the longer particle tracks at these angles, which enhance charge-sharing effects. Conversely, particle strikes at angles closer to 0° W-E or at ground angles resulted in minimal charge sharing. Overall, these findings emphasize the critical influence of LET and angular variations on charge-sharing dynamics. The consistent observation of higher charge collection in PMOS transistors further underscores their vulnerability, providing key insights for designing robust and fault-tolerant standard cell configurations.

3.4. Multiple Event Transient Generation Analysis

Device-level simulations reveal critical aspects of multiple event transients. Angular strikes, particularly between 30° and 60° , have a significantly greater impact on adjacent cells compared to normal incidence. Experimental data indicate that higher LET particles amplify charge sharing, increasing the probability of multiple transients. Table 6 outlines the probabilities of single event multiple transient occurrences in adjacent cells. In summary, results show that the probability of two or three adjacent cell cases remains below 5%, even under high LET conditions and sensitive angular ranges.

In most scenarios, the total charge transferred to the victim cell is higher than the charge collected in adjacent cells. However, variations exist where the adjacent cells collect a higher charge. The figure illustrates common MET patterns observed during simulations. Some scenarios, such as Fig. 6(d), show near-complete charge sharing among adjacent cells, while others, like Fig. 6(e)-(f), highlight distributions involving the victim cell and adjacent cells.

It is worth mentioning due to fundamental differences across various process technologies (e.g., Planar, FinFET, etc.), our findings cannot be directly mapped, and performing the same analysis approach is required. However, if the process technology remains the same and only the technology node size changes, the derived results can be generalized to the new node. For instance, findings such as the most disruptive strike angles and the cells most vulnerable to particle strikes under different conditions can be generalized to other technology node sizes.

4. Circuit-Level Evaluation

To evaluate the failure rates of cells, the charge values measured at the device level are injected into circuit nodes. Circuit-level simulations are performed extensively to analyze the electrical behavior of particle strikes by modeling current injections at sensitive nodes. A double-exponential current model [11] is used to replicate single-event effects during circuit simulation. This model adjusts the injected current based on collected charge values and compares these with the critical charge (Q_{crit}), a threshold indicating whether a fault will propagate to the output. The parameters of the current model, including rise and fall times, are tuned to reflect realistic conditions. Current injection is conducted using the HSPICE tool, adapted to simulate various LETs, angles, and transistor types for NAND, NOR, and INV cells. In this regard, equations (1) to (5) are used. When accumulated charges fall below Q_{crit} , equation (1) is applied,

$$I(t) = \begin{cases} 0 & t < t_{d1} \\ I_m \left(1 - e^{-\frac{(t-t_{d1})}{\tau_a}} \right) & t_{d1} \leq t < t_{d2} \\ I_m e^{-\frac{(t-t_{d1})}{\tau_b}} & t \geq t_{d2} \end{cases} \quad (1)$$

where t_{d1} and I_m are the pulse delay time and peak current, respectively, that are given by,

$$I_m = \frac{V_{DD}}{R_{on}} \quad (2)$$

where V_{DD} and R_{on} are the source voltage and on-state resistance, respectively. In the circuit-level simulation, the collected charge is compared with Q_{crit} and if this value is greater than Q_{crit} , then charge injection will be performed in a proper duration and frequency, through equations (3) to (5) [11],

$$Q_{crit} = \frac{V_{DD}}{R_{on}} \left[(\tau_1 - \tau_2) + (t_{d2} - t_{d1}) - \tau_1 e^{-\frac{(t_{d2}-t_{d1})}{\tau_1}} \right] \quad (3)$$

where τ_1 is the rise time and τ_2 is the fall time,

$$\tau_1 = \frac{\left(\frac{Q_{coll}}{I_m} \right) - (t_{d2} - t_{d1})}{e^{-\frac{(t_{d2}-t_{d1})}{\tau_1}} - 1} \quad (4)$$

$$\tau_2 = (1-f) \frac{Q_{coll}}{I_m}$$

and f is calculated by,

$$f = \frac{\int_{t_{d1}}^{t_{d2}} I_m (1 - e^{-\frac{(t-t_{d1})}{\tau_1}}) dt}{Q_{coll}} \quad (5)$$

The probability of failure (PoF) is calculated for each standard cell using a weighted model that accounts for sensitive node probabilities, diffusion areas, and output flipping probability [30]. This metric quantifies the probability of an erroneous output due to particle strikes. PoF values are derived for different input states, LETs, and particle angles, ensuring comprehensive evaluation across scenarios.

Since our simulation at the device level was done with different particles and strike situations, it is necessary to consider all these conditions at the circuit level. To this end, a script has been written to apply this information at the circuit level. In each simulation, if the output voltage reaches half the nominal voltage, then it will be considered a failure. The PoF has been obtained for each standard cell as,

$$PoF = \sum_{i=1}^N E_i \times W_i \quad (6)$$

where in this equation, N represents the number of sensitive nodes within the circuit. The variables E_i and W_i denote the probability of output change and the area proportion of a node, respectively. The value of E_i is calculated using:

$$E_i = \frac{\sum_{j=1}^M FC_{i,j}}{M} \quad (7)$$

where $M = p \times q \times r$ is the number of fault injection scenarios applied to the sensitive node i . Here, p , q , and r represent the number of input vectors, particle energy levels, and particle incident angles, respectively. $FC_{i,j}$ denotes a faulty case j and is assigned a value of 1 if the fault causes the output to cross half of the supply voltage level; otherwise, it is 0. Also, W_i is given by,

$$W_i = \frac{A_i}{\sum_{j=1}^N A_j} \quad (8)$$

where A_i is the occupied diffusion area of node i .

In this regard, PoF is calculated for cells subjected to particles with varying LET values, considering both normal and angular incidences. Extensive simulations identify the most and least sensitive cells. The PoF values are derived across all input levels, ensuring that the energy transferred to the circuit is analyzed for each input vector. The input vectors are applied in circuit-level simulations, where the transferred energies are modeled through a current source, and the circuit outputs are monitored.

Table 7 presents the failure probabilities for individual standard cells in isolation, without neighboring cells. The simulations were conducted on standalone cells, where all transferred energy was introduced as a current source under varying conditions such as LET, strike angle, and PMOS/NMOS injections. Simulation results reveal that the NAND cell exhibits the highest PoF when isolated from adjacent cells. This is attributed to its higher susceptibility to charge collection under various conditions. Conversely, the NOR cell demonstrates the lowest PoF among the experiments.

Figure 6 illustrates the PoF of adjacent cells for these standard cells across varying LET values (10–150 MeV·cm²/mg). We iterated each configuration of the fault injection experiment 10000 times and reported the PoF with a 99.7% confidence level (3-sigma), demonstrating the high statistical stability of our results. The experiments reveal that the NAND-NAND pair is the most sensitive, while the NOR-NOR pair is the least sensitive among identical cell combinations. For non-identical pairs, the NAND-INV combination shows the highest vulnerability, whereas the NOR-INV combination is the least affected. In summary, these results provide insights into optimal cell configurations for reliability-aware design. For instance, using less vulnerable combinations, such as NOR-NOR or NOR-INV, in place of NAND-NAND or NAND-INV, can significantly enhance circuit robustness. These results enable designers to optimize cell placements and configurations to minimize soft error rates in mission-critical applications.

5. Hardened Cell Design

Previous approaches to hardening standard cells against particle strikes have frequently utilized spatial redundancy techniques [5, 15]. These methods depend on accurate placement information since the effectiveness of redundancy is influenced by the final positioning of cells, which is determined after placement. In contrast, this study proposes a hardened standard cell design developed using physical 3D-TCAD simulations, focusing on fortifying specific vulnerability areas.

In this section, the proposed hardened standard cells are presented. Each cell is hardened based on the sensitive areas identified using device-level information. Before applying the transistor-level hardware redundancy method to harden cells against particle strikes, it is crucial to determine the sensitive zones of each standard cell. To achieve this, we use information extracted from device-level simulations, which are then analyzed at the circuit level to calculate the failure probability for each sensitive zone.

Table 8 presents the failure probability for sensitive zones of the standard cells. The hardening process for the standard cells is carried out based on the identified most sensitive zones. Specifically, a holding transistor is added innovatively into the sensitive zone with an appropriate size to mitigate the effects of particle strikes and create a discharge path to VDD or ground, thereby eliminating the unwanted collected charge of the transient fault.

The proposed hardened Inverter cell and its sensitive zones have been shown in Fig. 7. It should be noted that each added transistor to the hardened INV cell has its probability of failure against particle strike. In other words, when a transistor is added to the sensitive zone of an inverter cell to prevent the particle strike from affecting the output, there is a possibility that the added transistor itself may be struck by a particle or may even amplify the effect of the induced charge. To prevent this condition, a redundant transistor was added, and device-level simulation, as well as circuit-level simulation, were carried out to find the probability of failure for the output inverter cell. This scenario has been repeated until the proposed inverter cell has been designed.

The proposed inverter incorporates six redundant transistors, resulting in a significant reduction in the overall cell's probability of failure. Transistors M1 and M2 with 0.5X size have been chosen to reduce the drive strength. Adding the series transistor (T) will help to reduce the particle strike effect, but this will lead to a new sensitive zone. To solve this problem,

two transistors M3 and M4 are inserted. These two transistors will help to diminish the effect of particle strike at nodes N1 and N2, respectively. Finally, transistors M5 and M6 will reduce the particle strike effect of the redundancy of the circuit. Consider a case where a particle strikes the drain of transistor T1. In this case, if M1 is in the off-state, then the ion strike has no path to the output; and if it is in the on-state, then the restore current path will turn on, and VDD will annihilate the induced current. The same scenario will happen when a particle strikes the M1 transistor. If transistor T1 is in the on-state, then T1 will put down the current induced through the restore path, and if T1 is in the off-state, then M1 will decrease the current amplitude by itself, and next, the transistors M3 and M4 will turn on and eliminate the effect of the ion strike. In cases where particles strike transistors M3/M4 or M5/M6 since the induced current will cause these transistors to turn on instantly, there will be a restore path to reduce the transient effect.

Fig. 8 shows the simulation waveform of the presented hardened INV cell and its ability to eliminate the SET effect. As stated in Section 3, various values for fault injections have been considered, and all these values are injected at different times. As an example in Fig. 8, a single event transient in the sensitive zone does not cause output failure, and the unwanted voltage is immediately discharged. It is worth noting that in most hardened circuits, although the added transistors can mitigate the effects of particle strikes in the primary design, they introduce a new source of fault. In this work, the proposed hardened standard cells reduce this impact as well, albeit at the cost of increased power consumption and delay overhead.

The presented hardened NOR cell has been shown in Fig. 9. Three transistors have been added to the conventional NOR cell to mitigate single event transient. The sensitive zones in the NOR cell need to be hardened against particle strikes. The first sensitive zone is related to transistor T1, and the second sensitive zone is shared between transistors T3 and T4. If particle incidence happened in T1, then there are two conditions: 1) transistor T2 is in the on-state. In this situation, the effect of the particle strike will turn the M1 and M2 transistors on, and they will diminish the induced current immediately. 2) Transistor T2 is in an off state; in this situation recovery path will be generated after T1 turns on. There will be the same scenario for transistors T2, T3, and T4, except that in those transistors, there will be only one sensitive zone, and therefore one transistor is enough to eliminate the transient's effect. The simulation waveform of the presented hardened NOR cell, shown in Fig. 10, demonstrates the transient fault tolerance ability of the NOR cell in the presence of a single event transient that occurred in the sensitive zone.

The presented hardened NAND cell is shown in Fig. 11. Since the NAND cell is similar to the NOR cell, the hardening process is similar. In this regard, the M1 transistor is added in the NAND cell to the immunized output node, while M2 and M3 are added to the immunized node N2 and the output nodes. Since NAND was the most vulnerable cell to particle strike, 2X-sized transistors were chosen for nodes N2 and output. The simulation waveform of the presented hardened NAND in the presence of a single event transient in the sensitive zone has been shown in Fig. 12.

The PoF for each hardened cell, compared to the conventional design across various LETs, is presented in Table 9. Notably, charge sharing and single-event multiple transients have been accounted for in the PoF calculation. The results indicate that the probability of failure for the hardened cells remains below 2%, even at high LETs. This demonstrates the effectiveness of utilizing device-level data in the hardening process to mitigate the impact of particle strikes.

Table 10 provides a comparison between the proposed method and two previous works that have focused on hardening-by-design techniques and adding redundancy [21, 22]. To determine the probability of failure of these two previous works, the same device-level evaluation must be conducted. In this regard, the collected charges obtained from device-level analysis are modeled as a current source for circuit simulation. The same script was used to perform the circuit simulations, and the PoF was calculated using Equation (6). As shown in Table 10, the proposed method demonstrates significant superiority in terms of the probability of failure over the other two methods while maintaining moderate power consumption and acceptable delay.

On average, the proposed hardened cells introduce up to 75% delay overhead relative to the basic unhardened design. In this regard, among the three proposed standard cells, the INV cell exhibits the highest delay overhead. This is due to the simplicity of the conventional INV cell and the additional redundancies required during its hardening process. Additionally, the use of transistors with 0.5X size in the INV cell's hardening process contributes to the increased delay in the output signal. Despite this, while the proposed method significantly decreases the PoF, it also exhibits on average 44.7% and 27.8% lower delay when compared to previous works [21], and [22], respectively.

The power consumption of the proposed hardened cells, when compared to examined related works [21] and [22], falls within on average 59.2% and 45% overhead. However, it is important to note that the presented standard cells of these methods exhibit a higher PoF compared to our method. Also, the power consumption of the proposed cells in this work is

less than half of conventional hardening methods such as the triple modular redundancy (TMR) technique.

In terms of area, the proposed hardened cells exhibit an increased footprint due to the use of additional transistors and diffusion regions, as expected. When compared with related works [21] and [22], the proposed designs exhibit an average of 83.7% and 32.1% higher area, respectively. This increase is a direct consequence of our hardening strategy that prioritizes SET and MET suppression by applying transistor redundancy. Nevertheless, this trade-off results in significantly lower PoF values, making the overhead acceptable for safety-critical applications such as aerospace or military-grade circuits.

The limitations of the proposed method can be summarized as: 1) Although in safety-critical applications like aerospace applications, reliable behavior outweighs area and power overheads [3, 4]—making our approach’s trade-off acceptable—the hardening scheme may be constrained in designs with the tight area, power, or other design-parameter budgets. 2) Our evaluation is limited to 45nm planar bulk CMOS INV, NOR, and NAND standard cells; extending the method to advanced process technologies (e.g., FinFET, etc.) or other standard cells will require employing similar additional device- and circuit-level simulations, which is considered future work. 3) The hardened cell designs should be incorporated into standard cell libraries to be used in the digital design flow, which introduces integration efforts.

6. Conclusion

This paper presented a comprehensive investigation into the vulnerability and hardening of combinational standard cells against particle-induced faults through device-level and circuit-level analyses. By leveraging 3D-TCAD simulations, we characterized the effects of particle tracks, strike angles, and charge sharing on standard cells such as INV, NOR, and NAND. The extracted insights led to the design of hardened cells with high transient fault tolerance. Key findings include the identification of critical LET values and angular ranges that significantly influence charge-sharing dynamics and fault susceptibility. Circuit-level simulations further quantified the probability of failure for various cell configurations, and experiments demonstrated that the NOR cell exhibits higher resilience compared to NAND. Additionally, the analysis of adjacent cell effects highlighted the importance of cell placement and design optimization to minimize multiple-event transients. The proposed approach provides a practical methodology for reliability-aware circuit design, offering valuable guidance for selecting and configuring standard cells in mission-critical applications. Future work will explore cross-layer strategies that integrate layout-level and architectural techniques to further enhance the robustness of digital circuits against transient faults.

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Table 1. Ions used in 3D-TCAD simulations

Table 2. Particle track in PMOS transistors of std. cells (μm)

Table 3. Particle track in NMOS transistors of std. cells (μm)

Table 4. Most disruptive angle for adjacent cells

Table 5. Collected charge in single cell (fC)

Table 6. Possibility of occurrence for different single event multiple transients in experiments

Table 7. PoF of single standard cell

Table 8. Most sensitive zone of each cell and its probability of failure (%)

Table 9. Probability of failure (%) for the proposed cells vs the basic design

Table 10. Comparison of the proposed method with two cell hardening methods

Fig. 1. The 3D Inverter model used in 3D-TCAD simulations

Fig. 2. Simulation setup example of cell adjacency placement; a) identical-type adjacent cells, b) non-identical adjacent cells (INV cell in the center)

Fig. 3. The side view of striking particles with different angles to a bulk semiconductor process (the N implants are shown in dark orange and the P implants are shown in dark blue)

Fig. 4. Collected charge in adjacent cells when particles strike the center cell in standard cells under various LET values and strike angles: a) 0°, b) 30°, c) 60°, and d) 80°

Fig. 5. Most common pattern in charge sharing scenario (Victim cell is in the center) from the most probable (a) to the least probable pattern (f)

Fig. 6. Probability of failure calculated for adjacent cells

Fig. 7. The hardened INV cell design

Fig. 8. SET filtering capability of the proposed hardened INV cell

Fig. 9. The hardened NOR design

Fig. 10. SET filtering capability of the proposed hardened NOR cell

Fig. 11. The hardened NAND design

Fig. 12. SET filtering capability of the proposed hardened NAND cell

Table 1.

Ion	LET (MeV·cm ² /mg)
Si	9.8
Kr, Ar	48, 46.9
Bi, Xe	98.2, 100
He, U	143, 150

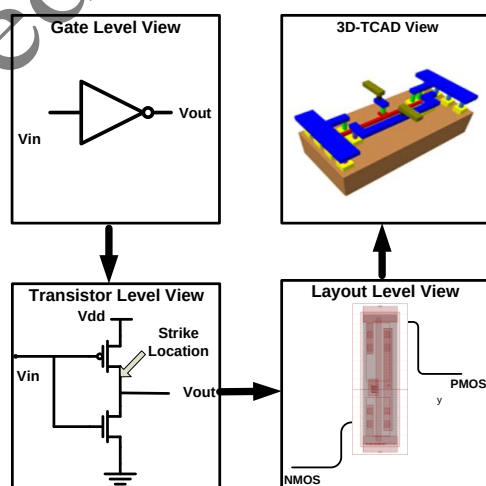


Fig. 1.

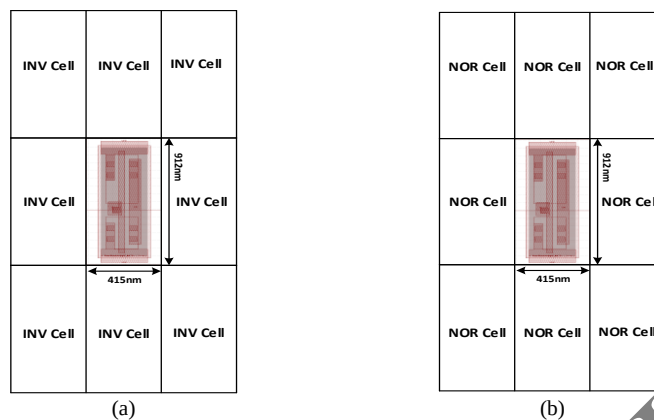


Fig. 2.

Table 2.

<i>LET</i> (MeV.cm ² /mg)	<i>Around Center</i>	<i>NAND</i>	<i>NOR</i>	<i>INV</i>
10	<i>NAND</i>	2.2101	1.1022	1.6125
	<i>NOR</i>	0.9554	0.7554	0.8988
	<i>INV</i>	1.8779	1.0112	1.8554
50	<i>NAND</i>	3.4921	1.8321	2.3656
	<i>NOR</i>	1.6554	1.3930	1.5215
	<i>INV</i>	2.2321	1.8665	2.2951
100	<i>NAND</i>	3.9930	2.1255	2.2364
	<i>NOR</i>	1.6239	1.5928	1.4655
	<i>INV</i>	2.4648	2.2354	2.6986
150	<i>NAND</i>	4.3124	2.7554	3.1322
	<i>NOR</i>	2.6544	1.9554	2.5878
	<i>INV</i>	3.1245	2.7898	3.1255

Table 3.

<i>LET</i> (MeV.cm ² /mg)	<i>Around Center</i>	<i>NAND</i>	<i>NOR</i>	<i>INV</i>
10	<i>NAND</i>	1.4565	1.9221	1.5455
	<i>NOR</i>	0.8002	1.1224	0.9887
	<i>INV</i>	1.8544	1.2654	1.8477
50	<i>NAND</i>	1.9856	2.4913	1.9977
	<i>NOR</i>	1.2927	1.6422	1.5935
	<i>INV</i>	2.1927	1.6294	2.0783
100	<i>NAND</i>	1.7334	2.3664	1.8311
	<i>NOR</i>	1.7899	1.9131	1.8321
	<i>INV</i>	2.3315	2.0252	2.4757
150	<i>NAND</i>	2.0112	2.4454	1.9233
	<i>NOR</i>	2.1221	2.5544	2.2211

	INV	3.0002	2.8221	3.2214
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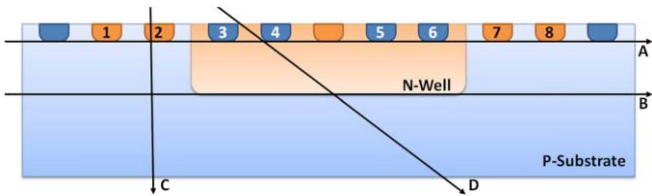


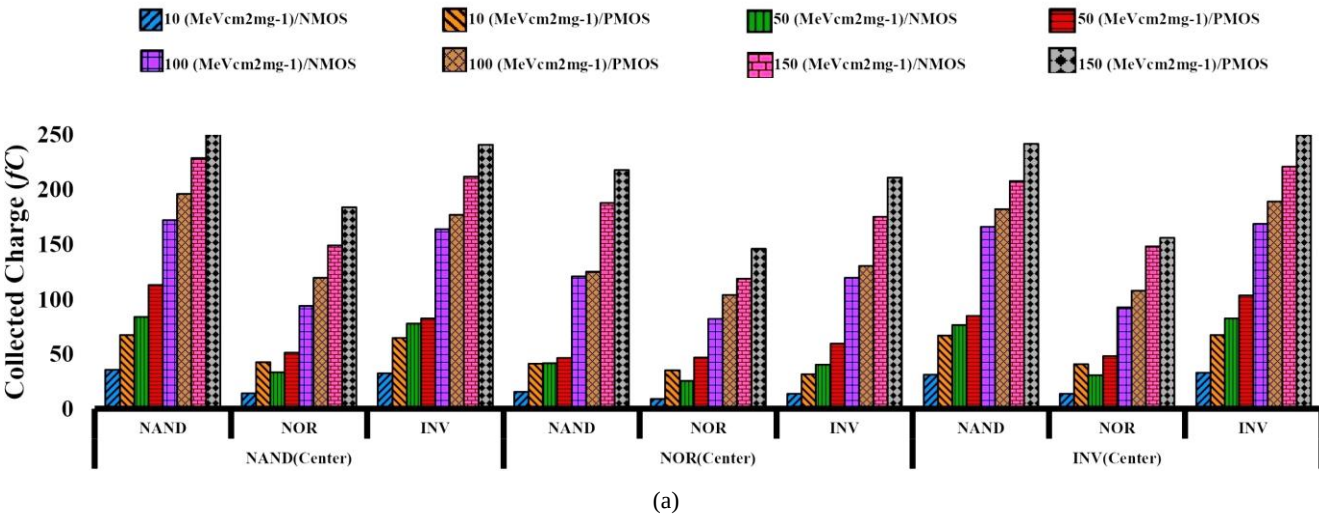
Fig. 3.

Table 4.

Center \ Around	NAND	NOR	INV
	NAND	NOR	INV
NAND	55°	60°	55°
NOR	60°	60°	55°
INV	55°	60°	55°

Table 5.

LET (MeV.cm ² /mg)	NMOS			PMOS		
	NAND	NOR	INV	NAND	NOR	INV
10	83.2	90.1	73.2	109.4	95.3	101.6
50	158	161	143.7	188	174	183
100	229	225	218	278	261	275
150	344	348	337	412	383	393



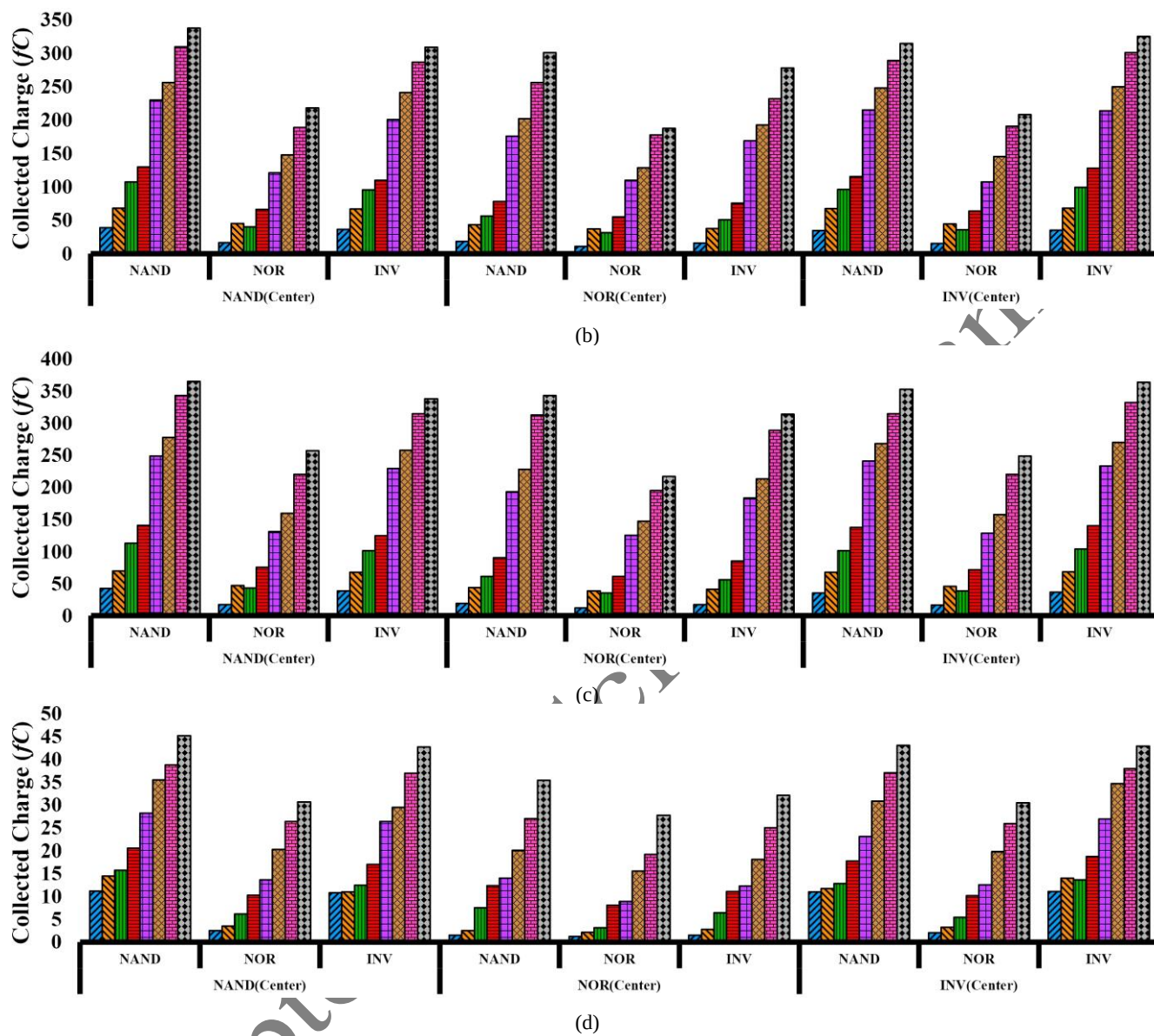


Fig. 4.

Table 6.

Single Event Multiple Transient	Possibility of Occurrence (%)
Single-cell	62.0
Two adjacent cells	33.0
Two non-adjacent cells	2.8
Three adjacent cells	1.7
Three non-adjacent cells	0.3

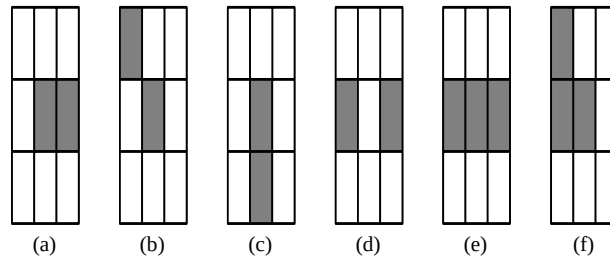


Fig. 5.

Table 7.

Standard Cell Name	<i>NAND</i>	<i>NOR</i>	<i>INV</i>
Probability of Failure (%)	93	87	89

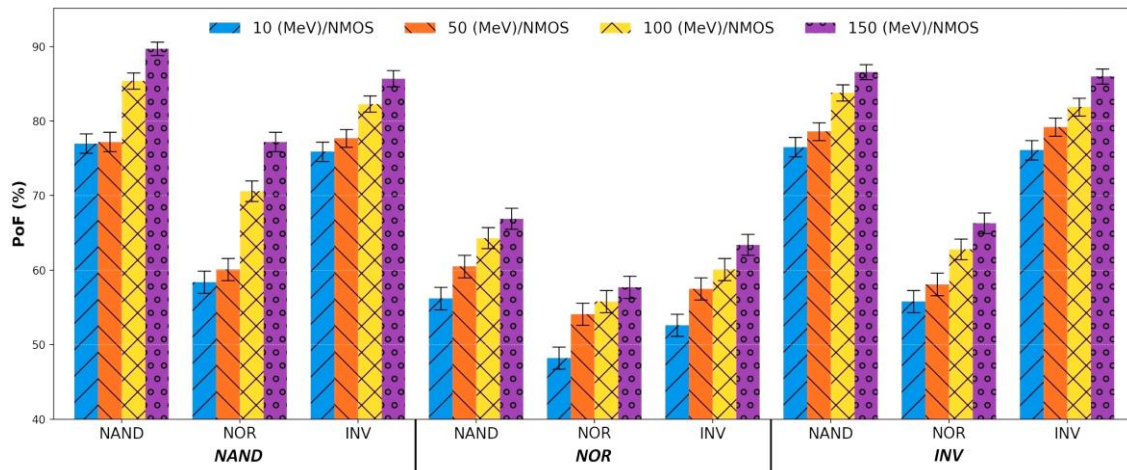


Fig. 6.

Table 8.

	Sensitive Nodes	Probability of Failure
NOR	Zone 1	82%
	Zone 2	91%
NAND	Zone 1	93%
	Zone 2	89%
INV	Zone 1	92%

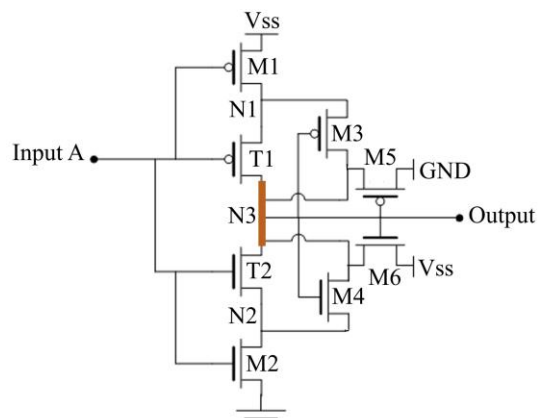


Fig. 7.

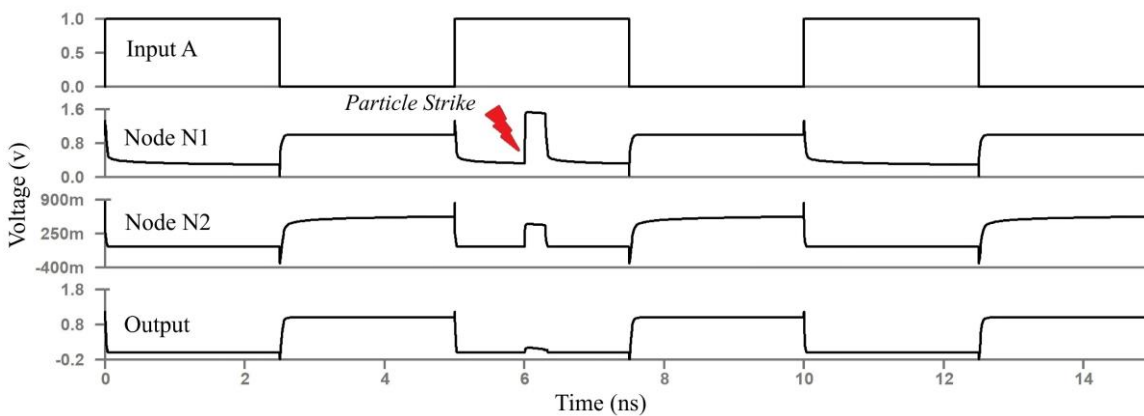


Fig. 8.

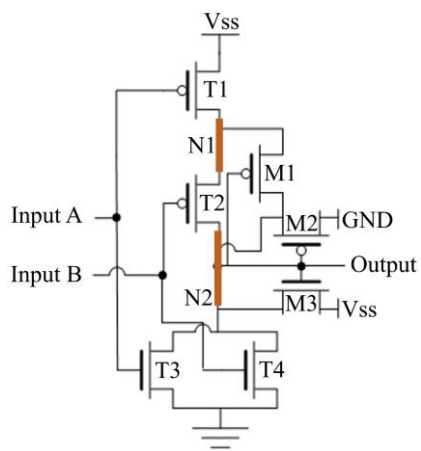


Fig. 9.

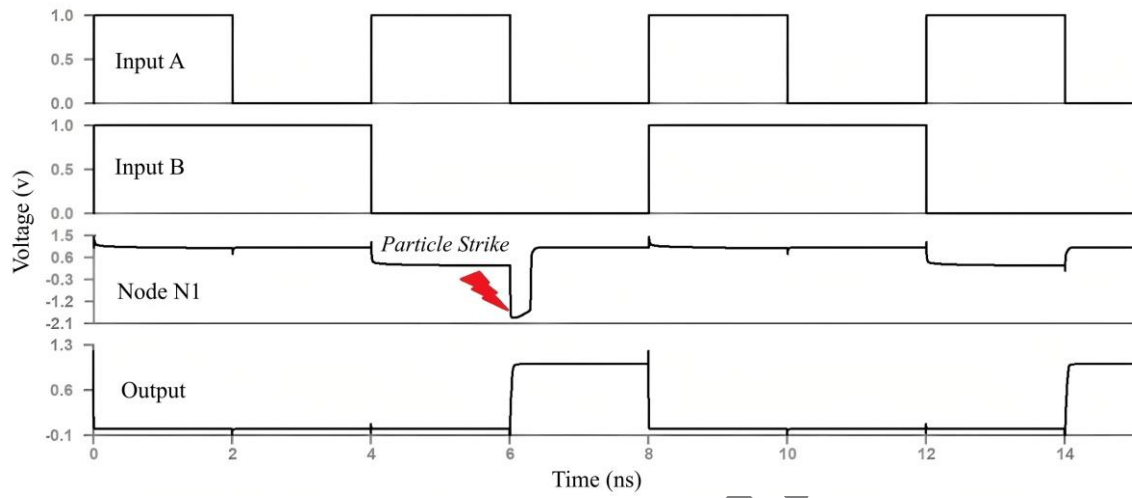


Fig. 10.

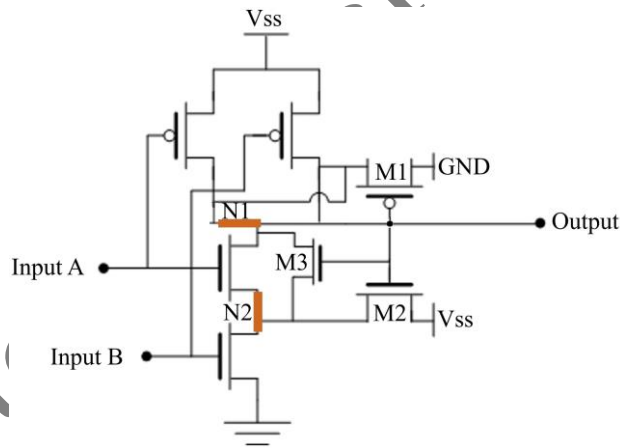


Fig. 11.

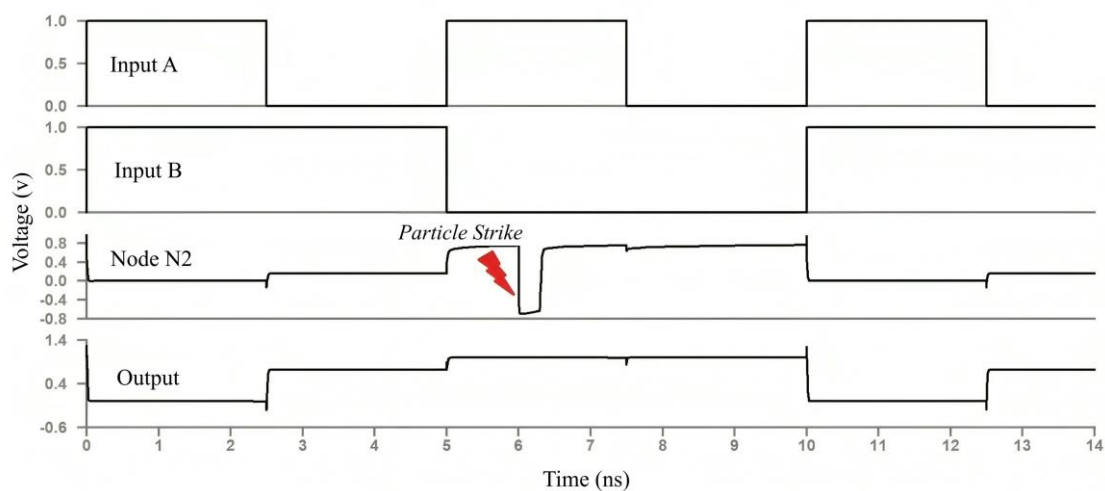


Fig. 12.

Table 9.

<i>LET</i> (MeV.cm ² /mg)	<i>INV</i>		<i>NOR</i>		<i>NAND</i>	
	<i>Basic</i>	<i>Hardened</i>	<i>Basic</i>	<i>Hardened</i>	<i>Basic</i>	<i>Hardened</i>
10	88.5	0.001	86.1	0.001	87.3	0.001
50	90.5	0.001	87.0	0.001	88.9	0.001
100	93.2	1.1	88.4	0.3	92.2	0.72
150	97.2	1.8	91.2	1.0	96.8	1.2

Table 10.

Method	Cell	PoF (%)	Delay (ps)	Area (um ²)	Power (uw)
This work	INV	1.8	6.7	1.719	7.85
	NOR	1	3.6	1.463	6.96
	NAND	1.2	5.3	1.434	6.78
Work [21]	INV	18.9	12.2	0.665	4.15
	NOR	12.1	8.1	0.917	4.56
	NAND	13.4	7.9	0.931	4.85
Work [22]	INV	22.8	9.7	0.832	4.45
	NOR	18.7	5.8	1.331	5.12
	NAND	23.2	6.1	1.331	5.32

Author Biography

Ali Zarei is currently working toward a Ph.D. degree in computer engineering at Amirkabir University. He is now a member of the Design and Analysis of Dependable Systems (DADS) at the computer engineering department, Amirkabir University of Technology. His research interests include dependable systems, fault-tolerant systems, embedded systems, and low power VLSI circuits.

Hamid Reza Zarandi received the BSc, MSc, and PhD degrees all from the Department of Computer Engineering at the Sharif University of Technology, Iran, in 2000, 2002, and 2007, respectively. He is currently an associate professor with the Department of Computer Engineering at Amirkabir University of Technology (Tehran Polytechnic). His research interests include dependability evaluation using fault injection techniques, fault-tolerant computing, dependable computer architecture, and high-performance computing, on which he has published more than 100 referred conferences and journal papers. He established the “Design and Analysis of Dependable Systems (DADS)” laboratory at Amirkabir University, in 2007.

Amir Mohammad Hajisadeghi received the M.Sc. and Ph.D. degrees in computer engineering from Amirkabir University of Technology (Tehran Polytechnic), Iran, in 2018, and 2024, respectively. He is currently a researcher at the Design and Analysis of Dependable Systems (DADS) laboratory at the computer engineering department, Amirkabir University of Technology. His research interests include computer architecture, reliable system design, emerging memory technologies, and in-memory computing.