Negative Capacitance Gate-Stack Structure with HfO_2 Ferroelectric Layer for Improving Digital Performance of the Field Effect Diodes

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Abstract: In this paper, a negative capacitance gate-stack field effect diode (FED) with reduced subthreshold slope, increased on-state current (I_{ON}) and decreased off-state current (I_{OFF}) has been proposed. By using the HfO_2 ferroelectric layer following by the SiO_2 dielectric layer under the two gates of the device, a negative capacitance structure is created in the gate-stack. Therefore, the gate control over the channel is strengthened which improves the short channel effects and digital performance of the proposed device. Comparing to the conventional FED, the negative capacitance structure in the gate-stack of the proposed FED amplifies the voltage amplification in the channel which causes larger induced carrier concentration for the same applied gate voltages. As the result, smaller I_{OFF}, higher I_{ON}, higher I_{ON}/I_{OFF} ratio and smaller subthreshold slope are achieved in the proposed FED. In addition, the proposed device exhibits smaller gate capacitance, smaller gate delay time and smaller energy delay product which provide better switching performance with less energy consumption.

Keywords: Ferroelectric; Field effect diode; Negative capacitance; Subthreshold slope

1. Introduction

Rapid CMOS technology scaling has focused on exploring alternative devices such as field effect diode (FED) with more suppressed short channel effects (SCEs). The structure of the conventional FED has been represented in Fig. 1a [1] which is similar to the MOSFET except some differences. The channel is intrinsic or low doped and there are n+ and p+ regions under the source and drain sides. The device has two gates that modulate the charge concentration in the channel. By applying opposite polarity potentials to the gates with respect to the source, holes and electrons are accumulated under the gates, so a diode is formed in the channel between the source and drain, in

either reverse- or forward- biased condition.

Despite of the current saturation in MOSFET, the current in FED faces no pinch off and it increases exponentially with increasing of drain-source bias [1]. FED shows higher on-state current (I_{ON}), lower off-state current (I_{OFF}), lower subthreshold slope and higher I_{ON}/I_{OFF} than MOSFET [2]. FED has been used in many high-speed analog and digital circuits and systems, such as electrostatic discharge protection [3-4], memory cells [5-6] and other digital and analog circuits [7-8].

The conventional FED suffers from high I_{OFF} when down scaling to sub 100nm channel length. This drawback is due to the injection of minority carriers from the n+ and p+ regions to the channel in the off-state. For reducing I_{OFF}, small n+ and p+ regions (called reservoirs) were added to the source and drain sides, so the amount of the injected minority carriers to the channel were decreased in the off-state [2]. For making more feasible fabrication and improving the properties of the introduced FED in [2], the reservoirs were extended to the entire of the source/drain sides [9]. This FED structure provided higher I_{ON}/I_{OFF}, lower gate delay time and smaller Subthreshold slope with much feasible fabrication process [9]. Continuing the research in this field led to introduce modified structures for FED that exhibited improved I_{ON}/I_{OFF} ratio, Subthreshold slope and better performance. In [10], three dimensional FED structure was proposed in which the reservoirs were implemented laterally and the channel was composed of four region from source to drain. In [11], similar to the double-gate MOSFETs, double-gate FED was introduced which improved electrical performance of the device. In [12], a silicon on raised insulator FED was introduced to improve performance of the FED by using an oxide insulator pocket layer in the channel. In [13], a hetrostructure channel structure was implemented by using Si/Ge regions under the two gates of the FED for improving I_{ON}/I_{OFF}. In [14], a graphene-channel FED was proposed to improve the I_{ON}/I_{OFF} ratio, while it suffers from early channel pinch-off at small drain-source voltage. By embedding doped pockets in the source/drain ends of the channel, the energy delay product of a nanoscale FED was improved [15]. In [16] two layers of wide-bandgap material have been embedded at the source/drain sides of the channel of FED which creates potential barriers for lowering the injection of the additional carriers to the channel in the OFF-state. Among FED structures introduced above, much attention has been paid to FED structure of [9], since it has compatible structure and fabrication process with MOSFET. In FED structure of [9] represented in Fig. 1b, the dielectric SiO_2 has been used in the gate-stack, and for ease of comparison, hereafter this structure is called the dielectric gate-stack FED (DEFED).

Utilizing the negative capacitance (NC) effect observed in ferroelectric materials when used as

the gate-stack has theoretically and experimentally proven improvement in I_{OFF}, I_{ON} and Subthreshold slope of MOSFETs [17-20]. In the NC gate-stack, a ferroelectric layer is added in series with a dielectric layer of the gate. By applying the external potential to the gate, the process of charge transfer in the ferroelectric layer slows down and a transient reduction in the dropped voltage on the ferroelectric material is observed. The charge will be increased as the potential is decreased, resulting in NC gate. The ferroelectric layer amplifies the applied gate voltage which induces more channel charges and causes higher current flow in the channel comparing to the MOSFET. Consequently, Subthreshold slope is achieved at smaller gate voltages [21]. The NC gate-stack can be implemented by adding simple steps to the fabrication process of the MOSFET for deposition of the ferroelectric layer in the gate-stack [17]. The NC gate-stack has attracted much attention for adopting in the MOSFET circuit design technology [22-25].

Some materials like High-k HfO_2, ZrO_2, TiO_2, Lead Zirconate Titanate (PZT), Barium Titanate and polar-phase polymer P(VDF-TrFE) have shown ferroelectricity [26-27]. High-k materials can reduce leakage current when being used in the MOS contacts [28]. P(VDF-TrFE) has large remanent polarization, simple device fabrication process and device flexibility [29-30]. However, balancing large polarization and FET charge density imposes thick insulator layer for some ferroelectric materials such as PZT, Barium Titanate, ZrO_2 and TiO_2. This is a challenge as these materials are not compatible to the advanced scale CMOS technology. In addition, contamination by heavy metals in the manufacturing process is a big challenge in this case too [31]. Among high-k materials, HfO_2 is a good candidate for using in the insulator layer of the MOS contact, due to its advantages like high dielectric constant, large band gap, high breakdown electric field and thermal stability [28]. HfO_2 film can be implemented in nanometer scale which is very compatible to the fabrication process of MOSFETs [31-32]. However, its low crystallization temperature is a drawback which causes increment in the leakage current of the crystal boundary paths and impurity getters during processing. Growing high quality HfO_2 layer can be done by a number of deposition techniques [28].

In this manuscript, increasing of the I_{ON}/I_{OFF} and decreasing of the subthreshold slope has been achieved in the FED by utilizing the NC gate-stack. In order to form the NC structure, HfO_2 as the ferroelectric material has been used in series with the SiO_2 as the dielectric material in the gates of FED. By exploiting the benefits of the NC structure, the gate control over the channel will be strengthened which improves short channel effects and digital performance of the proposed device. Simulation results achieved by using ATLAS TCAD device simulator reveals that comparing with

DEFED of [9] (in which only the SiO_2 as the dielectric layer is under the gates), the proposed NCFED provides smaller subthreshold slope especially for shorter gate lengths and higher I_{ON}/I_{OFF}. Besides improving the digital performance, the proposed NCFED has simple fabrication process, similarly to that of the MOSFET, with extra simple steps for implementing the NC gate-stack. Finally, effect of different thicknesses of the ferroelectric layer on electrical parameters of the proposed device will be investigated.

2. Brief description of the negative capacitance phenomenon in MOSFETs

The concept of the negative capacitance (NC) was firstly used to lowering the Subthreshold slope value of the conventional MOSFETs below the classical limit [19]. In this regard, the ferroelectric material was used in the gate oxide of MOSFET (see Fig. 2) which experimentally, exhibited reduction in Subthreshold slope and I_{OFF} [17-19]. When the applied gate voltage drops on the ferroelectric material, the dipole moment in the ferroelectric material makes polarization which decelerates the charge transfer by the applied voltage. Consequently, the dropped voltage on the ferroelectric layer reduces transiently, which results in the so-called negative capacitance behavior in the ferroelectric layer [21]. NC has an unstable state, and adding a series dielectric layer to the ferroelectric layer makes it be stabilized [18].

In a conventional MOSFET, the applied gate voltage, V_G, drops on the dielectric and the semiconductor layers. The charge density in the channel is expressed as $Q = C_S \times \varphi_S$ where C_S is the semiconductor capacitance and φ_S is the dropped voltage on the semiconductor layer. In contrast, in NC MOSFET, the gate capacitance, C_{OX}, is negative. The charge on the ferroelectric layer must be equal to Q. V_G drops on the ferroelectric and on the semiconductor layers. Due to the existence of NC in the ferroelectric layer, φ_S is larger than V_G which is a voltage amplification phenomenon in the NC MOSFET. So, more charges are induced in the channel comparing to the conventional MOSFET. This means that accumulation of the same amount of Q in C_{OX} and C_S needs smaller gate voltage in the NC MOSFET. The drain current is proportional to the induced charge in the channel. So, comparing with the conventional MOSFET, for the same applied gate voltage, higher amount of the current can be flowed in the channel and consequently, smaller Subthreshold slope can

be achieved at smaller applied gate voltage in the NC MOSFET [21].

Ferroelectric materials inherently exhibit hysteresis behavior in their dipole polarization by changing of the intensity of the internal electric field [33]. In the equilibrium condition (i.e. without existence of the external voltage), dipoles have random orientation. By applying the external voltage, the produced internal electric field orients the dipoles parallel to its direction, which finally ends at parallel orientation of all of dipoles (known as saturation polarization). Bound charges are accumulated at the surface of the ferroelectric layer when switching of the polarization occurs which can exceed the free charges produced by the external voltage. This phenomenon can amplify the surface potential of the channel. Hysteresis of the ferroelectric layer is dependent on its thickness [21]. The detailed description of fundamental aspects in operation of the NC MOSFETs can be found in [17-22, 32].

Mathematically, the potential amplification in the NC gate-stack for improvement of the subthreshold slope and the on-state current, can be described as follows. The subthreshold slope, SS, is defined as [21]

$$SS = \left(\frac{\partial \left(\log_{10} I_D \right)}{\partial V_{GS}} \right)^{-1} = \left(\frac{\partial \left(\log_{10} I_D \right)}{\partial \psi_S} \right)^{-1} \cdot \frac{\partial V_{GS}}{\partial \psi_S} = \left(\mathrm{Ln}(10) \ \frac{kT}{q} \right) \cdot \frac{\partial V_{GS}}{\partial \psi_S} \tag{1}$$

where

$$I_D \propto \exp\left(\frac{q\psi_S}{kT} \right) \ , \quad m = \frac{\partial V_{GS}}{\partial \psi_S} = 1 + \frac{C_S}{C_{Ins}} \tag{2}$$

In (1) and (2), V_{GS} and ψ_S are the applied gate voltage and the channel surface potential respectively, k is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, I_D is the channel current, C_S is the semiconductor depletion capacitance, C_{Ins} is the gate-stack (insulator) capacitance and m is called the body factor. In a dielectric gate-stack, the insulator capacitance is positive. Therefore, m is always greater than 1, making SS be greater than its limit value $\left(kT/q \right) \mathrm{Ln}(10)$ (or equally 60mV/dec at room temperature).

By using the NC gate-stack, $C_{Ins} < 0$ and m becomes less than 1, allowing the possibility of lower SS than 60mV/dec. In addition, regarding (2), $m < 1$ means that an small change in V_{GS} makes larger change in ψ_S; so the voltage is amplified in the semiconductor channel, resulting in larger charge

accumulation under the gate and higher channel current.

3. Proposed Negative Capacitance gate-stack FED

The structure of the proposed NC gate-stack FED (called NCFED hereafter for simplification) has been represented in Fig. 3. In order to reduce the I_{OFF}, regions with opposite polarity charges have been extended over the reservoir regions at the source and drain sides, i.e. n^+ over the p^+ at the source side and p^+ over the n^+ at the drain side as suggested in [9]. The gates near the source and drain sides are named GS and GD, respectively and they are biased with respect to the source. The gate-stack has the negative capacitance structure at where the HfO_2 layer as the ferroelectric has been deposited on GS and GD and followed by the SiO_2 as the dielectric layer.

For $V_{DS} > 0$, if $V_{GS} > 0$ and $V_{GD} < 0$ are applied to GS and GD respectively, the n^+npp^+ region is formed in the channel from the source to the drain. In this condition, the np region formed under the GS-GD gates acts as a forward biased diode. This is called the on-state operation. In contrast, for $V_{DS} > 0$, if $V_{GS} < 0$ and $V_{GD} > 0$ are applied to GS and GD respectively, the n^+pnp^+ region is formed in the channel from source to drain. In this condition, the pn region formed under the GS-GD gates acts as a reverse biased diode. This is called the off-state operation. The p^+ region at the source side and n^+ region at the drain side reduce the amount of injected minority carries into the channel in the off-state, resulting in strengthening the pn region under the GS-GD gates and thereby, decreasing the I_{OFF}.

4. Fabrication Process

The NCFED can be fabricated similarly to the fabrication process of the common MOSFETs with simple extra steps for HfO_2 deposition and two steps of metallization. Fabrication challenges are similar to those for MOSFETs. The brief fabrication steps have been represented in Fig. 4. First, a lightly doped Si layer on an insulator substrate which forms an SOI structure is implemented as the active channel. Then two n^+ regions and two p^+ regions are created separately, by using ion implantation. Next, SiO_2 is thermally deposited to wrap the channel. The extra oxide is etched to reach the n^+ and p^+ regions. The etching process should be controlled to maintain the desired SiO_2 thickness under the gate contacts. Then, metallization is performed by thermal deposition method for forming source and drain contacts and inner GS and GD plates. This process should be controlled to

minimize the asymmetric contacts and reduce the contact parasitic resistances. In the next step, HfO_2 is deposited to wrap the channel. The extra HfO_2 layer is etched to reach the source and drain contacts. Again, the etching process should be controlled to maintain desired HfO_2 thickness on the inner GS and GD plates. Finally, metallization is done to extend the source and drain contacts and form the top GS and GD contacts. The main challenge in the final metallization step is maintaining true alignment of the inner and top GS and GD plates in the NC gate-stack and preventing from undesired overlap of the top GS and GD contacts on inner GS and GD plates.

5. Simulation Results and Discussion

The NCFED is simulated by ATLAS simulation software [34] and compared with the DEFED. In simulation, the Fermi-Dirac distribution function was used. Carrier generation and recombination was considered by employing the Shockley–Read–Hall recombination model with concentration-dependent lifetimes and Auger recombination model. Velocity saturation effects were included in simulation by activating the parallel and perpendicular electric-field-dependent and concentration dependent mobility models. The highly doped n^+ and p^+ regions at the source and drain sides shift the conduction and valance band edges which in turn affects the bipolar currents in the devices. This phenomenon was included in simulation by activating the bandgap narrowing model. The parameters for Si, SiO_2 and HfO_2 at 300K have been selected with respect to the values recommended in [34]. Other geometrical and physical parameters for simulation have been given in Table 1.

It is useful to note that the geometrical dimensions of the proposed devices are in the classical range, i.e. channel length longer than 20nm and channel thickness thicker than 10nm. As explained in [35], for the classical dimensions, the carrier quantum confinement at the surface and quantum effects can be ignored, and the potential can be achieved by using the Poisson equation and drift-diffusion current model in the simulator. The simulator was first calibrated with the experimental results of the fabricated DG MOSFET represented in [36]. The fabricated sample has channel length of 60nm and channel thickness of 25nm which are in the classical range. Fig. 5 compares the simulation results achieved by using the mentioned models and the fabrication result. Good agreement between the results reveals the validity of the adopted simulation method.

As explained in [37], the values of the remanent polarization $P_r=9\mu C/cm^2$ and the coercive field $E_C=1MV/cm$ are considered as the reference values for the ferroelectric HfO_2. With these values, if

the HfO_2 thickness is chosen in the range of 2 to 5nm, there will be no hysteresis in the polarization-electric field dependency in the NCMOS channel and consequently, the voltage amplification does not face any hysteresis. For thicker HfO_2 thickness, the polarization-electric field dependency will show hysteresis. Based on this explanation, in this manuscript, the thickness of the HfO_2 layer was chosen in the range of 2 to 5nm with P_r=9μC/cm^2 and E_C=1MV/cm, in order to prevent from appearance of the hysteresis. Also, for HfO_2, the spontaneous polarization P_S=9.4μC/cm^2 and the dielectric constant ε_r=32 were considered.

For SiO_2 and Si, the parameters at 300K have been selected with respect to the recommended values given in [34]. Other simulation parameters were given in Table 1.

Fig. 6a represents the polarization-electric field dependency on the thickness of the HfO_2 layer in the NCFED which reveals that the polarization-electric field dependency has no hysteresis for the HfO_2 thickness in the range of 2 to 5nm and applied gate voltage of ±2V. For thicker HfO_2 (i.e. 6nm and above), the curve shows hysteresis.

Considering Fig. 2, the in series ferroelectric (HfO_2) and the dielectric (SiO_2) layers make in series ferroelectric and dielectric capacitances, C_{FE} and C_{DE}, respectively. So, the same amount of charge Q accumulates in each of them. The total energy of the series capacitors (U_{Total}) is the sum of the energies of the ferroelectric (U_{FE}) and the dielectric (U_{DE}) capacitors, i.e. $U_{total}(Q)=U_{FE}(Q)+U_{DE}(Q)$. If C_{FE} is negative and $|C_{FE}|>C_{DE}$, then the equivalent gate insulator capacitance $C_{FE-DE}=\left(C_{FE}^{-1}+C_{DE}^{-1}\right)^{-1}$ can be larger than C_{DE} [38]. C_{FE-DE} stabilizes at a charge Q that minimizes the total energy of the system. Considering the energy-charge relation for a capacitance, i.e. $C=\left(d^2U/dQ^2\right)^{-1}$, at a given Q, if the energy curve U is flatter, then C_{FE-DE} is larger than C_{DE}. Flatter energy curve resembles that the ferroelectric-dielectric stack behaves more like a dielectric and is stable. At steady state operation, the polarization (P) is nearly equal to Q. So, we can evaluate the stability of the ferroelectric-dielectric gate-stack by examining the flatness of the energy-polarization diagram. In addition, the total gate capacitance $C_G=\left(C_{OX}^{-1}+C_S^{-1}\right)^{-1}$, where $C_{OX}=C_{FE-DE}$ must be positive for having hysteresis free and stable operation [38]. In the DEFED, the gate-stack is only a dielectric layer and $C_{OX,DEFED}=C_{DE}$. In the proposed NCFED, the gate-stack

is serial connection of the ferroelectric-dielectric layers and $C_{OX,NCFED} = C_{FE-DE}$. The total gate capacitances for DEFED and NCFED are $C_{GS,DEFED} = \left(C_{OX,DEFED}^{-1} + C_S^{-1}\right)^{-1}$ and $C_{GS,NCFED} = \left(C_{OX,NCFED}^{-1} + C_S^{-1}\right)^{-1}$, respectively. Regarding the above explanation, it can be concluded that $C_{OX,NCFED} > C_{OX,DEFED}$, resulting in $C_{GS,NCFED} < C_{GS,DEFED}$ which will be demonstrated by simulation results later in Fig. 10.

The energy-polarization diagram of the HfO_2-SiO_2 gate-stack capacitance of the proposed NCFED for $V_{GS} = \pm 2\text{V}$ and HfO_2 thickness of 5nm is represented in Fig. 6b. The energy landscape is nearly flat at its minimum value without a considerable minimum point, so the gate-stack in the proposed NCFED is stable.

Fig. 6c represents the surface potential–gate voltage curve for the proposed NCFED for HfO_2 thickness of 5nm. At each point on the curve, the surface potential has larger value than the gate voltage. Regarding (2), $\partial\psi_S / \partial V_{GS}$ is positive, resulting in $m < 1$ and revealing occurrence of voltage amplification.

Fig. 7 represents the surface carrier concentrations of the NCFED and DEFED along the channel in the off-state. By applying $V_{DS} > 0$, $V_{GS} < 0$ and $V_{GD} > 0$, the n^+pnp^+ region is formed in the channel from source to drain which creates a reverse-biased pn junction under the GS-GD gates and at the interface of p and n regions, carrier recombination forms a depletion region. So, both of DEFED and NCFED go to the off-state. In the off-state, the excess minority electrons and holes are injected into the channel from the n^+ region at the source and p^+ region at the drain, respectively. These injected carriers increase the electron and hole concentrations under GS and GD, respectively, resulting in weakening the reverse-biased behavior of the pn junction, thereby, increasing I_{OFF}. In contrast, the p^+ and n^+ reservoirs at source and drain reduce the concentration of the injected excess minority carriers. Therefore, the total I_{OFF} is decreased.

By using the NC gate-stack in the NCFED, voltage amplification at the channel surface helps increasing of the carrier concentration under GS and GD. As illustrated in Fig. 7, under GS, the net electron concentration is smaller and the net hole concentration is larger in NCFED. Under GD, the net electron concentration is larger and the net hole concentration is smaller in NCFED. This carrier distribution profile forms stronger reverse-biased np region with wider depletion width under the

GS-GD gates, resulting in smaller I_{OFF} in NCFED will be represented in the next figures.

Fig. 8 represents the surface carrier concentrations of the NCFED and DEFED along the channel in the on-state. By applying $V_{DS} > 0$, $V_{GS} > 0$ and $V_{GD} < 0$, the n^+npp^+ region is formed along the channel which creates a forward-biased np junction under the GS-GD gates, so both devices go to the on-state. In the on-state, excess minority electrons and holes are injected into the channel from the n^+ region at source and p^+ region at drain, respectively. These injected carriers increase the electron and hole concentrations under GS and GD, respectively, resulting in strengthening the forward-biased behavior of the np region.

By using the NC gate-stack in the NCFED, voltage amplification at the channel surface helps increasing of the carrier concentration under GS and GD. As illustrated in Fig. 8, under GS, the net electron concentration is larger and the net hole concentration is smaller in NCFED. Under GD, the net hole concentration is larger and the net electron concentration is smaller in NCFED. This carrier distribution profile forms stronger forward-biased np region with thinner depletion width under the GS-GD gates, resulting in larger I_{ON} in NCFED will be represented in the next figures.

Fig. 9a compares I_{OFF} of NCFED with DEFED for different channel lengths. Because of positive V_{DS}, the longitudinal resultant electric field forces injection of extra electrons from the n^+ reservoir at the source into the p region under GS and injection of extra holes from the p^+ reservoir at the drain into the n region under GD. By shortening the channel length, intensity of the electric field is increased which causes increasing carrier injection from the reservoirs into the channel, which in turn, weakens the pn region. As the result, higher I_{OFF} will be produced at shorter gate lengths for both of the NCFED and DEFED. For shorter channel lengths, I_{OFF} of NCFED is slightly smaller than DEFED, while for longer channel lengths, it becomes much smaller in NCFED. Regarding fig. 7, by using the NC gate-stack in the proposed NCFED, the voltage amplification at the channel surface helps increasing of the carrier concentration under GS and GD. Therefore, stronger reverse pn region is formed under GS and GD, which provides smaller I_{OFF} in NCFED.

Fig. 9b compares I_{ON} of NCFED with DEFED for different channel lengths. Because of positive V_{DS}, the longitudinal resultant electric field forces injection of extra electrons from the n^+ reservoir at the source into the n region under GS and injection of extra holes from the p^+ reservoir at

the drain into the p region under GD. Therefore, stronger forward biased np region is formed in the channel. The shorter gate length, the more intensive electric field and consequently, the stronger favorable carrier injection from the reservoirs into the channel in the on-state. Thereby, higher I_{ON} is produced at shorter gate lengths for both of the NCFED and DEFED. For longer channel lengths, the area where the minority carriers are injected into from source and drain reservoirs becomes wider and carrier recombination rate is increased, resulting in wider depletion region in the channel under the GS-GD gates which decreases I_{ON} for both devices. For all channel lengths, I_{ON} is larger in NCFED, and the difference slightly is increased as the channel becomes longer. Again, this behavior corresponds to the NC gate structure in NCFED. Regarding Fig. 8, voltage amplification helps increasing of the carrier concentration under GS and GD. Therefore, stronger forward np region is formed under GS and GD and higher I_{ON} is produced in the proposed NCFED.

I_{ON} / I_{OFF} for NCFED and DEFED for different channel lengths has been represented in Fig. 9c. The behavior of I_{ON} / I_{OFF} can be inferred from Fig. 9a and Fig. 9b in which for shorter channel lengths, I_{OFF} of DEFED and NCFED is close together, resulting in close I_{ON} / I_{OFF}. In contrast, for longer channel lengths, NCFED represents smaller I_{OFF} and larger I_{ON} than DEFED, resulting in higher I_{ON} / I_{OFF} for NCFED.

As explained in [38-39] for NCFETs, as the gate is biased, an inner fringing electric field is created and penetrates into the device channel. Depending on the polarity of gate charge, different spatial distribution of the polarization in the ferroelectric layer along the channel for different gate lengths is achieved. This, in turn, makes different voltage drop across the ferroelectric layer, and consequently, different channel surface potential. For longer channel lengths, the inner fringing field does not affect the polarization and the gate capacitance remains negative. In contrast, for shorter channel lengths, the adverse effect is considerable, leading to the positive gate capacitance and reduced NC effect. Therefore, the level of the voltage amplification is reduced for shorter channel lengths. Similar discussion can be applied to the proposed NCFED. In the NCFED, for shorter channel lengths, the adverse effect of inner fringing electric field reduces the NC effect in each gate-stack. Consequently, increment in I_{ON} and decrement in I_{OFF} is less for shorter gate lengths in the NCFED.

The subthreshold slope for DEFED and NCFED for different channel lengths has been represented in Fig. 9d. Similar to the subthreshold behavior of the MOSFET, in a FED, as the gate length is increased, the subthreshold slope is decreased for both of DEFED and NCFED. For DEFED, the nominal value of the subthreshold slope at long enough gates reaches 60mV/dec. By forming NC-gate stack in NCFED, smaller gate biases are required than DEFED for obtaining the same on-state current, resulting in smaller subthreshold slope in NCFED. This is obvious in Fig. 9d in which the subthrehold slope of the NCFED is less than that of the DEFED for all gate lengths.

Again, in NCFED, the adverse effect of the produced inner fringing electric field reduces the NC effect and the level of the voltage amplification at shorter channel lengths which affects the subthreshold current. As represented in Fig. 9d, in the proposed NCFED, the subthreshold slope is higher for shorter gate lengths while it reaches beyond 60mV/dec for longer channel lengths. Also, the difference between the subthreshold slopes of the two devices is larger at shorter gate lengths, while it becomes less at longer gate lengths.

I_{ON} / I_{OFF} and subthreshold slope are of main parameters in evaluation of switching operation of the field effect devices. In Fig. 9c, for channel lengths below 80nm, I_{ON} / I_{OFF} ratio of DEFED and NCFED are slightly close together, while in Fig. 9d, the subthreshold slope of NCFED is much smaller than that of DEFED for the same channel lengths. On the other side, in Fig. 9c, for the channel lengths above 80nm, I_{ON} / I_{OFF} is considerably higher in NCFED, while in Fig. 9d, the subthreshold slope of the two devices are slightly close together for the same channel lengths. Therefore, it can be concluded that switching performance of the proposed NCFED is better than DEFED in overall, i.e. for shorter channel lengths, the subthreshold slope is effective, while for longer channel lengths, I_{ON} / I_{OFF} is effective.

Switching response of a metal-oxide semiconductor device can be evaluated by the time for charging the gate capacitance, C_G, to the voltage V_{DS} at a constant I_{ON}, and it is described by the gate delay time, τ as [9]

$$\tau = C_G V_{DS} / I_{ON} . \quad (1)$$

where

$$C_G = \partial Q_{Channel} / \partial V_{GS} . \quad (2)$$

where $Q_{Channel}$ is the total channel charge.

In Fig. 10a, C_G of DEFED and NCFED have been compared with each other for different channel lengths. Because of existence of the negative gate capacitance behavior and gate voltage amplification in NCFED, its extracted C_G is smaller than that of the DEFED for any channel lengths. Detailed explanation for this characteristics has been represented in description of Fig. 6.

Calculated gate delay times by using (1) for NCFED and DEFED have been compared with each other in Fig. 10b, which exhibits smaller gate delay time for NCFED. For the same gate biases and a given V_{DS}, due to the gate voltage amplification, with small changes in gate voltage, large changes in the induced charges occurs and thereby, larger I_{ON} and lower I_{OFF} are flowed in the channel of NCFED. Therefore, formation and removal of the conducting channel is faster as the gate voltage is changed which resembles smaller gate delay for the proposed NCFED comparing to DEFED.

It is obvious from Fig. 10b that as the channel length is increased, the gate delay is increased in both devices which limits their switching performance. However, the rate of increasing of the gate delay time is much lower in NCFED, resulting in less deterioration of switching performance in longer channel lengths for this device.

As another figure of merit, the energy delay product (EDP) gives an insight for evaluation of energy consumption of a switching device. Smaller EDP represents smaller energy consumption. EDP is estimated by [9]

$$EDP = \tau C_G V_{DS}^2 . \qquad (3)$$

Fig. 10c compares EDP of NCFED with DEFED for different gate lengths. Similar to the behavior of the gate delay time in Fig. 10b, EDP is smaller for NCFED for any gate lengths. For shorter channel lengths, the difference between EDP of the two devices is small, while it becomes larger for longer channel lengths. Therefore, it can be concluded that the NCFED offers lower power consumption in switching operation than DEFED.

Comparative comparison between the characteristics of DEFED, the proposed NCFED and NCFET for some channel lengths is given in Table 2. While DEFED has superior characteristics over the conventional MOSFET (as expressed in [9] in detail), using the NC gate-stack in NCFET, improves these characteristics over DEFED. Also, superiority of the behavior of the proposed NCFED over NCFET is obvious from Table 2.

6. Effect of HfO_2 thickness on Performance of NCFED

Fig. 11 represents variation of I_{ON}, I_{OFF}, I_{ON}/I_{OFF} and subthreshold slope of NCFED against gate length for different HfO_2 thicknesses. Changing the thickness of the HfO_2 layer in the range of 2 to 5nm does not affect the mentioned parameters considerably in the proposed NCFED.

In Fig. 12, variation of gate capacitance, gate delay time and energy delay product of NCFED has been represented against gate length for different HfO_2 thicknesses. At a certain gate length, as the HfO_2 thickness is increased, the mentioned parameters are increased, too. For shorter gate lengths, the values of these parameters for different HfO_2 thicknesses are close together; while they slightly differ from each other for longer channel lengths. However, the differences are very small; for example, the gate capacitance is increased about 0.05fF when HfO_2 thickness is increased from 2 to 5nm.

Considering both of Fig. 11 and Fig. 12, it can be concluded that the parameters of NCFED are not dependent considerably on changing of the HfO_2 thickness in the range of 2 to 5nm. This is consistent with the hysteresis behavior of the HfO_2 material, represented in Fig. 6a in which the polarization does not face hysteresis for thicknesses in the range of 2 to 5nm when the electric field intensity across the layer is changed. Consequently, the voltage amplification does not face any hysteresis, too, and the amount of voltage amplification, the amount of induced charge and the amount of current flowed in the channel will be nearly the same in the on- (or off-) state for HfO_2 thicknesses in the range of 2 to 5nm. As represented in Fig. 9, I_{OFF}, I_{ON}, I I_{ON}/I_{OFF} and subthreshold slope are nearly the same at each channel length.

Regarding Fig. 6a, as the HfO_2 thickness is increased, the polarization-electric field dependency faces steeper slope which leads to increasing of the gate capacitance. So, as represented in Fig. 12a, especially for longer channel lengths, the gate capacitance of NCFED is increased as the HfO_2 thickness is increased. As the result, as represented in Fig. 12b, and Fig. 12c respectively, the gate delay time and the energy delay product will be increased as the HfO_2 thickness is increased, especially for longer channel lengths. This reveals that NCFED with thinner HfO_2 layer can provide better switching performance with less energy consumption.

7. Scalability and Fabrication Challenges

Representation of the diode behavior in the FED is dependent on the channel length, channel and reservoirs doping level and the gate voltage. The FED Channel is lightly doped and formation of the inversion layer and pn (or np) regions under the gates is occurred by applying suitable gate voltages. When each gate is biased, inner fringing electric field is created under it which affects the inversion condition under the other gate, and consequently, the strength of the pn (or np) region. In order to reduce the amplitude of the gate voltage, the channel thickness can be shortened. However, for very short channel thicknesses, the quantum confinement of the carriers occurs at the channel surface, which reduces the surface charges under the gates and weakens the strength of the pn (or np) region and voltage amplification, thereby, deteriorating the NC effect and on- (or off-) state current.

Reducing the channel length increases the longitudinal electric field intensity along the channel (created by V_{DS}), which in turn, increases the carrier injection from the reservoirs into the channel. In the on-state, the longitudinal electric field forces carrier injection from the reservoirs into channel that forms stronger forward biased np region. Thereby, higher I_{ON} is produced at shorter gate lengths. In the off-state, these injections form weaker reverse biased pn region. Thereby, lower I_{OFF} is produced at shorter gate lengths.

On the other hand, as explained above, the produced inner fringing electric field does not affect the polarization and the gate capacitance remains negative and C_{FE-DE} remains larger than C_{DE} at longer channel lengths; while at shorter channel lengths, the adverse effects are considerable, causing positive gate capacitance, reduced NC effect and reduced C_{FE-DE}. Therefore, the subthreshold slope will be above 60mV/dec for short channel lengths. Reduction in C_{FE-DE} causes reduction in gate delay time and *EDP* at shorter channel lengths as represented in Fig. 10. Therefore, it can be concluded that scalability of the proposed NCFED with respect to the gate length has some limits especially, for shorter channel lengths which is due to reduction in NC effect.

There are some challenges for adopting the ferroelectric layer, also. Integration of ferroelectric layer with conventional MOS structures needs matched design of the ferroelectric-dielectric layers to get a stabilized insulator in the gate-stack. The resultant insulator is very sensitive to representing non-hysteretic and non-transient behavior for realizing stable static NC effect. In addition, it is difficult to achieve uniform ferroelectricity in very thin ferroelectric film. The disordered and polycrystalline oxide film causes various problems, with changing threshold voltage as well as

non-uniform doping. These problems are challenges that remain to be solved by optimization of deposition techniques for HfO_2 film [40-41].

8. Conclusion

In this manuscript, a negative capacitance (NC) gate-stack field effect diode (NCFED) was proposed in which using the ferroelectric HfO_2 in series with the dielectric SiO_2 allowed presence of NC phenomenon in the gate-stack. NCFED was analyzed by TCAD simulation and the results were compared with the dielectric gate-stack FED (DEFED). Due to NC phenomenon, for a certain applied gate voltage, voltage amplification occurred in NCFED and more charges were accumulated in the channel under the gates in the off- and on-states. Since the current is proportional to the density of the accumulated charges, lower I_{OFF}, higher I_{ON} and larger I_{ON}/I_{OFF} were achieved in NCFED comparing to DEFED. In addition, the subthreshold slope was considerably reduced in NCFED by utilizing the benefit of the NC gate-stack. Increment in I_{ON}/I_{OFF} and decrement in subthreshold slope can provide better switching performance for the proposed NCFED comparing to DEFED.

Also, the advantage of using NC gate-stack was observed in gate capacitance, gate delay time and energy delay product where these parameters were lower considerably in NCFED than DEFED. This feature makes less energy consumption during the switching operation in NCFED.

Finally, effect of changing of the HfO_2 thickness on the considered electrical parameters was investigated in NCFED. It was observed that changing the HfO_2 thickness in the range of 2 to 5nm would not change the values of I_{ON}, I_{OFF}, I_{ON}/I_{OFF} and subthreshold slope considerably for a given channel length. This behavior is consistent to small variation of polarization versus applied electric field for the HfO_2 thicknesses in the range of 2 to 5nm. In this thickness range, the polarization and consequently, the amplified voltage do not experience any hysteresis. So, the induced charge and the current flow in the channel will not change considerably.

On the other side, changing the HfO_2 thickness changed the gate capacitance, gate delay time and energy delay product slightly for shorter channel lengths. However, these parameters were changed more for longer channel lengths. Again, this behavior is related to the previously observed variation of polarization of HfO_2 by the applied electric field, in which the change in values of polarization against the electric field is steeper for thicker HfO_2. As the result, larger gate capacitance

is created for thicker ferroelectric layer.

In overall, comparing the electrical characteristics of the proposed NCFED with DEFED revealed that NCFED could provide better switching performance in addition with lower energy consumption, while its parameters were not too sensitive to the HfO_2 thickness.

Statements and Disclosures

The authors declare that no funds, grants, or other support were received during the preparation of this manuscript. The authors have no relevant financial or non-financial interests to disclose. S.A. Hashemi conducted the research subject. Both of the authors S.A. Hashemi and M. Hajipour run the materials and performed the simulations. S.A. Hashemi wrote the main manuscript text. All authors reviewed the manuscript.

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Fig. 1 Structure of FED with dielectric (SiO_2) gate-stack (a) conventional FED [1] (b) DEFED [9]

Fig. 2. NC MOSFET (a) gate structure (b) capacitor representation.

Fig. 3 Structure of proposed NCFED

Fig. 4. Fabrication process of proposed NCFED (a) SOI channel formation (b) n^+ regions implantation (c) p^+ regions implantation (d) SiO_2 deposition (e) SiO_2 etching (f) source/drain and inner GS/GD metallization (g) HfO_2 deposition (h) HfO_2 etching (i) extended source/drain and top GS/GD metallization.

Fig. 5 Comparison between simulated and experimental results for DG MOSFET of [36]

Fig. 6 (a) polarization-electric field characteristics as a function of ferroelectric thickness (b)

energy-polarization diagram of total gate-stack capacitance (c) surface potential-gate voltage dependency of proposed NCSFED

Fig. 7. Carrier distribution in DEFED and NCFED in the off-state.

Fig. 8. Carrier distribution in DEFED and NCFED in the on-state.

Fig. 9. Comparison between NCFED and DEFED (a) I_{OFF} (b) I_{ON} (c) I_{ON}/I_{OFF} (d) Subthreshold slope, V_{DS}=1.3V.

Fig. 10. Comparison between NCFED and DEFED (a) gate capacitance (b) gate delay time (c) energy delay product, V_{DS}=1.3V.

Fig. 11. Effect of HfO_2 thickness on NCFED parameters (a) I_{OFF} (b) I_{ON} (c) I_{ON}/I_{OFF} (d) Subthreshold slope, V_{DS}=1.3V.

Fig. 12. Effect of HfO_2 thickness on NCFED parameters (a) Gate capacitance (b) Gate delay time (c) Energy delay product, V_{DS}=1.3V.

Table 1. Parameters of proposed NCFED and DEFED. Physical parameters for Si and SiO_2 at 300K have been selected with respect to recommended values in [34].

Table 2 Characteristics of proposed NCFED, DEFED and NCFET.

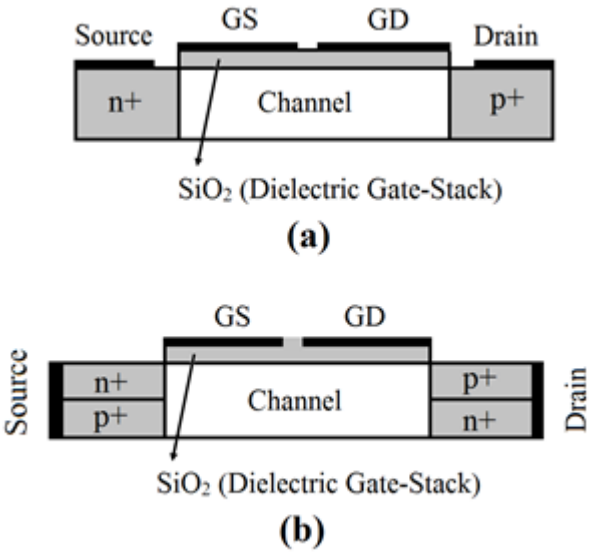


Fig. 1

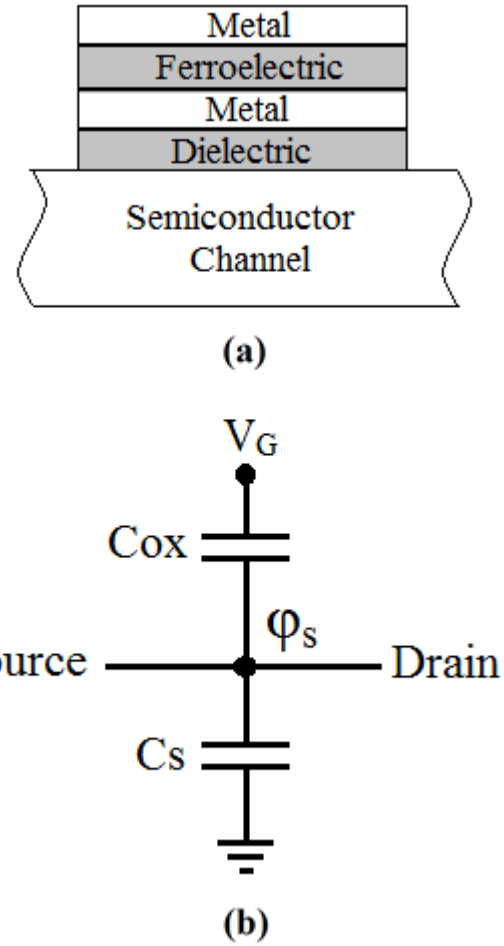


Fig. 2

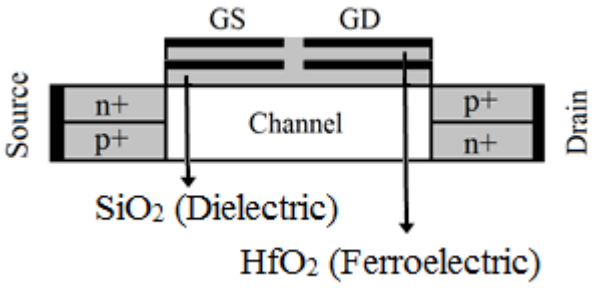
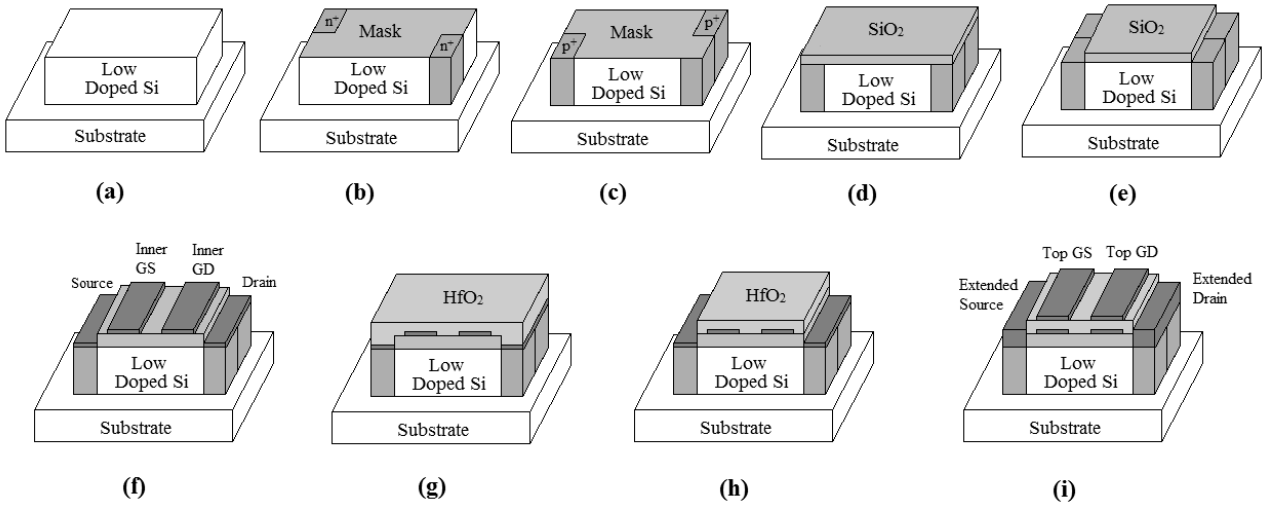


Fig. 3



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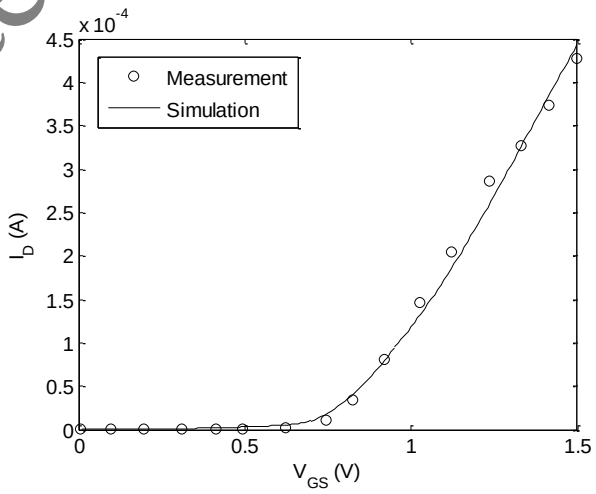

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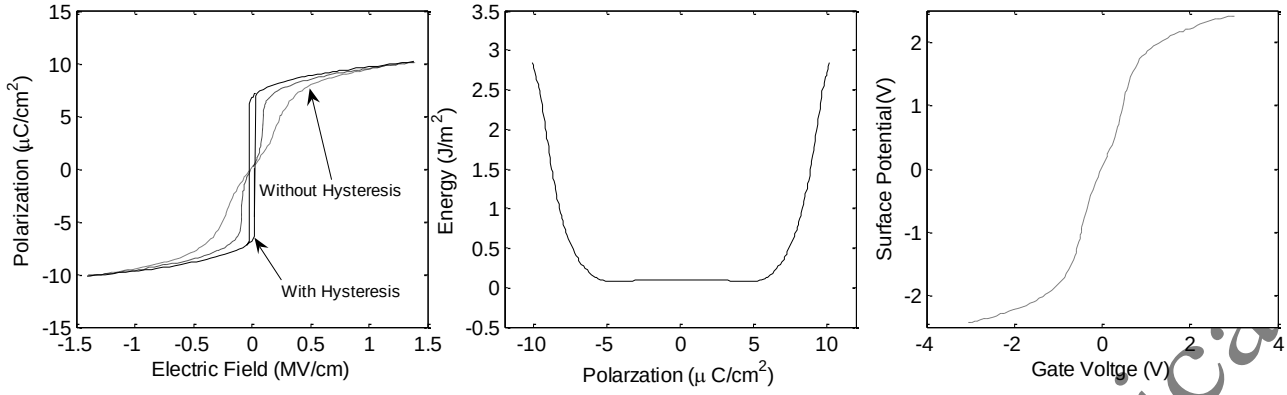

Fig. 6

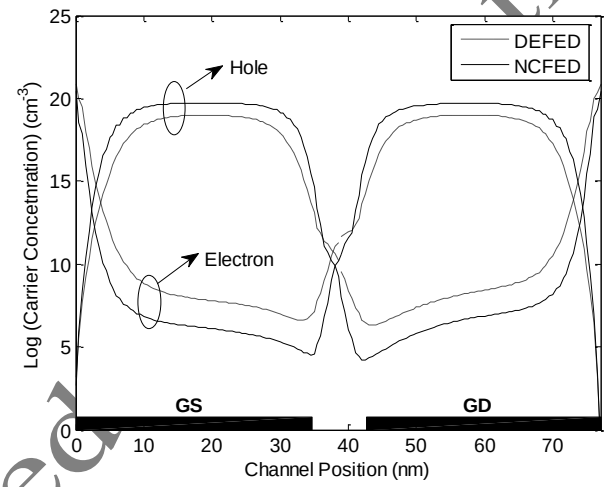

Fig. 7

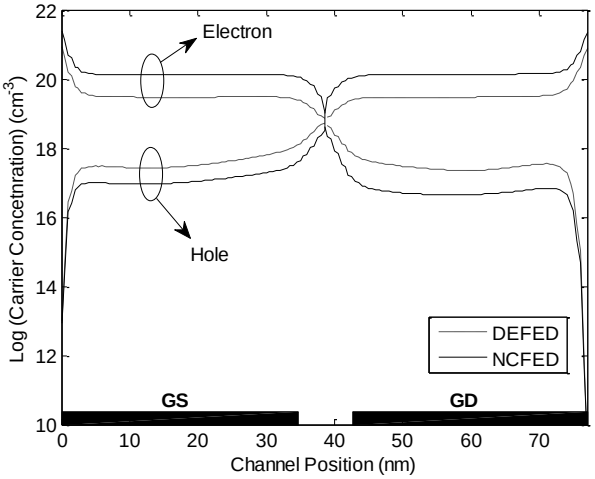

Fig. 8

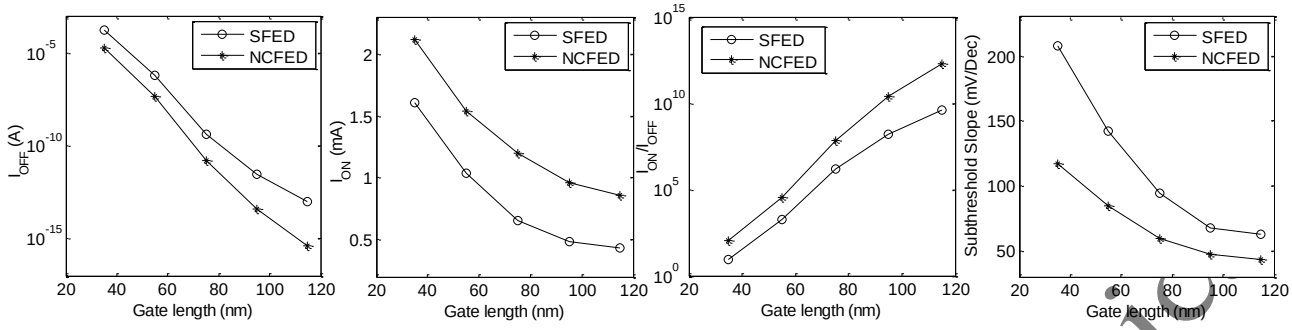

Fig. 9

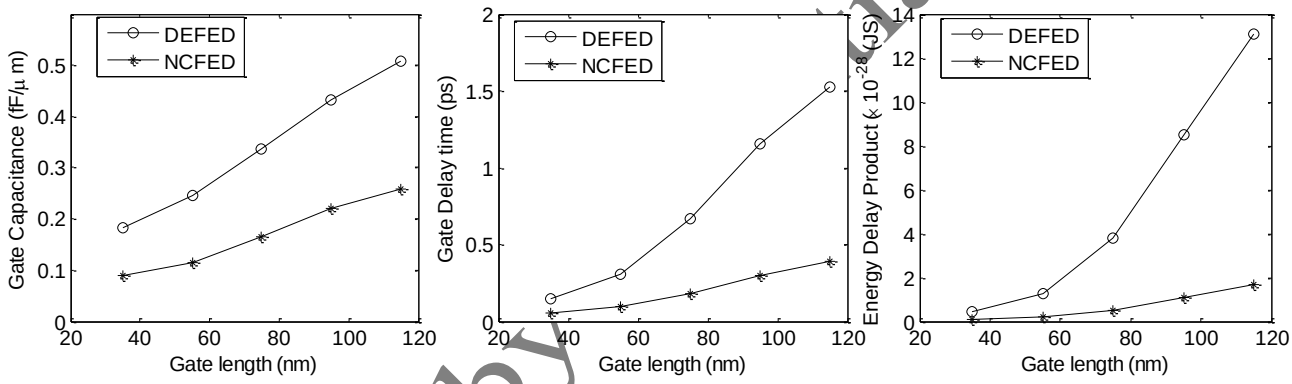

Fig. 10

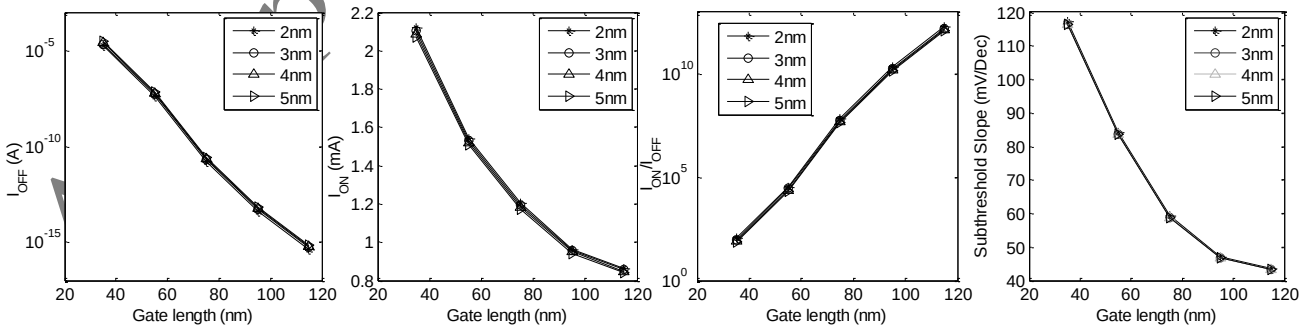

Fig. 11

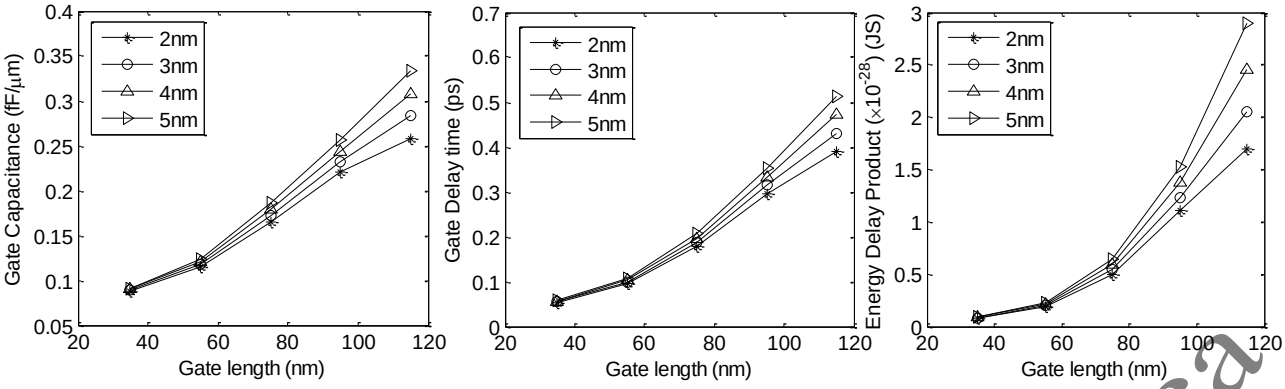

Fig. 12

Table 1

Parameter	Value
$L_S=L_D$	85 nm
$L_{GS}=L_{GD}$	35nm
Si thickness	50nm
n^+ concentration	10^{21} cm^{-3}
p^+ concentration	10^{21} cm^{-3}
Channel concentration	10^{14} cm^{-3}
GS-GD separation	7nm
SiO_2 thickness	2nm
HfO_2 thickness	2nm
Gate metal work function	5eV
Channel material	Si
GS /GD Bias	±2V
Drain/Source Bias	1.3V
Remanent polarization for HfO_2	9μC/cm^2
Coercive field for HfO_2	1MV/cm

Spontaneous polarization for HfO_2	9.4μC/cm^2
Dielectric constant for HfO_2	32
Dielectric constant for SiO_2	3.9
Dielectric constant of Si	11.7

Table 2

Parameters	Device	L_G		
		35nm	75nm	115nm
I_{ON} / I_{OFF}	DEFED	9.2	1.6×10^{6}	4.3×10^{9}
	NCFET	75.6	1.5×10^{7}	3.2×10^{11}
	NCFED	117.3	7.2×10^{7}	2×10^{12}
SS (mV/dec)	DEFED	207.5	94.2	62.6
	NCFET	160.3	64.4	50.5
	NCFED	117.4	59.3	43.7
C_G (fF/μm)	DEFED	0.18	0.34	0.51
	NCFET	0.13	0.23	0.34
	NCFED	0.09	0.17	0.26
τ (ps)	DEFED	0.15	0.67	1.53
	NCFET	0.09	0.38	0.92
	NCFED	0.05	0.18	0.39
EDP ($\times10^{-28}$ Js)	DEFED	0.45	3.81	13.11

NCFET	0.19	1.48	5.29
NCFED	0.08	0.52	1.71