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A packed U cells multilevel inverter fed six-phase induction drive for industrial applications

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Multilevel inverter;
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Power loss.

Abstract

This paper analyses a Six-Phase Induction Drive (SPID) powered by a five-level Packed U Cells (PUC) Multilevel Inverter (MLI) for high-power applications. The MLI produces a symmetrical 5-level output voltage waveform through sensor less self-capacitor voltage balancing control. This ensures that the voltage across the capacitor stays at half the value of the DC source. This control method reduces system complexity and enhances performance. The proposed system requires fewer components than conventional Cascade H-Bridge (CHB) fed drives. The proposed system is similar to drives using Flying Capacitor (FC) and CHB MLI technology. The system is designed to power a SPID with a distributed neutral load, and its functionality is simulated using MATLAB/Simulink software. Finally, a prototype experimental setup has been developed in the laboratory to validate the analytical development of the proposed system.

1. Introduction

In modern industry, high-performance, durable, low-maintenance induction motor drives are commonly used. However, the converters required for high-power electrical drives often rely on expensive high-frequency semiconductor switches that may not always be available. One possible solution to the challenge is multiphase drives with multilevel converter. This method uniformly distributes the power among the semiconductor switches, decreasing current for each phase while maintaining the per-phase voltage. Opting for multiphase drives instead of traditional three-phase drives offers several benefits, including increased stator frame power, higher torque pulsation frequency, reduced DC-link current harmonics and lower amplitude of pulsating torque. Additionally, their expandable design ensures high reliability. By effectively utilizing induction motor drives and multiphase voltage source inverters, it is possible to achieve high power for various industrial drives [1-4].

It is possible to create a multiphase machine with any number of phases by shifting the stator winding of a traditional three-phase machine by δ electrical degree. However, studies show that a six-phase machine offers superior performance compared to other options, as noted by Rathore and Yadav [5]. A Six-Phase Induction Drive (SPID) with an unsymmetrical winding arrangement is frequently employed for high-power applications. The stator winding of the motor is divided into two parts, covering δ = 300° electrical, and utilizes a 60-degree phase belt. Its rotor winding is of the cage type. Although it has a similar power rating to other designs, the proposed inverter has lower current rating switches.

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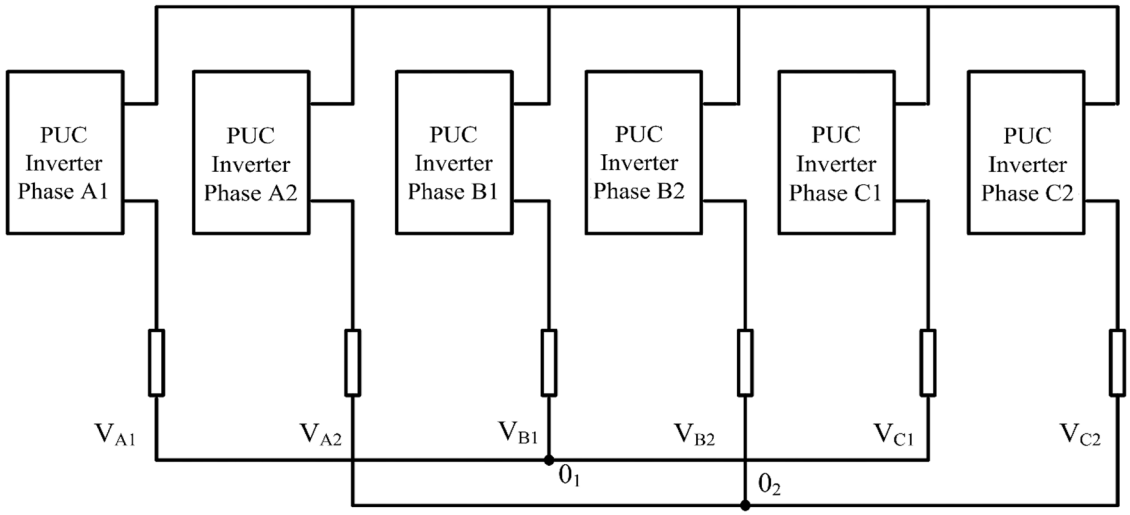


Figure 1. Block diagram of proposed MLI fed SPID.

In various industrial applications, a Multilevel Inverter (MLI) offers multiple advantages over a traditional two-level inverter, such as reduced Total Harmonic Distortion (THD), lower dv/dt stress, decreased switching losses, and improved efficiency [6,7]. In a study by Bana et al. [8], researchers surveyed three popular MLI topologies, namely Neutral-Point Clamped (NPC), Cascaded H-bridge (CHB), and Flying Capacitors (FC). The Packed U Cells (PUCs) MLI structure is a highly promising alternative to traditional MLIs. It offers a combination of benefits from both CHB and FC. With the PUC MLI structure, only one DC source is needed, and the other sources required are supplied by capacitors that serve as auxiliary sources [9,10]. Compared to FC, the PUC structure generates half the voltage of a capacitor and the same level of the inverter.

Innovative advancements in power conversion technology have led to the creation of the PUC inverter, combining the benefits of FC and CHB. This hybrid technology has reduced production costs, smaller device sizes, and improved power conversion efficiency [11,12]. Researchers have explored various control schemes for PUC, including non-linear controllers and hysteresis current control [13]. PUC inverters are designed to provide exceptional power quality and flexibility in producing multilevel voltage, using fewer components than traditional inverters [14,15]. However, certain control techniques, such as FCS-MPC, depend on converter models and component sizes, which can cause fluctuations and high switching frequencies [16,17]. In contrast, the hysteresis control technique has been proposed as an effective solution for regulating the discharging and charging of capacitor voltage in the rectifier and inverter modes.

Additionally, the suggested hysteresis control method can be effortlessly put into practice and allows for flexible switching frequencies, resulting in higher loss and potential challenges in filter design. Trabelsi et al. [18] have introduced a sensor less single-phase 5-level PUC with balanced capacitor voltage that doesn't require an external controller or voltage feedback sensor. However, it's worth noting that these PUC topologies have only been tested in stand-alone or grid-connected inverters and haven't yet been applied to drive applications [19,20].

There have been few studies on using MLI to power multiphase machines, compared to 2-level inverters. The control algorithm for space vector modulation in MLI is complex to implement and design. While carrier-based PWM is commonly used for multiphase drives, it cannot fully utilize DC voltage [21]. Some researchers have proposed 5-level five-phase SVM techniques for cascaded inverters but could not limit harmonic currents [22]. Other researchers have developed novel SVM techniques that limit current harmonic components in five-phase 3-level NPC inverters and provide optimal switching states for regulating current in induction motor drives [23]. The techniques for a five-phase induction drive have been enhanced by expanding the sub-sector from 10 to 14 and minimizing the common-mode voltage variation [24]. However, these SVM techniques only suppress harmonics generated by the inverter itself and not those induced by the back e.m.f of the machine. Additionally, these techniques do not provide solutions for asymmetrical currents produced by the phase windings other than limiting harmonic components on the *x-y* plane [25].

This paper efficiently models SPID using a 5-level PUC inverter and studies the behavior of the motor through an appropriate control technique. Moreover, the suggested system's performance is evaluated compared to the traditionally designed CHB system. Moreover, the power losses and efficacy of FC, PUC, and CHB MLI-based systems are assessed and compared. A test rig is developed in the lab to verify the proposed technique's effectiveness. Current, voltage, and harmonics waveforms are analyzed using scopes YokogawaDL750E and FLUKE43B.

2. Proposed PUC MLI structure

Figure 1 shows the proposed 5-level PUC inverter connected to the SPID. For clarity, we only look at Phase-A1 in Figure 2 to understand how the inverter operates. This MLI has six unidirectional switches per phase (T_1 to T_6), a DC source voltage (V_1), and a self-voltage balancing capacitor (C_1). The switches are controlled in complementary pairs (T_1, T_4), (T_2, T_5), and (T_3, T_6) with different switching sequences. The PUC configurations' eight switching states, named Δ_i (i = 0, 1, 2, 3, 4, 5, 6, 7), produce a 5-level output ranging from +2E to -2E. You can find all the details in Table 1.

Table 1. Switching prioritization of the 5-level PUC MLI.

Modes (M)	Prioritization no.	ON-Switches	Magnitude of output voltage	5-level output	Effect on capacitor
Δ_1	V_{pri11}	T_1, T_5, T_6	V_1	$+2E$	No change
Δ_2	V_{pri21}	T_1, T_3, T_5	$V_1 - V_2$	$+E$	Charged
Δ_3	V_{pri22}	T_1, T_2, T_6	V_2	$+E$	Discharged
Δ_4	V_{pri31}	T_1, T_2, T_3	0	0	No change
Δ_5	V_{pri32}	T_4, T_5, T_6	0	0	No change
Δ_6	V_{pri41}	T_3, T_4, T_5	$-V_2$	$-E$	Charged
Δ_7	V_{pri42}	T_2, T_4, T_6	$V_2 - V_1$	$-E$	Discharged
Δ_8	V_{pri51}	T_2, T_3, T_4	$-V_1$	$-2E$	No change

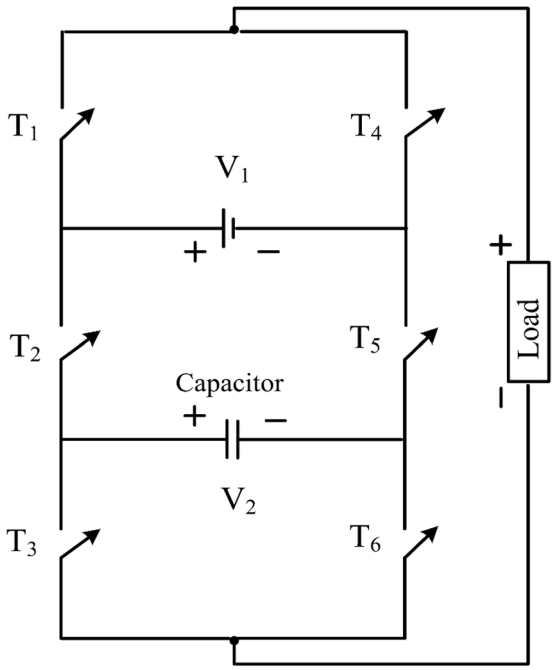


Figure 2. Phase A1 of the 5-level PUC MLI [15].

Figure 3 illustrates the different current paths and conducting modes of the proposed PUC MLI. For a better understanding, Figure 4 represents a complete cycle of the 5-level output voltage and current waveform.

The process of self-voltage-balancing is analytically derived using a capacitor power relationship. Let fundamental voltage $V(x)$ and instantaneous current I be expressed as:

$$V(x) = V_m \sin(\omega t), \tag{1}$$

$$I = I_m \sin(\omega t - \phi), \tag{2}$$

where V_m and I_m is the maximum value of voltage and output loads current, and ϕ is the power factor angle.

The DC capacitor transferred energy (E) to the load is given as:

$$I = \frac{dq}{dt}, \tag{3}$$

$$dE = Vdq = V * I * dt, \tag{4}$$

where q and I represent the electric charge and instantaneous current.

$$E = \int V * I * dt. \tag{5}$$

The voltage equation during the positive half for determining the capacitor energy is as:

$$E^+ = \int_0^{\Pi} V_K * I * dt. \tag{6}$$

After substituting the value, the resulting equation is given as:

$$E^+ = \int_0^{\Pi} V_K * \mathrm{I_m} \sin(\omega t - \phi) d\omega t, \tag{7}$$

$$E^+ = -V\,\mathrm{I_m}\left[\cos(\omega t - \phi)\right]_{\theta_1}^{\theta_2} + V\,\mathrm{I_m}\left[\cos(\omega t - \phi)\right]_{\theta_3}^{\theta_4},$$

$$E^+ = V\,\mathrm{I_m}\,[\cos(\theta_1 - \phi) - \cos(\theta_2 - \phi) + \cos(\theta_3 - \phi) - \cos(\theta_4 - \phi)]. \tag{8}$$

The voltage equation during the negative half for determining the capacitor energy is as:

$$E^- = \int_0^{2\Pi} V_K * \mathrm{I_m} \sin(\omega t - \phi) d\omega t, \tag{9}$$

$$E^- = -V\,\mathrm{I_m}\left[\cos(\omega t - \phi)\right]_{\theta_5}^{\theta_6} + V\,\mathrm{I_m}\left[\cos(\omega t - \phi)\right]_{\theta_7}^{\theta_8}$$

$$E^- = V\,\mathrm{I_m}\,[\cos((\Pi + \theta_2) - \phi) - \cos((\Pi + \theta_1) - \phi) + \cos((\Pi + \theta_4) - \phi) - \cos((\Pi + \theta_3) - \phi)]. \tag{10}$$

By analysing Eqs. (8) and (10), it is apparent that the energy level during the half-cycle will have an identical value but with an opposite sign.

As long as no average current flows through a capacitor during the fundamental period (T_s), the voltage across it will remain balanced. Capacitor current is calculated using Eq. (11) as:

$$i_c(t) = c\frac{dV_c}{dt}. \tag{11}$$

The Eq. (12), obtained by integrating Eq. (3) over one fundamental cycle, shows the instantaneous value of both voltage and capacitance. The variables $i_c(t)$ and $V_c(t)$ are associated with the value of the circuit's components:

$$\int_t^{t+T_s} i_c(t) = V_c(t) - V_c(0). \tag{12}$$

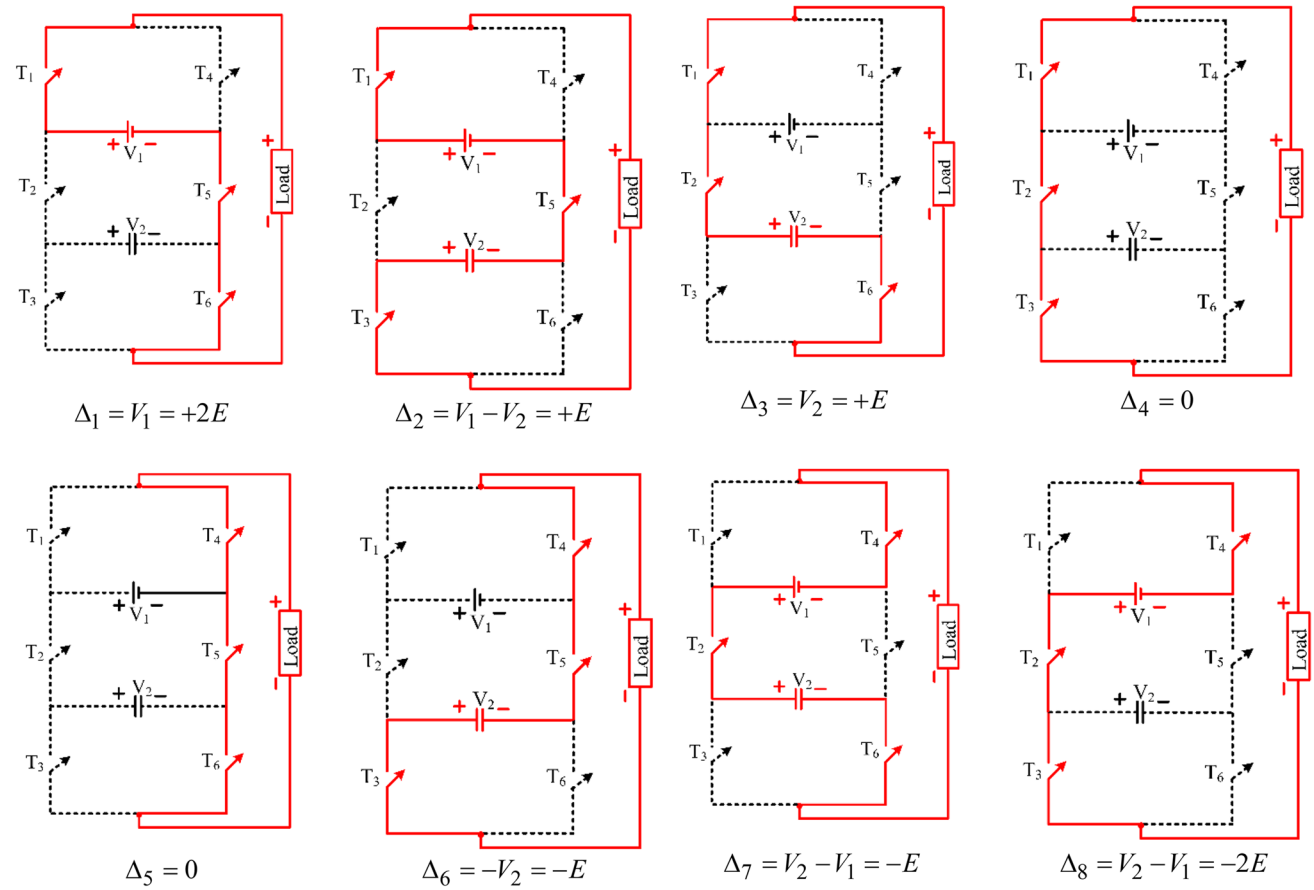


Figure 3. Conducting modes and current path of proposed 5-level PUC.

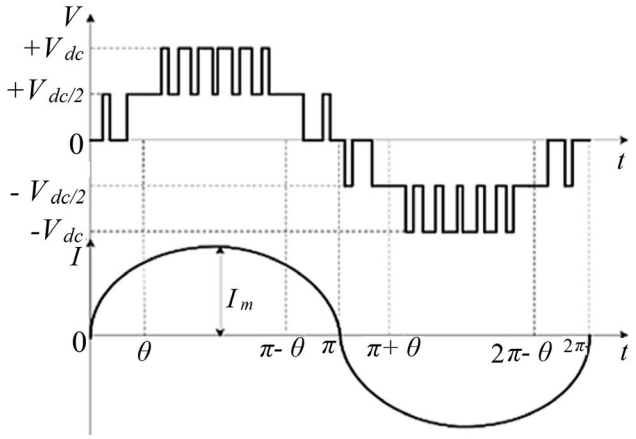


Figure 4. Waveform of output voltage and current.

In order to balance the voltage of a capacitor, it is important to ensure that the initial and final voltage values remain consistent. Therefore,

$$\int_{t}^{t+T_s} i_c(t) = 0. \tag{13}$$

If the average current flowing through a capacitive system over a cycle is zero, Eq. (13), a capacitive system can achieve voltage balancing. This is possible if the net charge built up during capacitor charging and discharging during each fundamental cycle is zero in a steady state. An LS-PWM switching strategy guarantees the exact duration of a specific output voltage level in both halves of the fundamental cycle. The carrier frequency and modulating voltage peak to peak are the same in this method. Additionally, the same parameters were used for both the simulation and the experiment, and the results were validated.

3. Modelling of SPIM

The equations of two three-phase systems in the *d-q* reference frame are converted to evaluate the effectiveness of an asymmetrical six-phase induction motor, utilizing the methodology adopted by Rathore and Yadav [26]. The resulting equations can be written as:

$$V_d = \frac{1}{3}\left[\sum_{k=1}^{6} V_k \operatorname{Cos}\left(\theta - \frac{(k-1)\pi}{6}\right)\right], \tag{14}$$

$$V_q = \frac{1}{3}\left[\sum_{k=1}^{6} V_k \operatorname{Cos}\left(\theta - \frac{(k-1)\pi}{6}\right)\right], \tag{15}$$

$$v_q = \frac{1}{3}\left[\sum_{k=1}^{6} v_k \cos\left(\theta - \frac{(k-1)\Pi}{6}\right)\right]. \tag{16}$$

The *q-d* axis current and flux component of the rotor and stator are as follows:

$$\psi_{ds} = \frac{1}{s}\left[-\omega_e \psi_{qs} - R_s i_{ds} + V_{ds}\right], \tag{17}$$

$$i_{ds} = \frac{1}{L_s}\left[\psi_{ds} - L_m i_{dr}\right], \tag{18}$$

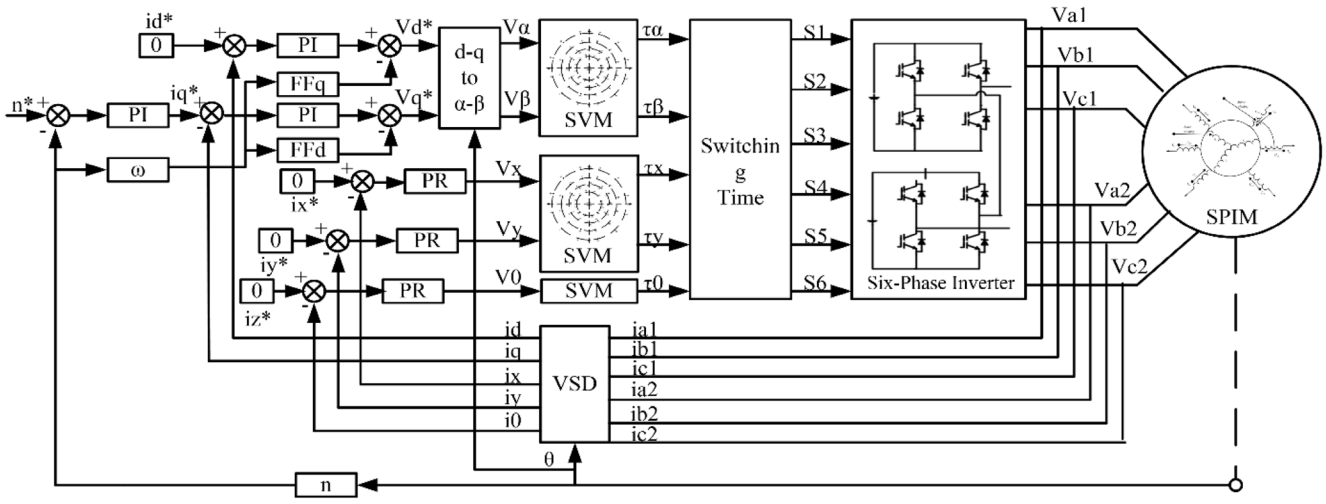


Figure 5. SPID control scheme.

$$\psi_{dr} = \frac{1}{s}\left[(\omega_e - \omega_r)\psi_{qr} - R_r i_{dr}\right], \tag{19}$$

$$i_{dr} = \frac{1}{L_r}\left[\psi_{qr} - L_m i_{ds}\right], \tag{20}$$

$$\psi_{qs} = \frac{1}{s}\left[-\omega_e \psi_{ds} - R_s i_{qs} + V_{qs}\right], \tag{21}$$

$$i_{qs} = \frac{1}{L_s}\left[\psi_{qs} - L_m i_{qr}\right], \tag{22}$$

$$\psi_{qr} = \frac{1}{s}\left[(\omega_r - \omega_e)\psi_{dr} - R_r i_{qr}\right], \tag{23}$$

$$i_{qr} = \frac{1}{L_r}\left[\psi_{qr} - L_m i_{qs}\right]. \tag{24}$$

The torque and speed are expressed as follows:

$$T_e = \frac{3p}{2}\left[\psi_{ds} i_{qs} - \psi_{qs} i_{ds}\right], \tag{25}$$

$$\omega_e = \frac{p}{2s}\left[\frac{1}{J}\left(T_e - T_L - D\frac{2}{p}\omega_e\right)\right]. \tag{26}$$

The equation includes several variables such as ω_r for angular speed, ω_e for arbitrary reference speed, (p) for pole pair, subscript (r) and (s) for rotor and stator, respectively, J for moment of inertia, L_m for mutual inductance, and T_L and T_e for load and electric torque respectively.

3.1. SPID closed-loop control

Figure 5 depicts the closed-loop control technique for the SPIMD. The d-axis reference current is kept constant while the closed-loop controllers generate the q-axis reference current. A PI controller governs the sub-space's current components, and the Feed Forward (FF) terms decouple the d-q axis. Closed-loop PR controllers watch the reference signals while considering periodic current elements on the x-y and zero-sequence subspace.

4. Efficiency and power loss calculation

4.1 Modelling of losses and efficiency of PUC inverter

Power semiconductor devices (MOSFET and Diode) are associated with conduction and switching losses in the proposed PUC MLI structure. During ON-state voltage, current flow through power semiconductor devices causes conduction power losses (P_C). Load current flows through the anti-parallel diode and MOSFET as in MLI Kumar et al. [27], resulting in $P_{C,MOSFET}$ and $P_{C,Diode}$. These losses can be expressed as follows:

$$P_{C,MOSFET} = \eta_{MOSFET}(t).\left[\frac{1}{2\Pi}\int_0^{2\Pi}\left[V_{ON,MOSFET} * I + R_{ON,MOSFET} * I^{\beta+1} d(\omega t)\right]\right], \tag{27}$$

$$P_{C,Diode} = \eta_{Diode}(t).\left[\frac{1}{2\Pi}\int_0^{2\Pi}\left[V_{ON,Diode} * I + R_{ON,Diode} * I^{2} d(\omega t)\right]\right], \tag{28}$$

$$P_{C,Total} = P_{C,MOSFET} + P_{C,Diode}. \tag{29}$$

The voltage when the MOSFET is turned on is labelled as $\eta_{MOSFET}(t)$, and the voltage when the anti-parallel diode is turned on is labelled as $\eta_{Diode}(t)$. β represents the MOSFET specification constant, $R_{ON,MOSFET}$ and $R_{ON,Diode}$ represent the equivalent resistance of the MOSFET and diode, respectively. The power lost during the turning-on and turning-off is called switching loss (P_s). The energy lost during turn-on and turn-off, $E_{on,T}$, $E_{off,T}$ can be calculated for the power switch.

$$E_{on,T} = \int_0^{ton} v(t)i(t)dt = \int_0^{ton}\left[\left(\frac{V_{sw}t}{t_{off}}\right)\left(-\frac{I_1(t-t_{on})}{t_{on}}\right)\right]dt = \frac{1}{6}V_{SW} I_1 t_{on}, \tag{30}$$

$$E_{off,T} = \int_0^{t_{off}} v(t)i(t)dt = \int_0^{t_{off}} \left[\left(\frac{V_{sw}t}{t_{off}}\right)\left(-\frac{I_2(t-t_{off})}{t_{off}}\right)\right]dt = \frac{1}{6}V_{SW}I_2t_{off}. \quad (31)$$

The switch's (MOSFET) cross-over time ON and OFF interval are represented by t_{on} and t_{off}, respectively. The power loss (P_s) of the switch can be calculated using the following expression:

$$P_S = \frac{1}{T}\left(N_{on}E_{on} + N_{off}E_{off}\right). \quad (32)$$

Therefore, for PUC MLI, the total power loss is given as:

$$P_{Total\ loss} = P_{C,MOSFET} + P_{C,Diode} + P_S. \quad (33)$$

These equations can be used to calculate the proposed MLI structure's overall power loss. Furthermore, the efficiency (η) can be evaluated in the following manner:

$$\eta = \frac{P_{output}}{P_{input}} = \frac{P_{output}}{P_{output} + P_{Total\ loss}}. \quad (34)$$

Quantitative analysis of power loss and efficiency is conducted using the equation provided. The proposed MLI structure's efficiency and power loss are evaluated using IRF640NSTRLPBF MOSFET switches.

4.2. Efficiency and power losses of SPID

When it comes to motors, there are two kinds of losses to consider: electrical and mechanical. In the suggested SPID, constant drive power is achieved by maintaining constant torque and speed, resulting in constant mechanical losses. Rathore and Yadav [28] have also ignored the impact of ripple torque on machine losses. As a result, the power input of the SPIMD is constant and given as:

$$P_{input} = P_{output} + P_{losses}. \quad (35)$$

SPIM total losses is given by:

$$P_{losses} = P_{iron} + P_{copper} + P_z + P_m. \quad (36)$$

Eddy current, hysteresis, and excess losses are all possible causes of iron losses. The following formula can be used to determine the iron losses if the coefficient for each loss stays constant. Expression:

$$P_{losses} = P_{eddy} + P_{hysteresis} + P_{excess}, \quad (37)$$

when a machine's flux and frequency change, the loss coefficient may also vary. The significant changes in this term may result in varying coefficients for hysteresis, eddy current, and excess loss [29]. The copper losses of the rotor and stator are dependent on the current and resistance of each. For steady-state analysis, leakage inductance is typically neglected, as simplified by the method described by Zhang et al. [30]. This leads to the expression of rotor and stator losses.

$$P_{copper,rotor} = \frac{1}{2}r_r\left(I_{r\alpha}^2 + I_{r\beta}^2\right), \quad (38)$$

$$P_{copper,stator} = \frac{1}{2}r_s\left(I_{s\alpha}^2 + I_{s\beta}^2\right). \quad (39)$$

The copper loss in a zero-sequence subspace is determined by the current and resistance and can be expressed as:

$$P_{zero} = \frac{1}{2}r_r\left(I_{rz_1}^2 + I_{rz_2}^2\right) + \frac{1}{2}r_s\left(I_{sz_1}^2 + I_{sz_2}^2\right). \quad (40)$$

The amount of mechanical loss is determined by the motor's speed, which can be calculated using the following equation as:

$$P_m = K_m\omega^2, \quad (41)$$

when keeping a steady speed, the mechanical losses stay the same. Additionally, inverter losses are combined with mechanical losses. As a result, the formula for power output is as follows:

$$P_{output} = \tau\omega, \quad (42)$$

and SPIMD efficiency is calculated as:

$$\eta = \frac{P_{output}}{P_{input}} = \frac{R\omega}{P_{output} + P_{losses}} = \tau\omega. \quad (43)$$

Eq. (43) is reformulated as:

$$\eta = \frac{P_{output}}{P_{input}} = \frac{\tau\omega}{V_{dc} \times I_{dc}}. \quad (44)$$

5. Results and analysis

5.1. Modelling of losses and efficiency of PUC inverter

The suggested SPFT topology uses multicarrier Sinusoidal PWM (SPWM), as shown in Figure 6. In this study, sine-modulated PWM pulses are produced by using the level-shifting (LS-PWM) approach to power switching devices.

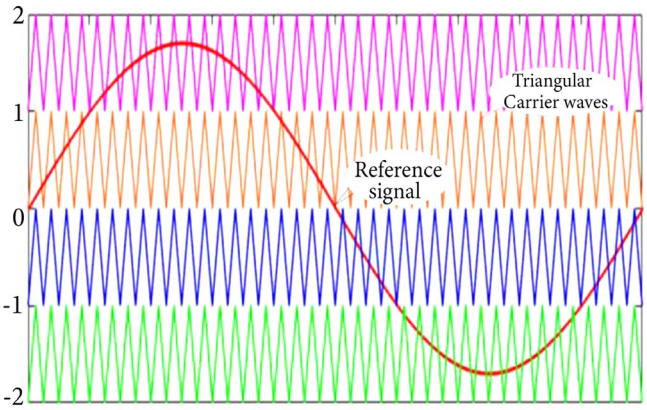


Figure 6. Switching scheme for the 5-level PUC MLI.

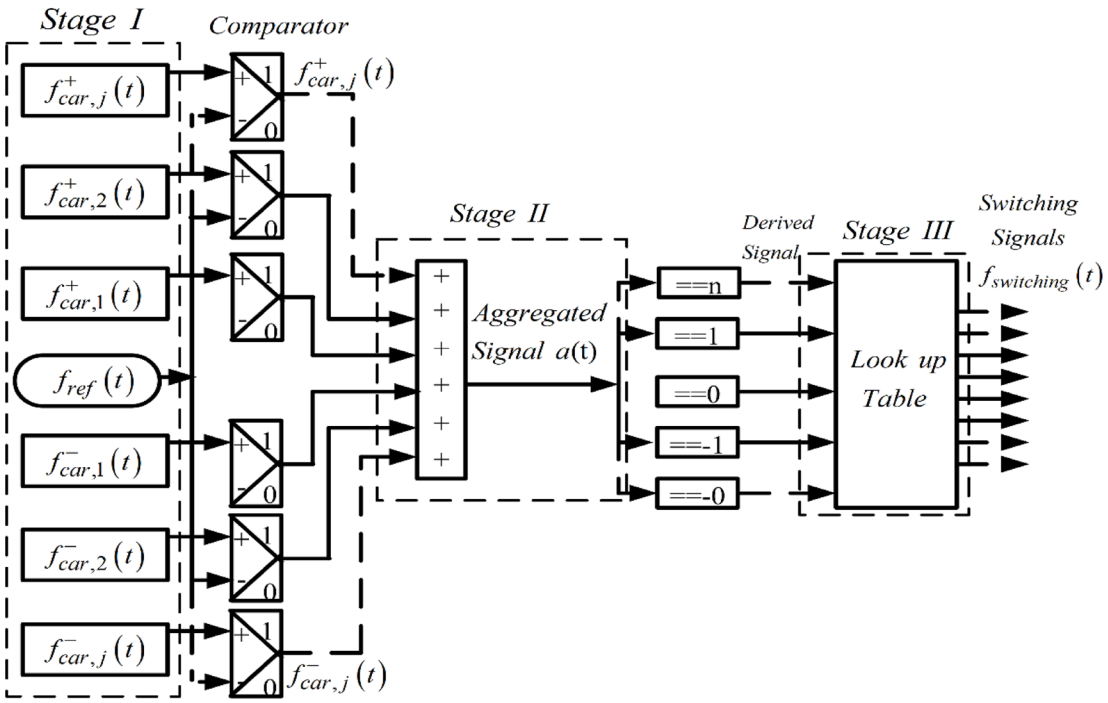


Figure 7. Schematic of modulation control strategy.

Table 2. SPIMD parameters.

Power (P)	1 HP	Stator resistance (R)	4.1 Ω
Voltage (V)	220 V	Rotor resistance (R)	4.1 Ω
Frequency (f)	50 Hz	Mutual Inductance (Lm)	782.7 mH
Speed (ω_r)	1500 rpm	Stator and Rotor Inductance (Ls, Lr)	808.1 mH
Current (i)	1.8 Amp.	Moment of inertia (J)	.0088 Kg-m^2
Capacitor	2500 µF	MOSFET switch	1200 V, 30 A

This is accomplished by using 'N-1' triangular carrier signals for a 'N' level MLI at f_s=3150 Hz. The required gate pulses are then generated by comparing these signals to a modulating sinusoidal reference signal with a frequency of f_m=50 Hz. Figure 7 provides an accurate illustration of the proposed modulation control strategy.

5.2. Analysis of simulation results

To model the proposed PUC 5-level inverter fed SPID, we utilize the MATLAB/SIMULINK environment. Table 2 lists the high-power drive parameters. We compare the performance of the proposed 5-level PUC with the traditional CHB MLI using simulation results.

The 5-level output voltage of the PUC and CHB MLIs are shown in Figures 8 and 9, respectively. A non-sinusoidal supply with a 5th harmonic component of V_{5ref}=200V at 200 Hz is introduced to test the drive's performance under unbalanced conditions. Figure 9 shows that the CHB inverter cannot minimize the x-y axis harmonic components, resulting in distinct 5th harmonic components in the machine.

Figures 10 and 11 compare the current per phase of two proposed drives. During peak voltage, the machine's back electromotive force causes the existence of the 5th harmonic. In contrast to the proposed PUC MLI, the CHB inverter drive cannot minimize the x-y axis harmonic components,

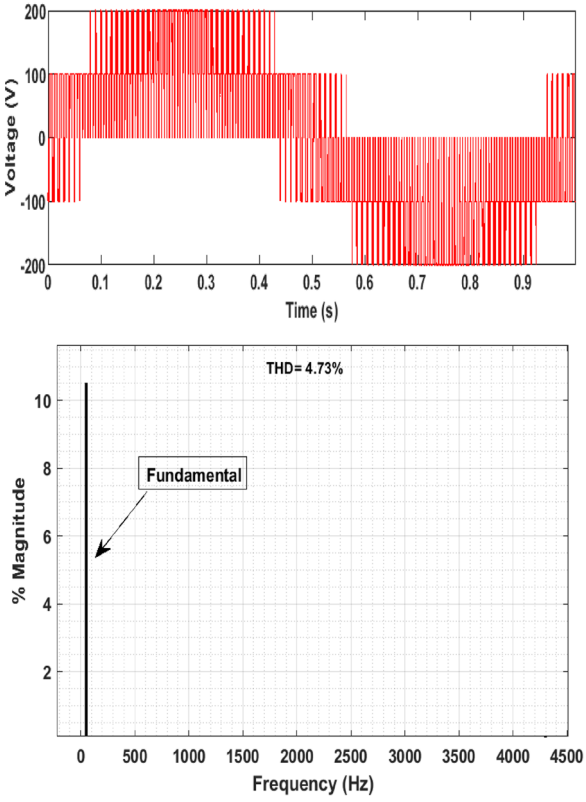


Figure 8. Stator phase voltage using 5-level PUC MLI.

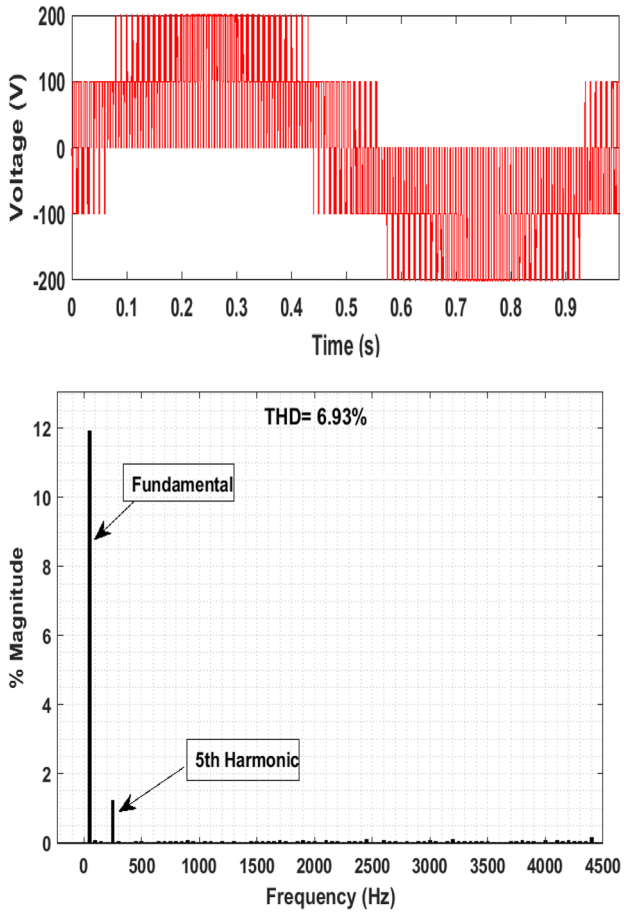


Figure 9. CHB MLI 5-level stator phase voltage.

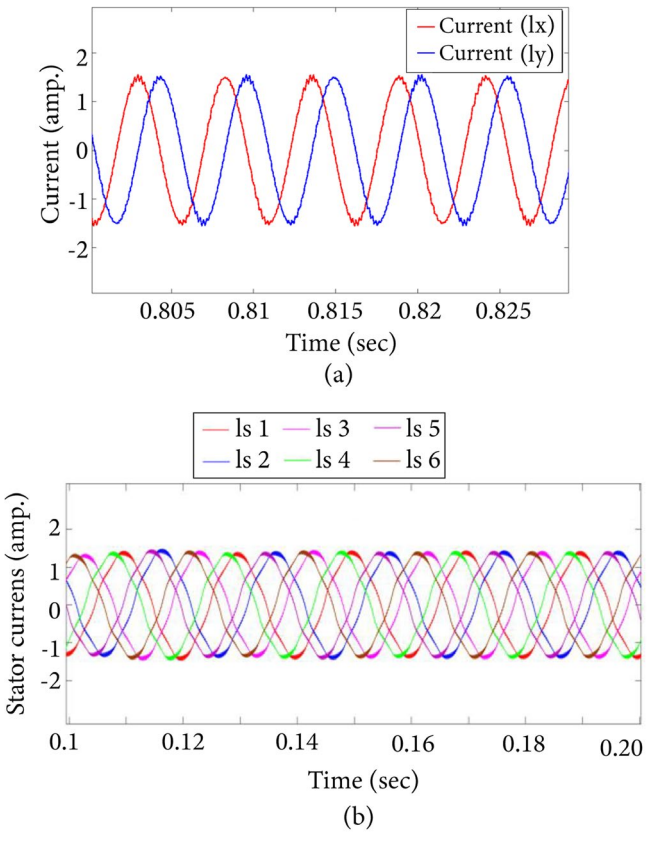


Figure 10. SPID currents using PUC MLI (a) *x-y* sub-space and (b) Steady-state.

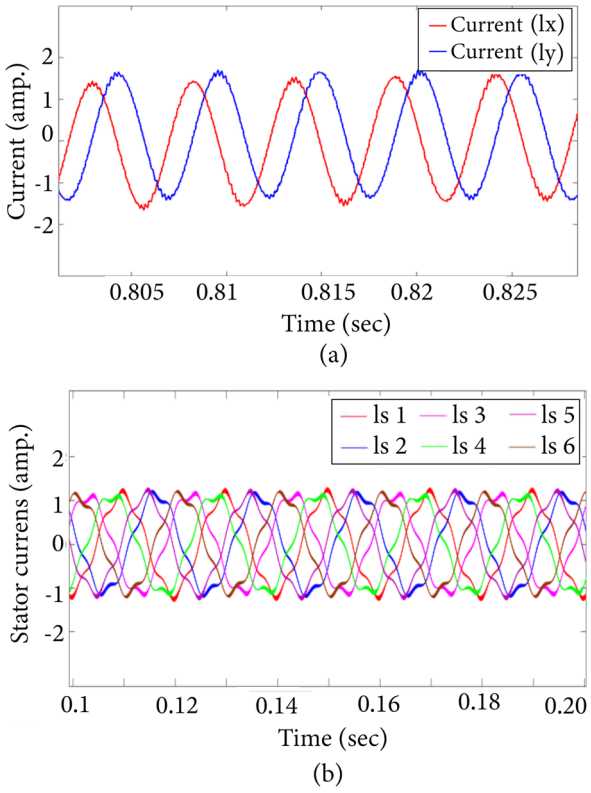


Figure 11. SPID currents using CHB MLI (a) *x-y* sub-space and (b) Steady-state.

resulting in the 5th harmonic, as demonstrated in Figure 11. However, Figure 10 shows that with the PUC MLI, the current can be controlled through a closed-loop while maintaining a DC bus voltage of V_{dc}=200 V and a machine reference speed of 1470 rpm.

The simulation results of both cases confirm the successful implementation of the proposed scheme. The following section will provide additional support through experimental validation.

5.3. Description of the test rig

The system prototype includes high-rated semiconductor switches, specifically MOSFET (IRF640NSTRLPBF), capable of withstanding 1200 V voltage and 30 A current for the 5-level inverter. An isolator (MCT2E) is used to get the gate pulses. Two MOSFET switches connected in parallel and operated by a single DC-link split the five-level, six-phase PUC inverter legs into two sections. In this case, the control pulses required to activate the switches are produced by the real-time controller dSPACE DS1104 device. These pulses are then delivered to the gate drive circuit TLP250 (F). The amplified voltages of -5V and +5V are used to satisfy the MOSFET voltage requirements. The voltage and current readings, which are utilized to control the drive, are sensed by the voltage sensor LV 10-1000 and the current sensor LEM manufacture LA 25 NP, respectively. Before being connected to the real-time platform attached to the host PC, the suggested MLI is modelled using the MATLAB/Simulink program. The relevant harmonics are recorded using FLUKE43B, and all waveforms are recorded using the Yokogawa power analyzer scope DL750E. Figure 12 displays an image of the entire test setup.

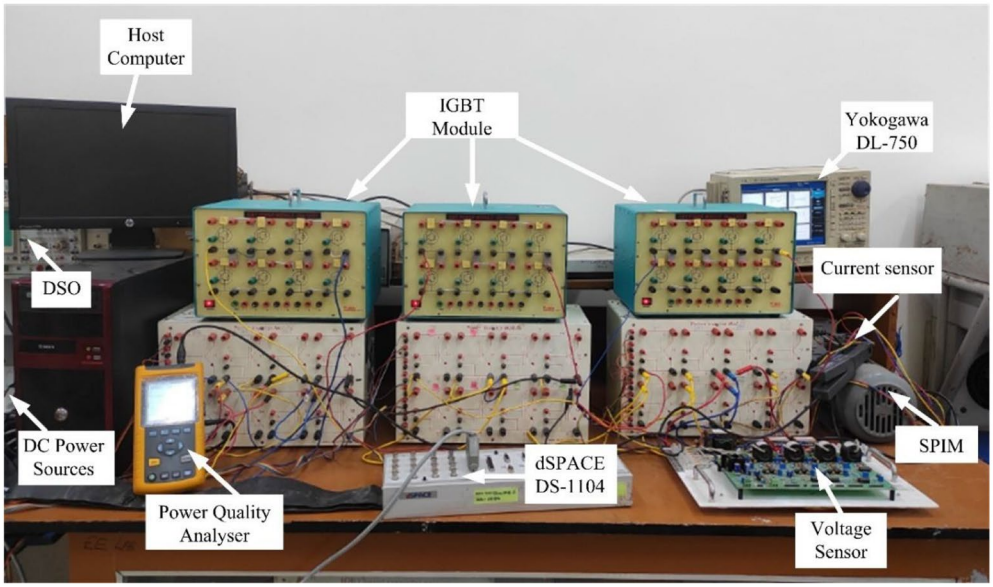
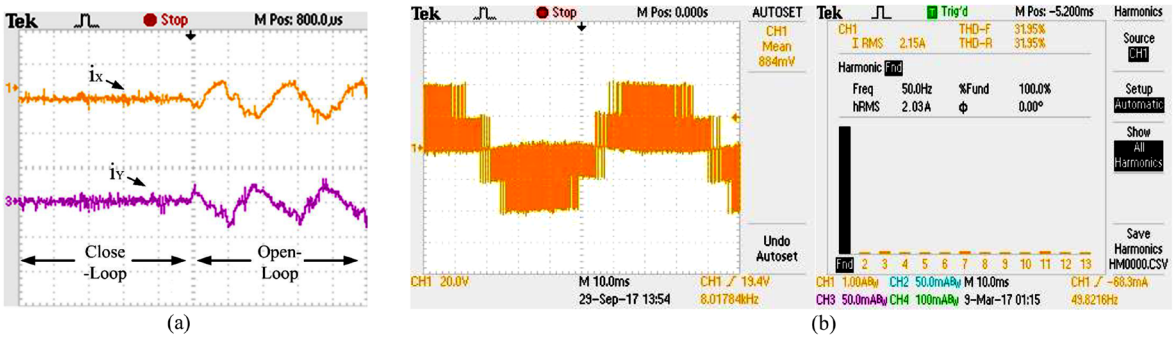


Figure 12. General test rig.



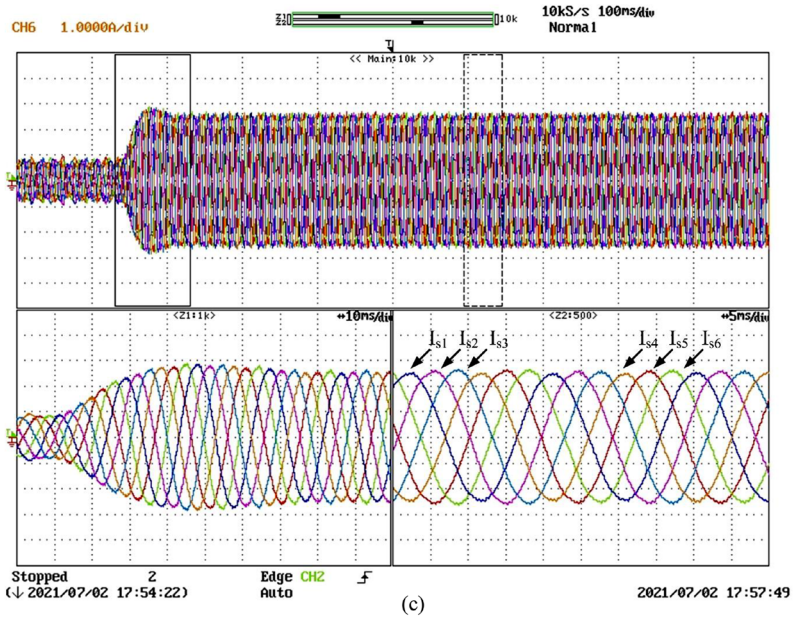
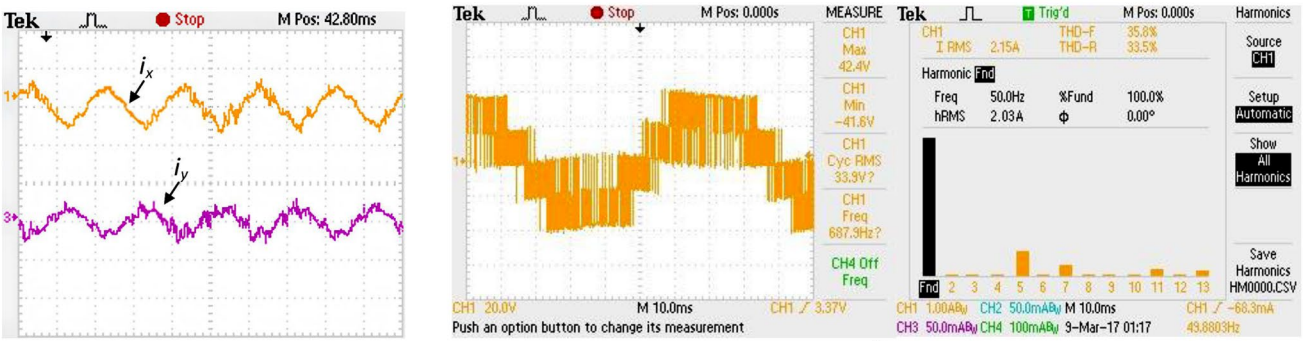


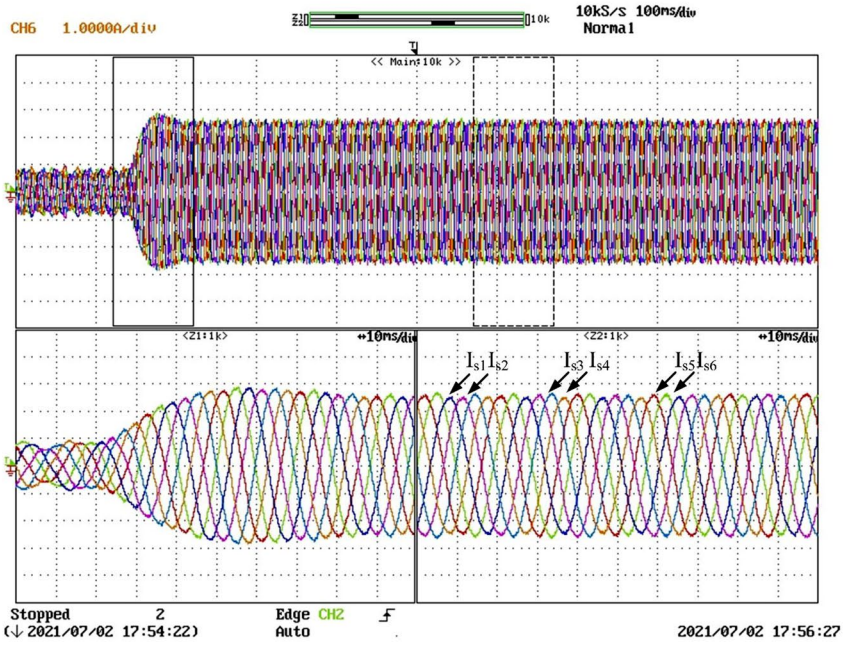
Figure 13. PUC MLI (a) *x-y* axis current, (b) phase voltages, and (c) six-phase currents.

5.4. Description analysis of hardware results

The SPID's performance with the 5-level PUC MLI is depicted in Figure 13 during steady-state. With a load torque of 12 Nm, the machine rotates at 1470 rpm. The current fluctuation on the *x-y* sub-space is depicted in Figure 13(a), and the inverter's 5-level output voltage is shown in Figure 13(b). Due to the non-identical characteristics of the six-phase windings in real applications, there is an apparent fundamental-frequency oscillation in the current components in the *x-y* sub-space without the closed-loop

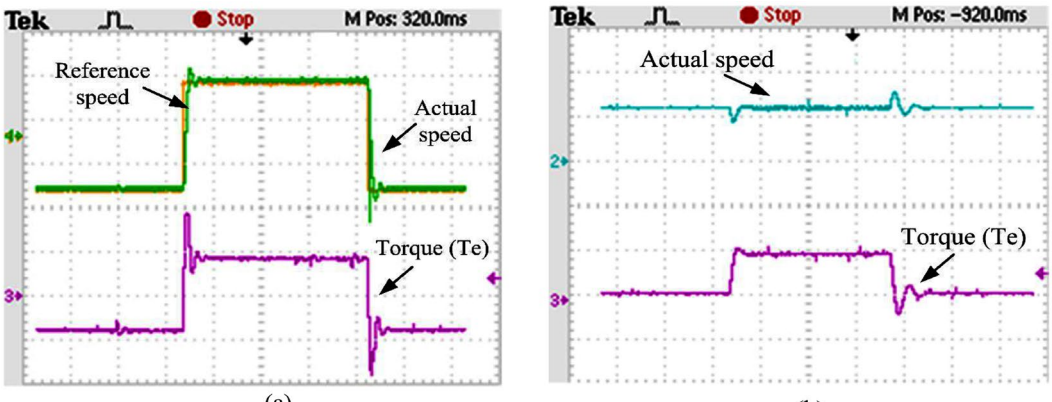


(a) (b)



(c)

Figure 14. CHB MLI (a) *x-y* axis current, (b) phase voltages, and (c) six-phase currents.



(a) (b)

Figure 15. Dynamic characteristic of the proposed drive (a) speed and (b) torque.

current controller. However, the oscillation is effectively suppressed after applying the closed-loop current controller on the *x-y* sub-space. The proposed MLI was useful in suppressing these oscillating current components. Figure 13(c) shows the six-phase symmetrical current of the drive.

Figure 14 displays the SPID's steady-state performance using a standard CHB MLI. The 5-level output voltage of the inverter is illustrated in Figure 14(b), and the waveform of the typical technique fails to suppress harmonic components, resulting in a distinct current component on the *x-y* plane. As a result, as shown in Figure 14(c), the SPID employing the traditional SVM technique exhibits asymmetrical current.

Figure 15 displays the suggested PUC MLI's dynamic reaction to the drive. Based on the response shown in

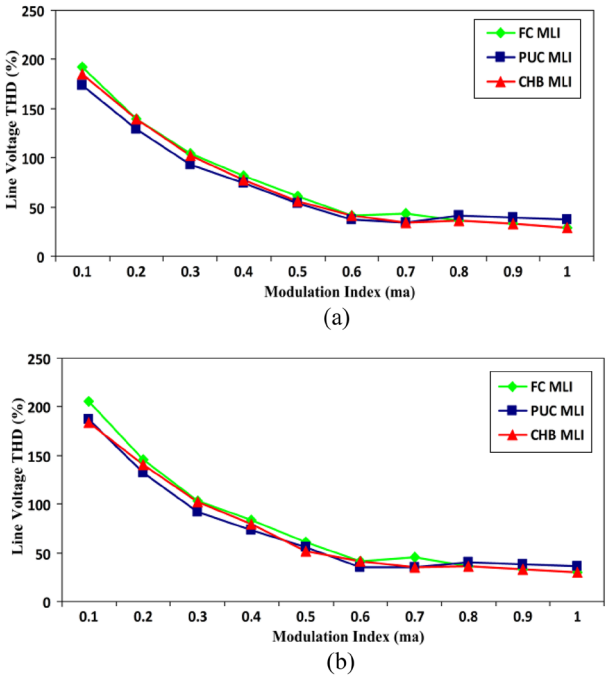


Figure 16. Line voltage THD comparison (a) simulation and (b) experimental.

Figure 15(a), it is evident that the speed precisely matches the reference speed at a load torque of 12 Nm. In Figure 15(b), the variation in load torque is depicted while maintaining the drive speed at the reference speed. The torque in this situation ranges from no load to 12 Nm. The response's correctness shows that employing the suggested MLI to construct drives produces a satisfactory dynamic response.

This study compares the performance of two different drives based on their efficiency and THD. A comparative performance study of the SPID fed with other MLIs has been performed to show the proposed MLI's effectiveness. Compared to the CHB and FC MLI, the PUC inverter has a faster computation time. The proposed MLI offers prospective advantages like the digital implementation of the DC-link voltage and the capacity to function during fault without the additional switching circuits. At a 50 Hz output frequency, we used a resistive-inductive load with a resistance of 12 Ω and an inductance of 8 mH to analyze the harmonic features of the inverter voltage.

5.5. Comparison of THD

The Using PUC, FC, and CHB MLI, Figures 16 and 17 compare the THD between line-to-neutral voltage and phase voltages. The curve unmistakably demonstrates that at ma values below 0.7, the proposed MLI has a lower THD than the other systems. When the m_a is more than 0.8, it does, however, offer a relatively high THD. It is projected that the suggested MLI will reduce system complexity and calculation time compared to previous approaches based on experimental and simulation results.

The proposed inverter has numerous benefits, including fast digital implementation, effective use of DC-link voltage and accurate switching operation. Table 3 compares the efficiency of the three inverters, primarily affected by switching and conduction losses. When a device is turned on or off, switching losses occur. These losses depend on the

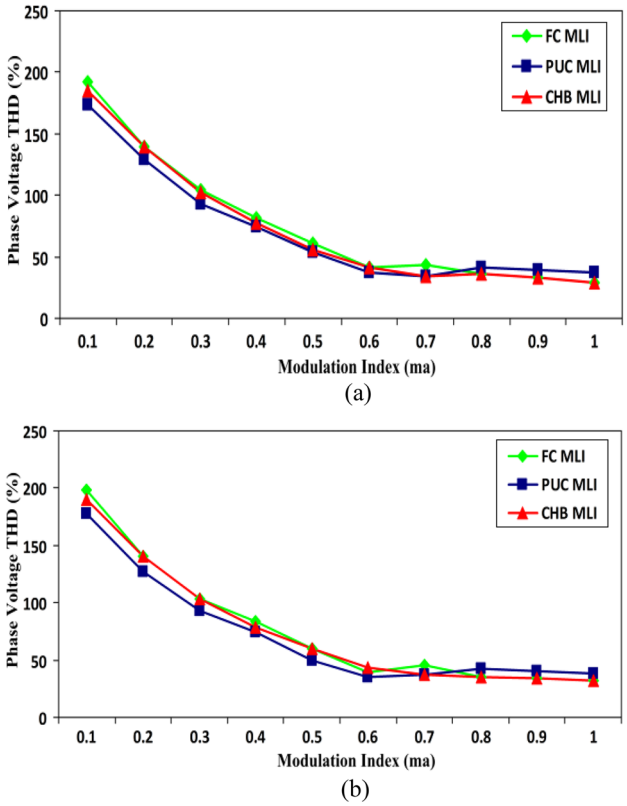


Figure 17. Phase voltage THD comparison (a) simulation (b) experimental.

Table 3. Comparison between the Proposed PUC, FC, and CHB MLIs.

Input power (W)	Power loss (W)			Efficiency (%)		
	CHB	PUC	FC	CHB	PUC	FC
225.9	17.1	16.8	16.2	90.9	91.8	91.3
293.1	20.6	21.6	21.1	92.7	93.0	93.3
329.9	24.2	22.7	23.6	93.1	94.3	94.2
392.7	27.8	25.7	26.2	94.3	94.9	94.6
430.2	30.8	30.1	29.5	95.2	96.1	95.9

current and voltage across the device and the total commutation time. Conduction losses, however, are influenced by the device's saturation voltage and the instantaneous current flowing through it Wiechmann et al. [31]. The device's average current and saturation voltage are measured to determine conduction losses, and input and output power are simulated to estimate efficiency. According to our estimates, switching losses outweigh conduction losses, but the three MLIs' conduction losses are nearly identical, resulting in equivalent efficiency for the proposed MLI, FC, and CHB MLI.

6. Conclusion

This research presents the performance analysis of a Six-Phase Induction Drive (SPID) using a 5-level Packed U Cells (PUC) Multilevel Inverter (MLI). The new MLI creates an output voltage waveform with five symmetric levels and maintains the voltage of the capacitor at half the value of the DC source thanks to a sensor less self-capacitor voltage balancing control. This technique simplifies the control system, accelerates computation, and enables independent regulation of 5-level dual three-phase inverters' voltages using the input DC voltage. If there is an imbalance, the

modulation limit is attained, and the back EMF-derived current components are stopped. Unlike CHB MLI, mathematical advancements and numerical modelling are verified using experimental tests. Lastly, a resistive-inductive load is utilized to evaluate the inverter's voltage Total Harmonic Distortion (THD) performance based on PUC, CHB, and FC MLIs. The proposed five-level PUC MLI delivers superior performance at low modulation indices, but may lead to a slight increase in THD at high indices.

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Conflicts of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Authors contribution statement

Frist author

Vishal Rathore: Conceptualization; Data curation; Investigation; Methodology; Validation; Visualization; Roles/Writing – original draft; Writing – review and editing.

Second author

Dhananjay Kumar: Formal analysis; Resources; Software

Third author

Krishna Bihari Yadav: Supervision

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