A 4-X Gain 9-Level Multilevel Inverter Topology with Reduced Part Count

[*1]Kasinath Jena, [2]Krishna Kumar Gupta, [3]Dhananjay Kumar

[*1]Department of Electrical and Electronics Engineering, ARKA JAIN University, Jharkhand, India, Email; kasi.jena@gmail.com
[2]Department of Electrical & Instrumentation Engineering, Thapar Institute of Engineering & Technology Patiala, India, Email;kkg.manit@gmail.com
[3]Department of Electrical Engineering, Government Engineering College, Siwan, India, Email; dhananjaymanit23@gmail.com
.

***Abstract*- This research presents a new quadruple boost 9-level single-phase switched-capacitor (SC) inverter. The proposed topology (PT) comprises eight semiconductor switches, two capacitors, one power diode, and a single supply source unit that can synthesize nine voltage levels at the output terminal. A brief description of structural design, operating principle, modulation strategy, and determination of optimum values of the capacitances are presented in this work. Simulation and experimental studies have been carried out under different loading conditions to validate the effectiveness of the PT. Further, a comparative fair survey with state-of-the-art SC topologies regarding component count per level, gain, total standing voltage, and cost function proves the merits of the suggested novel work.**

Index words- Cost function, Multilevel Inverter, Switched-capacitor, Total Standing Voltage.

I. INTRODUCTION

In recent years, multilevel inverters (MLIs) have received wide attention from the research and academic community due to the improved waveform, lower total harmonic distortion, low power losses, and absence of transformer or magnetic circuits [1-4]. Conventional multilevel inverters (CMLIs) are commonly categorized as neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB). However, these inverters have several drawbacks: unbalanced capacitor voltage (both for NPC and FC inverters), a larger number of active and passive components for higher voltage levels (i.e., more than three levels), complex control, and unity voltage gain. The significant issues of larger switching components of CMLIs can be solved by reduced switching component counts [5]. However, it also needs voltage-boosting ability; these topologies are unsuitable for applying non-conventional energy sources (like photovoltaic (PV), wind, and fuel cells) and electric vehicles. Voltage boosting is a critical requirement for grid-tied systems because the voltage output from renewable energy sources is typically low. To achieve the necessary voltage levels, either a front-end boost converter or a back-end magnetic circuit/transformer is commonly employed. However, integrating a magnetic circuit with the boost converter increases the system's size, weight, cost, and inefficiency, making it less practical for certain applications [6].The challenges mentioned above can be effectively resolved by implementing the switched-capacitor-based series/parallel approach. This approach has several advantages, such as greater voltage gain than unity, self-balancing of capacitor voltage, absence of transformer or magnetic circuit, and modular structure. Because of these advantages, the research community has concentrated more on the evolution of SC topologies in the last few years. Additionally, SCMLIs can be classified into single-stage and two-stage SC topologies. Two-stage configurations require a back-end H-bridge (HB) to produce a bipolar voltage level. However, the maximum load voltage values are equal to the PIV of the four HB switches. This feature limits its application in high-voltage applications [7-11].

The generation of bipolar voltage at the output terminal is accomplished without any back-end HB in single-stage designs. Besides, all the switches total voltage stresses are also reduced. Capacitor voltage has an intrinsic self-balancing capability, and voltage gain is four in the 9-level structure, as stated in [12–15]. Nevertheless, these topologies possess a greater quantity of switching components. Besides, the 9-level structural design presented in [16-17] and [18-19] lacks voltage boosting ability, i.e., restricted within one.

Additionally, relatively larger numbers of active and passive components have been used. Triple gain 7-level topology advocated in [20-22] has more component counts. A single-stage 9-level SC inverter incorporating an enhanced T-type inverter referenced in [23]. The above design minimizes the blocking voltage of the switches, the number of power components, and the DC-link capacitor voltage. The two 17-level SCMLIs that were produced by combining SC units with an NPP circuit had the same number of components [24]. An SCMLI with 17 levels has a capacitor voltage ripple (CVR) but quadruples voltage gain. The BF and CVR of the alternate 17-level SC-MLI are cut in half.

In reference [25], a generalized inverter with ($2n + 5$) levels was shown. This inverter consists of n SC units. A CHBMLI, based on SC technology, has been suggested to tackle the current leakage problem. This configuration necessitates only one DC power source and offers the possibility to increase voltage [26]. A transformerless grid-connected inverter utilizes six power switches and two power diodes to generate six distinct voltage levels at its output [27]. Additionally, the proposed inverter effectively addresses the issue of leakage current.

This article [28] introduces a six-level SCMLI achieving 2.5x VG from a single DC source, designed for compact, transformerless PV systems with minimized line filters. The MLI features capacitor voltage balance, reduced harmonics, and closed-loop control for effective grid integration, achieving a peak efficiency of 95.79%. This study [29] introduces a five-level SC inverter specifically designed for PV applications. It effectively eliminates leakage current by directly connecting the DC bus to the grid's neutral point. The proposed topology offers features such as self-voltage balancing, reactive power handling, and optimal utilization of the DC bus.Simulation and experiments demonstrate its practical advantages over conventional inverters. This article[30] presents a nine-level ANSCMLI with a minimized capacitor charging current, enhancing its sensible use. A modified switching sequence reduces switching loss, improving efficiency to 98.03% at 583.91 W. Experimental results confirm stable capacitor voltages and reduced losses under various loads. The article[31] introduces a six-level transformerless inverter for grid-connected PV systems, addressing leakage current issues and offering VB without an added boost converter. Key features include reduced filter size, lower THD, and full reactive power support. A 770 W lab prototype validates its performance and practical feasibility. This article[32] proposes a flexible multilevel topology for open-end winding motor drives, similar to CHB inverters, combining three-phase and single-phase HB inverters. The modular design allows easy voltage level extension, enabling higher motor voltages or lower DC voltage use. Experimental tests validate its performance and compatibility with SPWM modulation. The seven-level achieves a voltage gain of just 1.5 MLI, described in [33] and [34], using ten switches, two diodes, and three capacitors.
Nevertheless, it requires components with a high rating due to its high TSVpu. Achieving voltage increases of 2.0 and 1.0 are also detailed in [35] and [36] for the common ground five-level MLI. This study presents a single-source, high-voltage-gain SCMLI to overcome these restrictions. With its flexible architecture, the suggested six-level SCMLI can handle various tasks. The paper introduces a five-level active-NPC SCMLI designed for unity gain, inrush current reduction, and active balancing of the DC-link capacitor voltage. Minimizing switching losses achieves an efficiency of 98.04% at 510 W [37].

The preceding paragraphs inspire us to develop a 9-level SC inverter that incorporates the following essential characteristics:

(a) Boosting ability, i.e., the gain is 1:4
(b) A single direct current voltage source can generate a voltage waveform with nine levels.
(c) The reduced number of switches counts per level
(d) Capacitor voltages have self-balancing features.
(e) Only half of the switches are activated in each switching state.

Next to this section, the proposed work has been organized in the following way. The structural design, working principle, self-balancing mechanism of capacitors voltage, and determination of the optimum value of capacitance of the proposed work are presented in section II. A suitable logic gate modulation scheme is described in section III. The analysis of losses in the PT is conducted in section IV. Comparative studies with the SCMLIs are represented in section V to verify its merits. Simulation and hardware results verify the suggested topology effectiveness presented in section VI. Lastly, the conclusion is highlighted in section VII.

II. PROPOSED 9-LEVEL SC INVERTER TOPOLOGY

(A) Structural design and its operation

Figure 1 shows the simple 9-level SC structural design of the *PT*. It consists of two kinds of nine power switches (IGBTs) (one with an anti-parallel diode and the other without an anti-parallel diode), two capacitors, and one power diode. Five different sets of switches, namely (S_1S_2, S_3S_4, S_5S_6, S_6S_7, and S_8S_9) are designed to function in a complementary manner to prevent short circuits with the input supply voltage and maintain less complexity of the switching scheme.

The PT generates 9- output voltage level (0, $\pm 1V_{DC}, \pm 21V_{DC} \pm 3V_{DC} \pm 4V_{DC}$) with a peak value four times the supply inputs, i.e., $4V_{DC.}$ Table I presents the valid switching combinations corresponding to the different operational states, while Table II outlines the voltage and current stresses experienced by each switch. Capacitor charging and discharging are indicated by "Δ" and "∇," respectively, while idle states are represented by "-."The corresponding circuit design illustrated in Figure 2 depicts the PT main features for various states.

(B) Self-balancing mechanism of capacitor voltage

The PT uses a series/parallel combination of capacitors to self-balance the capacitor voltage [8]. The following is a list of the conditions that must be met for capacitors to be charged and discharged at different levels.

For 0 and $\pm 1V_{DC}$ output voltage levels, the capacitor C_1 is brought in parallel with the input source through the path $S_5 - V_{DC} - D - S_7$ and charged to $1V_{DC}$, as shown in the state-1,state-2,state-6, and state-7, respectively. The capacitor C_1 discharges its stored energy to load when it is connected in series with the input source for the voltage levels$\pm 2V_{DC}$, $\pm 4V_{DC}$. This feature of charging and discharging capacitor voltage for different voltage levels makes it self-balanced to V_{DC} automatically. Similarly, the capacitor C_2 charged to $2V_{DC}$ when it brought in the path $S_3 - S_6 - V_{DC} - D$ during the output voltage level $\pm 2V_{DC}$ as mentioned in Fig.2, state-3 and state-8. The capacitor C_2 discharges its energy to the load for the voltage level $\pm 3V_{DC}$ and$\pm 4V_{DC}$. Multiple times of charging and discharging of the capacitor C_2 occurs for different voltage levels in one cycle of the load voltage. Therefore, the voltage of the capacitor C_2 is maintained at $2V_{DC}$ automatically.

(C) Determination of capacitance

The capacitance plays a significant role in SCMLI design. During the discharging period, the voltage across the capacitor drops, i.e., known as voltage ripple. The performance of the design is impacted by the voltage ripple that the capacitor produces. Therefore, an optimum capacitance value is necessary to improve performance [7]. Henceforth, the voltage ripple (ΔV) for C_1 and C_2 of

the PT can be expressed for a purely resistive load as

$$\Delta V_1=\frac{1}{\omega C_1}\int_{\theta_1}^{\theta_2} i_l\, d\theta+\frac{1}{\omega C_1}\int_{\theta_3}^{\pi-\theta_3} i_l\, d\theta \quad (1)$$

$$\Delta V_1=\frac{1}{\omega C_1}\int_{\theta_1}^{\theta_2} \frac{2V_{DC}}{R}\, d\theta + \frac{1}{\omega C_1}\int_{\theta_3}^{\pi-\theta_3} \frac{4V_{DC}}{R}\, d\theta \quad (2)$$

$$\Delta V_1=\frac{V_{DC}}{\omega C_1 R}[4\pi - 2\theta_1 - 2\theta_2 - 8\theta_3] \quad (3)$$

$$\Delta V_2=\frac{1}{\omega C_2}\int_{\theta_2}^{\theta_3} i_l\, d\theta+\frac{1}{\omega C_2}\int_{\theta_3}^{\pi-\theta_3} i_l\, d\theta \quad (4)$$

$$\Delta V_2=\frac{V_{DC}}{\omega C_2 R}[4\pi - 3\theta_2 - 5\theta_3] \quad (5)$$

Where $\theta_1, \theta_2, \theta_3$ can be obtained from Fig 3 as

$$\theta_1 = \frac{\sin^{-1}\left(\frac{1}{4}\right)}{2\pi f} \quad (6)$$

$$\theta_2 = \frac{\sin^{-1}\left(\frac{2}{4}\right)}{2\pi f} \quad (7)$$

$$\theta_3 = \frac{\sin^{-1}\left(\frac{3}{4}\right)}{2\pi f} \quad (8)$$

It is important to note that the quantity of discharging that occurs in the capacitor is dependent upon the longest discharging time (($\theta_x - \theta_y$), load current (i_l) and power factor. Therefore, the discharging amount (ΔQ) of a capacitor can be calculated as

$$\Delta Q_i = \int_{\theta_x}^{\theta_y} i_l \sin\theta\, d\theta \quad (9)$$

As a result, the values that are appropriate for the capacitors C_1 and C_2 are represented as follows:

$$C_1 \geq \frac{\Delta Q_1}{\Delta V_1} \quad (10)$$

$$C_2 \geq \frac{\Delta Q_2}{\Delta V_2} \quad (11)$$

$$\Delta Q_{C1} = \frac{1}{2\pi f}\int_{\theta_1}^{\pi-\theta_1} i_l \sin\theta d\theta \quad (12)$$

$$\Delta Q_{C2} = \frac{1}{2\pi f}\int_{\theta_2}^{\pi-\theta_2} i_l \sin\theta \, d\theta \quad (13)$$

III. CONTROL SCHEME OF THE INVERTER

Various control strategies are utilized to operate the inverter. The multicarrier level-shifted PWM technique is applied in the PT. The switching pulse is generated by comparing eight carrier signals $(e_1\_e_8)$ with a sinusoidal reference signal (f_{ref}). All carriers share identical peak-to-peak amplitudes and frequencies.

Figure 4 illustrates the modulation method that is appropriate for the positive half-cycle.

Modulation of the negative half-cycle can also be accomplished similarly. The driving pulses for switches from S_1 to S_9 using 'OR' gates can be written as:

$$S_1 = y_1 + y_2 + y_3 + y_5 + y_4 \quad (14)$$
$$S_2 = x_1 + x_2 + x_3 + x_5 + x_4 \quad (15)$$
$$S_3 = x_3 + y_3 \quad (16)$$
$$S_4 = x_4 + x_5 + y_4 + y_5 \quad (17)$$
$$S_5 = x_1 + x_2 + x_4 + y_1 + y_2 + y_4 \quad (18)$$
$$S_6 = x_3 + x_5 + y_3 + y_5 \quad (19)$$
$$S_7 = x_1 + x_2 + y_1 + y_2 \quad (20)$$
$$S_8 = x_4 + x_2 + x_3 + y_5 + y_1 \quad (21)$$
$$S_9 = x_1 + y_2 + y_3 + y_4 + y_5 \quad (22)$$

IV.POWER LOSSES CALCULATION

The investigations of substantial power losses in SCMLIs are categorized into three groups. This section provides an extensive analysis of these losses.

(a)Switching losses:

Power switches experience switching losses whenever turned on and off [20]. These losses are expressed as:

P_{s_on}, P_{s_off} are the terms used to describe the power losses associated with the switch on and off, respectively.

$$P_{s\_on} = \frac{f_0}{6} V I_{s\_on} t_{on} \quad (23)$$

$$P_{s\_off} = \frac{f_0}{6} V I_{s\_off} t_{off} \quad (24)$$

Finally, the total switching losses:

$$P_s = \sum (P_{s\_on} + P_{s\_off}) \quad (26$$

f_0 : fundamental frequency.

t_{on}, t_{off} : turn-on/off time.

V : blocking state voltage.

I_{s_on}, I_{s_off} : currents that flow through the switches after and before they are turned on and off, as appropriate.

(b) Conduction losses (P_C):

The internal resistance of the transistors generates this sort of loss.(R_s) and diodes (R_d) [20]. The losses resulting from switches and diodes can be quantified in numerical terms as follows:

P_{s_c}=$V_{s\_on}I_{s\_avg} + R_{s\_on}I^2_{s\_rms}$ (27)

P_{d_c}=$V_{d\_on}I_{d\_avg} + R_{d\_on}I^2_{d\_rms}$ (28)

Overall conduction losses(P_C) = $P_{s\_c} + P_{d\_c}$ (29)

An on-state resistance value for the transistor or diode is represented by R_{s_on} and R_{d_on}

V_{s_on},V_{d_on}: on-state voltage drop across the transistor and diode, respectively.

The rms and average currents through switches are denoted by $I^2_{s\_rms}$ and I_{s_avg} .

Average and rms diode current, respectively, are I_{d_avg} and $I^2_{d\_rms}$

(c) Ripple losses (P_r):

Equations (7&8) describe the loss during capacitor charging/ discharging [6].

$P_r = \frac{f_r}{2} C(\Delta V_C^2)$ (30)

The overall effectiveness can be represented as follows:

$\% \eta = \frac{P_{out}}{(P_{out} + total\ losses)} \times 100$ (31)

V.SIMULATION AND EXPERIMENTAL RESULTS

The proposed 9-level boost inverter topology has been evaluated through both simulation and experimental testing to confirm its effectiveness. The main parameters utilized for conducting the simulation and experimental studies are summarized in Table III.

(a) SIMULATION RESULTS

The MATLAB/Simulink environment is used to validate theoretical concepts. Figure 5(a-b) shows the simulation results for the RL load. When a step change in the load is introduced, it is observed that the output voltage remains steady at 9 distinct levels. The maximum magnitude of the load voltage is $4V_{DC}$

The voltage across capacitors C_1 and C_2 is automatically adjusted to achieve a balanced state and is maintained at $1V_{DC}$ and $2V_{DC}$, respectively, as depicted in Figure 5(a). Figure 5(b) displays the voltage and current stresses experienced by switches S_9 and S_3. It verifies that the charging path exhibits a greater current than the other switches.

(b) EXPERIMENTAL RESULTS

Experimental testing has been conducted using a laboratory prototype model shown in Figure 6 to verify the performance of the proposed 9-level topology.

The experimental findings for an RL load with a modulation index (MI) of 0.95 are shown in Figure 7. The results show how well the system works when the RL load is constant and when there is a sudden change, as illustrated in Figure 7(a). There are nine separate levels to the output voltage, as seen in the figure. The voltages across capacitors C_1 and C_2 denoted as V_{C1} and V_{C2}, are equalized, with V_{C1} measuring 10V and V_{C2} measuring 20V. The peak voltage is 40V for both the constant load and the load with a step change. The peak current is 1.2A for the continuous load and 1.9A for the load with a step change. This diagram shows that the currents lag the voltage when an RL load is present.

Figure 7(b) illustrates the variation in switching frequency for the RL load when using 500Hz and 2kHz. It is evident from the graph that altering the switching frequency does not impact the number of output voltage levels. Figure7 (c) shows the results of RL load evaluations using three different modulation indices: 0.95, 0.50, and 0.25. The graph shows that the number of output voltage levels is directly affected by the modulation index (*MI*) change. For *MI* values of 0.95, 0.5, and 0.2, the graph shows 9, 5 and 3 output voltage levels, respectively. The magnitude will decrease as the *MI* is reduced while keeping the load constant. The voltage stress of various switches is illustrated in Figure 6 (d-e).

The efficiency study for output power ranging from 50W to 350W is presented in Fig. 6(f). The graph illustrates the relationship between efficiency and output power. According to Figure 7(f), the *PT* achieves a maximum efficiency of 95.85% at an output power of 200W. At an output power of 350W, the efficiency tested was 94.7%. Figure 7(g) also shows the experimental results of the PT with a unity power factor. In this case, capacitors are naturally self-balancing; it has been noted that the output voltage stays constant at nine levels.

(c) Applications

The PT generates a 9-level output waveform with a voltage gain quadrupled, as evidenced by both modelling and experimental confirmation. The PT has been shown to minimise power losses in the switching components. The review of the current literature on SCMLIs has identified the subsequent practical uses for this proposed configuration:

(i) High-frequency ac distribution:

High-frequency alternating current (HFAC) power distribution systems (PDS) have become increasingly popular in applications requiring high power density, such as telecommunications [36-37], spacecraft, and computer systems [38].This preference is primarily due to their ability to reduce the size of transformers substantially, the number of power conversion stages, and the filtering components. Another emerging application for HFAC PDS includes localized networks, such as electric vehicles, buildings, and microgrids [39]. The adoption of SCMLI topologies enables low-voltage regions to eliminate the need for DC-DC boost converters or magnetic circuits.

(ii)Photovoltaic (PV) based power generation systems and electric vehicle (EV) Traction systems:

Solar power systems and other renewable energy sources can provide very little electricity. Methods such as deploying step-up transformers, DC-DC boost inverters, or cascading photovoltaic (PV) modules are commonly used to increase the voltage. Nevertheless, these methods lead to larger systems, higher costs, and more energy losses [40]. However, SCMLIs have several benefits, including being compatible with the grid, producing high-resolution waveforms, reducing the need for filtering, and increasing voltage gain [41–42]. Although electric vehicle (EV) systems that use cascade cells can attain high DC-link voltage, it also brings new issues, like charge balancing, which need to be addressed [43-45]. Researchers are looking at SCMLIs as a possible option for converting low-voltage DC to high-voltage AC in order to fix these issues with conventional EV drive systems [45-46].

VI. COMPARISON WITH SC TOPOLOGIES

A fair comparative analysis has been made with the other single-source SC topologies having the same levels to prove the benefit of the *PT*. Table V illustrates a reasonable comparison. The primary goal of the proposed topology is to produce enhanced waveforms by using fewer active and passive components, minimizing the cost, and providing voltage-boosting capability. The *PT* uses only nine switches, two capacitors, and one diode to generate quadruple voltage gain. The topologies presented in [3][6][10][16-19][23] have more switching

components with the least voltage gain than the *PT*. Quadruple boosting topologies advocated in [7-9] and [12- 15] require more switching components. The topology [14] also has the same capacitor number as the PT. Additional capacitors of the topologies [12-13], [15], [7-9] resulted in high costs, more losses, and complexity in charging and discharging.

Further, two parameters, component count and the cost function of the *PT*, are less than the other topologies, proving the merit of the structural design. The component count per level is defined as the total sum of active and passive components divided by the number of levels, and it can be represented as follows:

$$F_{C/L} = \frac{(N_{sw} + N_c + N_d + N_{dri})}{N_l} \quad (32)$$

The cost function is defined by [23]

$$CF = \frac{(N_{sw} + N_d + N_{dri} + N_c + \alpha * TSV) \times N_s}{N_l} \quad (33)$$

The significance of the *TSV* or switching components determines the weight coefficient "α". "α" is either greater or lesser than one according to the importance of the *TSV* or switching components. When both the parameter *TSV* and switching components are given equal importance, the PT weight coefficient is considered as one (α=1) [23].

$$F_{C/L} = \frac{(N_{sw} + N_c + N_d + N_{dri})}{N_l} \quad (34)$$

The cost function is defined by [23]

$$CF = \frac{(N_{sw} + N_d + N_{dri} + N_c + \alpha * TSV) \times N_s}{N_l} \quad (36)$$

The significance of the TSV or switching components determines the weight coefficient α. α is either greater or lesser than one according to the importance of the TSV or switching components. When both the parameter TSV and switching components are equally important, the PT weight coefficient is considered one (α=1) [23].

The statistics presented in Table IV and Table V unequivocally demonstrate that the PT exhibits a diminished CF, mostly attributable to its decreased number of components and operates at a lower voltage stress, leading to enhanced efficiency. Based on the information provided, it is evident that the PT offers advantages in several areas: a reduced quantity of power devices, compatibility with inductive loads, automatic balancing of capacitor voltage, and reliance on a single input source. These improvements are beneficial for expanding the range of applications for the inverter. Table VI presents the cost comparison analysis of the PT. It is observed that the PT demonstrates the lowest cost compared to the alternatives.

VII.CONCLUSION

The PT offers a simple structural design SC topology that achieves quadruple voltage gain. The suggested topology provides several advantages, including automatic balancing of capacitor voltage during charging and discharging and the efficient operation of only 50% of switches for any voltage level. A thorough comparison analysis established the PT benefits regarding component counting, cost function, and voltage gain. Both simulation and experimental work were conducted under various loading conditions to validate the suggested topology efficacy.

REFERENCES

[1] Rodriguez J., Lai J.-S., and Peng F. Z., "Multilevel inverters: a survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Nov.2002. doi: 10.1109/TIE.2002.801052.

[2] Cardoso R. d. B., da Silva E. R. C., et al., "A seven-level inverter with natural balance and boosting capability," in IEEE Transactions on Industry Applications, vol. 59, no. 1, pp. 925-937, Jan.-Feb. 2023, doi: 10.1109/TIA.2022.3205882

[3] Pal P. K., Jana K. C., Siwakoti Y. P., et al. "A Switched-capacitor multilevel inverter with modified pulsewidth modulation and active DC-link capacitor voltage balancing," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 12, no. 2, pp. 1215-1229, April 2024, doi: 10.1109/JESTPE.2023.3285690.

[4] Duong T. D., Lim Y. C. and Choi J. H., "A switched-capacitor-based six-level inverter," in IEEE Transactions on Power Electronics, vol. 37, no. 4, pp. 4804-4816, April 2022, doi: 10.1109/TPEL.2021.3127440.

[5] Gupta K. K., Ranjan A., Bhatnagar P., et al. "Multilevel inverter topologies with reduced device count: a review," IEEE Trans. Power Electron., vol. 31, no. 1, pp. 135–151, Jan.2016. doi: 10.1109/TPEL.2015.2405012.

[6] B. Chandan, P. K. Pal, K. C. Jana et al., "Performance evaluation of a new transformerless grid-connected six-level inverter with integrated voltage boosting," in IEEE Journal of Emerging and Selected Topics in Power Electronics, 2024 doi: 10.1109/JESTPE.2024.3427766.

[7] Hinago Y. and Koizumi H., "A switched-capacitor inverter using series/parallel conversion with inductive load," IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 878-887, Feb. 2012. doi: 10.1109/TIE.2011.2158768.

[8] Ye Y., Cheng K. W. E., Liu J., etal. "A step-up switched-capacitor multilevel inverter with self-voltage balancing," IEEE Trans. Ind. Electron., vol. 61, no. 12, pp. 6672-6680, Dec. 2014. doi: 10.1109/TIE.2014.2314052.

[9] Babaei E. and Gowgani S. S., "Hybrid multilevel inverter using switched capacitor units," IEEE Transactions on Industrial Electronics, vol. 61, no. 9, pp. 4614–4621, Sep. 2014. doi: 10.1109/TIE.2013.2290769.

[10] Pal P. K., Jana K. C., Siwakoti Y. P., et al., "An active-neutral-point-clamped switched-capacitor multilevel inverter with quasi-resonant capacitor charging," in IEEE Transactions on Power Electronics, vol. 37, no. 12, pp. 14888-14901, Dec. 2022, doi: 10.1109/TPEL.2022.3187736.

[11] Barzegarkhoo R., Moradzadeh M., Zamiri E., et al., "A new boost switched-capacitor multilevel converter with reduced circuit devices," IEEE Trans. Power Electron., vol. 33, no. 8, pp. 6738-6754, Aug. 2018. doi: 10.1109/TPEL.2017.2751419.

[12] Y. Nakagawa and H. Koizumi, "A boost-type nine-level switched capacitor inverter," in IEEE Transactions on Power Electronics, vol. 34, no. 7, pp. 6522-6532, July 2019, doi: 10.1109/TPEL.2018.2876158.

[13] Liu J., Lin W., Wu J. et al., "A novel nine-level quadruple boost inverter with inductive-load ability," IEEE Trans. Power Electron. doi 10.1109/TPEL.2018.2873188.
[14] Sandeep N., Ali J. S. M., Yaragatti U. R., et al., "Switched-capacitor-based quadruple boost nine-level inverter," IEEE Transactions on Power Electronics, vol. 34, no. 8, pp. 7147–7150, Aug. 2019. doi: 10.1109/TPEL.2019.2898225.
[15] Taghvaie A., Adabi J., and Rezanejad M., "A self-balanced step-up multilevel inverter based on switched-capacitor structure," IEEE Trans. Power Electron., vol. 33, no. 1, pp. 199–209, 2018. doi: 10.1109/TPEL.2017.2669377.
[16] Zeng J., Wu J., Liu J., et al., "A quasi-resonant switched-capacitor multilevel inverter with self-voltage balancing for single-phase high-frequency ac microgrids," IEEE Trans. Ind. Inform., vol. 13, no. 5, pp. 2669–2679, Feb.2017. doi: 10.1109/TII.2017.2672733
[17] Siddique M. D. et.al."A new single phase single switched-capacitor based nine-level boost inverter topology" IEEE Access, Vol. 7, pp. 174178 – 174188, Dec.2019, doi: 10.1109/ACCESS.2019.2957180.
[18] Bhatnagar P., Agrawal R., Dewangan N.K., et al."Switched capacitors 9-level module (SC9LM) with reduced device count for multilevel DC to AC power conversion " IET Electric Power Applications, Vol. 13, no. 10, pp. 1544 – 1552, Oct. 2019. doi.org/10.1049/iet-epa.2019.0053
[19] Sandeep N. and Yaragatti U. R., "Operation and control of an improved hybrid nine-level inverter," IEEE Trans. Ind. Appl., vol. 53, no. 6, pp. 5676–5686, Nov. 2017. doi: 10.1109/TIA.2017.2737406.
[20] Siddique M. D., Mekhilef S., Shah N. M., et al."A new switched-capacitor 7L inverter with triple voltage gain and low voltage stress," IEEE Trans. Circuits Syst. II Express Briefs, pp. 1–1, July 2019. doi: 10.1109/TCSII.2019.2932480
[21] Lee S. S., "A single-phase single-source 7-level inverter with triple voltage boosting gain," IEEE Access, vol. 6, pp. 30005–30011, May 2018. doi: 10.1109/ACCESS.2018.2842182
[22] Peng W., Ni Q., Qiu X., et al. "Seven-level inverter with self-balanced switched-capacitor and its cascaded extension" IEEE Transactions on Power Electronics. IEEE Transactions on Power Electronics, vol. 34, no,12, pp. 11889 - 11896, March 2019. doi: 10.1109/TPEL.2019.2904754.
[23] Sathik M J., Almakhles D. J., Sandeep N., et al., "Experimental validation of new self-voltage balanced 9L-ANPC inverter for photovoltaic applications," Sci. Rep., vol. 11, no. 1, 2021, doi: 10.1038/s41598-021-84531-z.
[24] Ye Y., Chen S., Hua T., et.al., "Self-balanced multilevel inverter with hybrid double- and half-mode switched-capacitor," IEEE Trans. Ind. Electron., vol. 69, no. 6, pp. 5735–5744, Jun. 2022, doi: 10.1109/TIE.2021.3086725.
[25] Barzegarkhoo R., Lee S. S., Khan S. A., et al. "A novel generalized common-ground switched-capacitor multilevel inverter suitable for transformerless grid-connected applications," in IEEE Transactions on Power Electronics, vol. 36, no. 9, pp. 10293-10306, Sept. 2021, doi: 10.1109/TPEL.2021.3067347.
[26] Kurdkandi N. V. Marangalu M.G. Mohammadsalehian S.et al., "A new six-level transformer-less grid-connected solar photovoltaic inverter with less leakage current," in IEEE Access, vol. 10, pp. 63736-63753, 2022, doi: 10.1109/ACCESS.2022.3182240.
[27] Jahan H. K., Abapour M., Zare K., et al. "A multilevel inverter with minimized components featuring self-balancing and boosting capabilities for PV applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 11, no. 1, pp. 1169-1178, Feb. 2023, doi: 10.1109/JESTPE.2019.2922415.
[28] Jena, K., Kumar, D., Singh, A.K., etal., " Single source multi gain 7-level switched-capacitor inverter topology with reduce device count"International Journal of Electronics Letters, vol.12,no.3, pp.256-269. doi.org/10.1080/21681724.2023.2267206
[29] Sandeep N., Sathik M. J., Yaragatti U. R., et.al, "Common-ground-Type five-level transformerless inverter topology with full DC-bus utilization," IEEE Trans. on Ind. Applicat., vol. 56, no. 4, pp. 4071-4080, July-Aug. 2020. doi: 10.1109/TIA.2020.2996152
[30] Jena, K., Kesh, R., Kumar, et al.. "Transformer-less multilevel inverter (TMLI) with reduced device count and voltage stress" e-Prime-Advances in Electrical Engineering, Electronics and Energy, vol.7, pp.100417. doi.org/10.1016/j.prime.2023.100417
[31] Jena, K., Panigrahi, C. K., & Gupta, K. K. "A new design self-balanced 13-level switched-capacitor inverter" International Journal of Circuit Theory and Applications, vol.50 no.4,pp-1216-1234,2022. doi.org/10.1002/cta.3200
[32] Pires V. F., Cordeiro A., Foito D., et.al. "Cascaded multilevel structure with three-phase and single-phase H-bridges for open-end winding induction motor drive," in IEEE Open Journal of the Industrial Electronics Society, vol. 4, pp. 346-361, 2023, doi: 10.1109/OJIES.2023.3309652.
[33] Jena, K., Panigrahi, C.K., Gupta, K.K., Kumar, et al. " Generalized switched-capacitor multilevel inverter topology with self-balancing capacitors." Journal of Power Electronics, vol.22, no.9, pp.1617-1626. doi.org/10.1007/s43236-022-00456-4
[34] Anand V., Singh V., and Ali J. S. M., "Dual boost five-level switched capacitor inverter with common ground," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 70, no. 2, pp. 556–560, Feb. 2023. doi: 10.1109/STPEC59253.2023.10431199.
[35] Baksi S. K. and Behera R. K., "A reduced switch count seven-level boost ANPC based grid following inverter topology with photovoltaic integration," IEEE Trans. Ind. Appl., vol. 59, no. 4, pp. 4238–4251, Jul./Aug. 2023. doi: 10.1109/TIA.2023.3259943
[36] Neti S. S., Singh V. and Anand V., "Common ground buck type five-level transformerless inverter with less stress," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 71, no. 4, pp. 2419-2423, April 2024, doi: 10.1109/TCSII.2023.3335148.
[37] Jena, K., Panigrahi, C.K. and Gupta, K.K., "Three-phase triple-gain switched-capacitor inverter with reduced component count"Electrical Engineering, vol.104no.5, pp.3547-3559,2022. doi.org/10.1007/s00202-022-01565-w
[38] Luo S. and Batarseh I., "A review of distributed power systems. Part II. High frequency AC distributed power systems," in IEEE Aerospace and Electronic Systems Magazine, vol. 21, no. 6, pp. 5-14, June 2006, doi: 10.1109/MAES.2006.1662037.
[39] Chakraborty S., Weiss M. D. and Simoes M. G., "Distributed intelligent energy management system for a single-phase high-frequency AC microgrid," in IEEE Transactions on Industrial Electronics, vol. 54, no. 1, pp. 97-109, Feb. 2007, doi: 10.1109/TIE.2006.888766.
[40] Kuncham S. K., Annamalai K. and Subrahmanyam N., "A two-stage T-type hybrid five-level transformerless inverter for PV applications," in IEEE Transactions on Power Electronics, vol. 35, no. 9, pp. 9510-9521, Sept. 2020, doi: 10.1109/TPEL.2020.2973340.
[41] Antaloae C. C., Marco J. and Vaughan N. D., "Feasibility of high-frequency alternating current power for motor auxiliary loads in vehicles," in IEEE Transactions on Vehicular Technology, vol. 60, no. 2, pp. 390-405, Feb. 2011, doi: 10.1109/TVT.2010.2092446.
[42] Kouro S. , M. Mariusz ,Gopakumar K. et al., "Recent advances and industrial applications of multilevel converters," in IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2553-2580, Aug. 2010, doi: 10.1109/TIE.2010.2049719.
[43] Jena K., Panigrahi C.K., Gupta K.K., et al. "A generalized transformerless switched-capacitor inverter for photovoltaic application" Electrical Engineering vol.104, pp.3435–3444 April.2022, doi.org/10.1007/s00202-022-01496-6

[44] Fong Y. C., Raman S. R., Ye Y. et al. "Generalized topology of a hybrid switched- capacitor multilevel inverter for high- frequency AC power distribution," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 3, pp. 2886-2897, Sept. 2020, doi: 10.1109/JESTPE.2019.2905421.
[45] Estima J. O. and Cardoso A. J. M., "Efficiency analysis of drive train topologies applied to electric/hybrid vehicles," in IEEE Transactions on Vehicular Technology, vol. 61, no. 3, pp. 1021-1031, March 2012, doi: 10.1109/TVT.2012.2186993.
[46] Dong B., Li Y. and Han Y., "Parallel architecture for battery charge equalization," in IEEE Transactions on Power Electronics, vol. 30, no. 9, pp. 4906-4913, Sept. 2015, doi: 10.1109/TPEL.2014.2364838.
[47] Jakkula S., Jayaram N., Pulavarthi S. V. K., et al., "A generalized high gain multilevel inverter for small scale solar photovoltaic applications," in IEEE Access, vol. 10, pp. 25175-25189, 2022, doi: 10.1109/ACCESS.2022.3152771.

Kasinath Jena received his B.E. degree in Electrical Engineering from Fakir Mohan University, India, in 2002 and M. Tech degree from Centurion University, Bhubaneswar, India in 1915. And completed his Ph.D degree from KIIT University Bhubaneswar, India in 2022. Currently working as associate professor in ARKA JAIN University, Jharkhand. His current research interests include Multilevel inverters and DC-DC converters and electric vehicle charging.

Krishna Kumar Gupta (Member, IEEE) received B.Tech. degree in electrical engineering, M.Tech. degree in power systems, and Ph.D. degree, all from the Maulana Azad National Institute of Technology, Bhopal, India, in 2005, 2007, and 2014, respectively. He is currently working with THAPAR University, India. His research interests include power electronics for renewable energy, multilevel inverters, and electric vehicle charging.

Dhananjay Kumar received his B.E. degree in Electrical and Electronics Engineering from the Lakshmi Narain College of Technology (LNCT), Bhopal, India; and his M.Tech. degree in Electrical Drives from the Maulana Azad National Institute of Technology (MANIT), Bhopal, India, in 2017, Completed his Ph.D degree from Maulana Azad National Institute of Technology (MANIT), Bhopal, India, in 2022.Working as assistant professor in Government Engineering College Siwan, Bihar. His current research interests include multilevel inverters and DC-DC converters.

Appendices

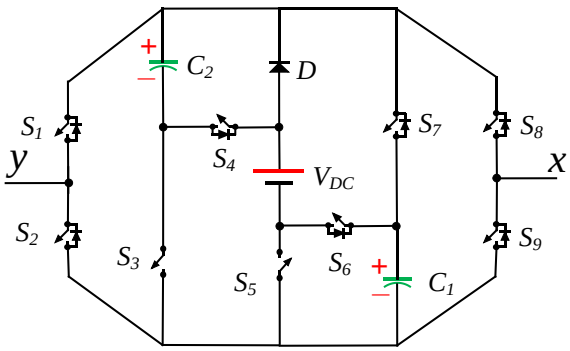
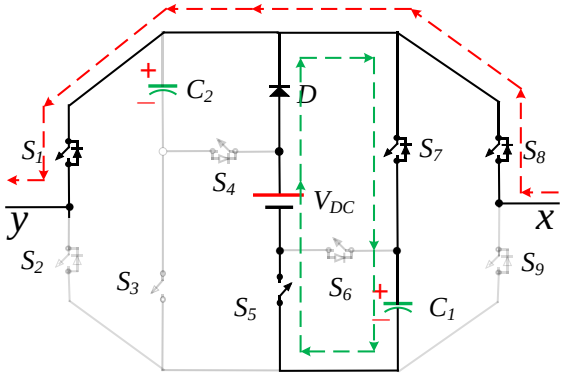
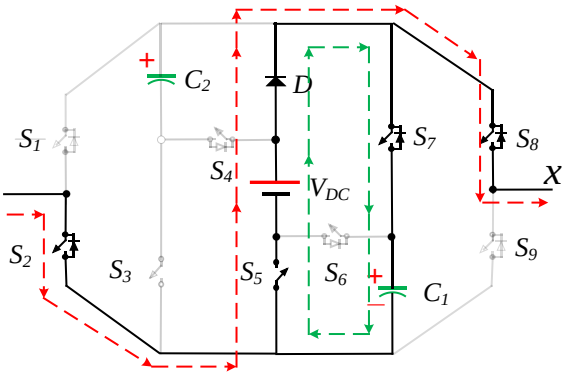


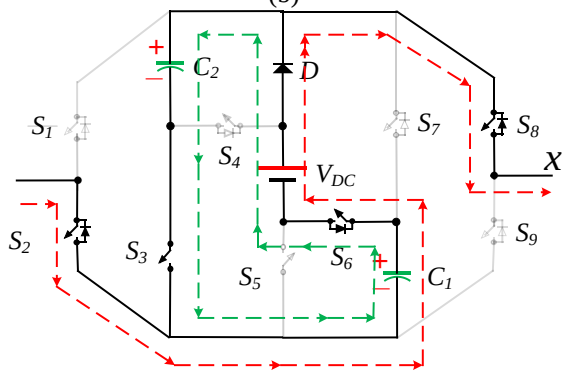
Figure 1 Simple 9-level SC structural design of the PT.


C2
D
S1
S4
VDC
S7
S8
y
x
S2
S3
S5
S6
C1
S9

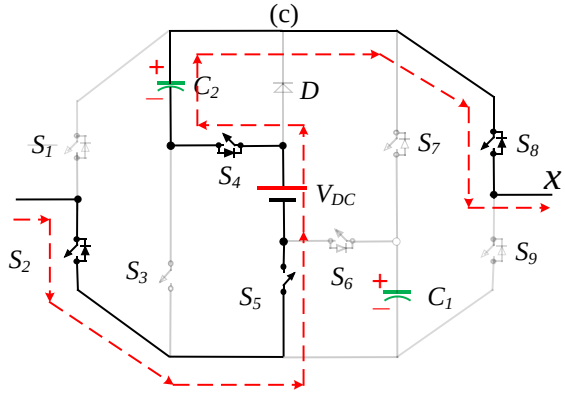
(a)


C2
D
S1
S4
VDC
S7
S8
x
S2
S3
S5
S6
C1
S9

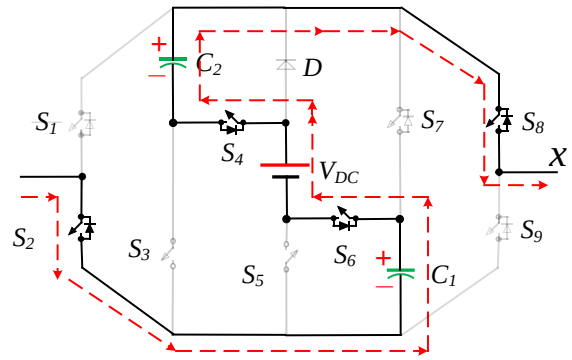
(b)


C2
D
S1
S4
VDC
S7
S8
x
S2
S3
S5
S6
C1
S9

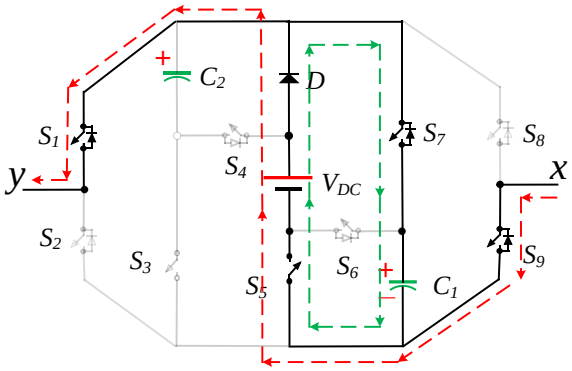
(c)


C2
D
S1
S4
VDC
S7
S8
x
S2
S3
S5
S6
C1
S9

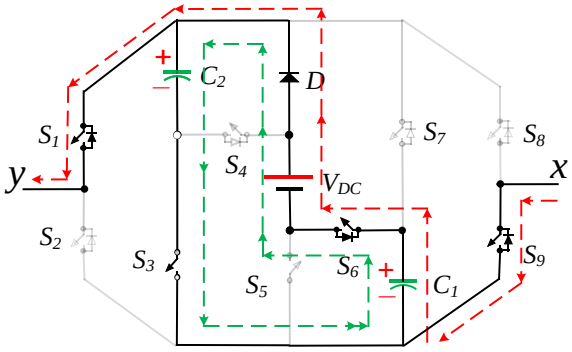
(d)


C2
D
S1
S7
S8
S4
VDC
x
S2
S3
S6
S9
S5
C1

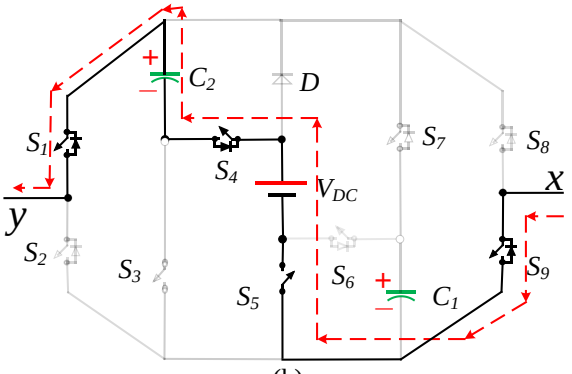
(e)


C2
D
S1
S7
S8
y
S4
VDC
x
S2
S3
S6
S9
S5
C1

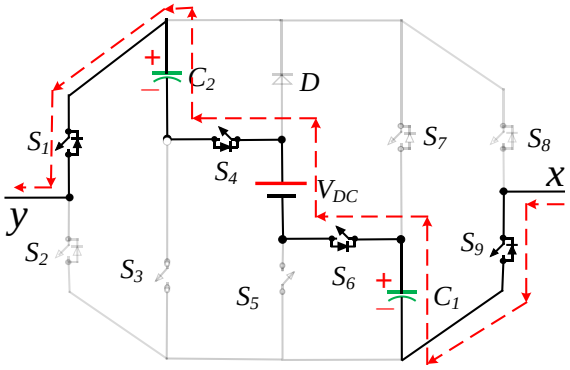
(f)


C2
D
S1
S7
S8
y
S4
VDC
x
S2
S3
S6
S9
S5
C1

(g)


C2
D
S1
S7
S8
S4
VDC
x
y
S2
S3
S6
S9
S5
C1

(h)



(i)

Figure 2 Operating states of the PT

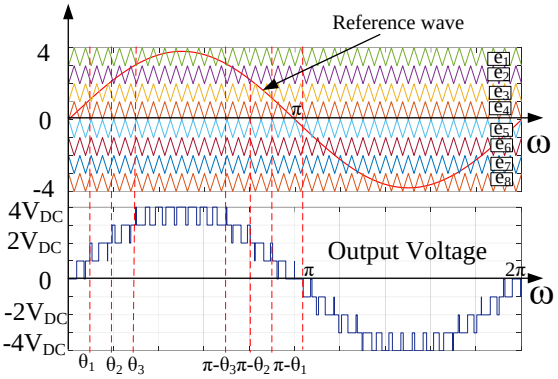


Figure 3 Discharging period of the capacitors.

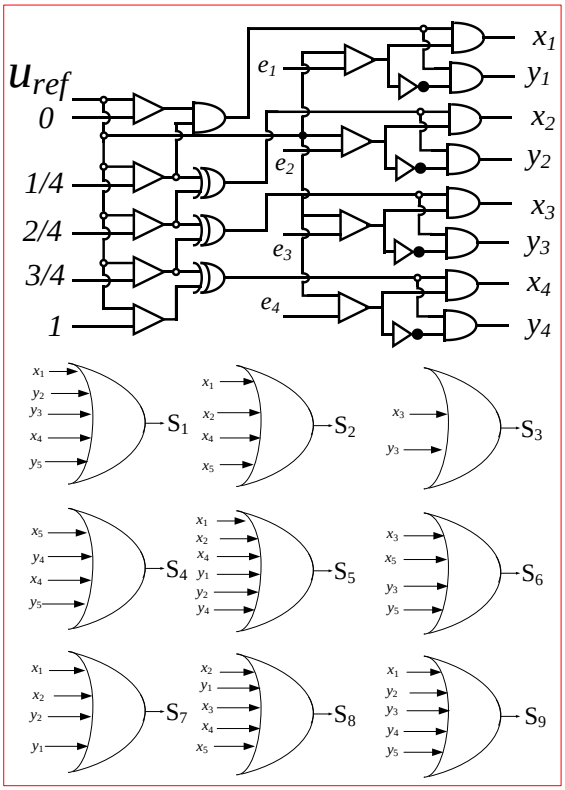


Figure 4 Control Scheme of the PT

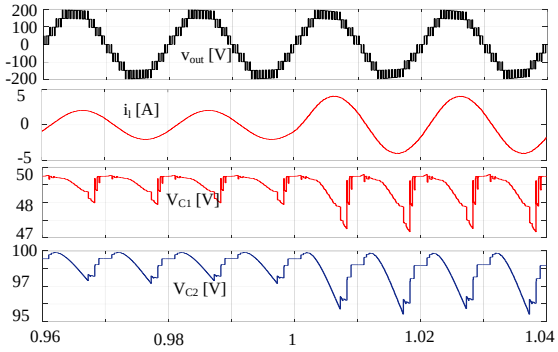


Figure 5 (a) Simulation results for RL-load

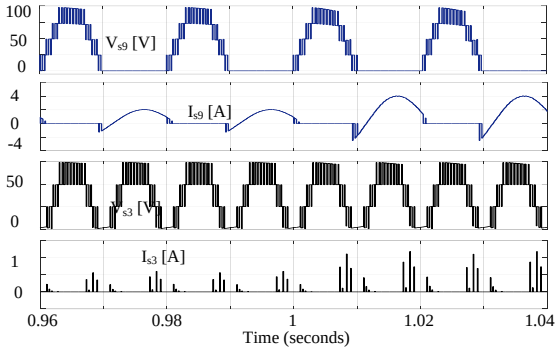


Figure 5 (b) Voltage and current stress of switch S_9 and S_3

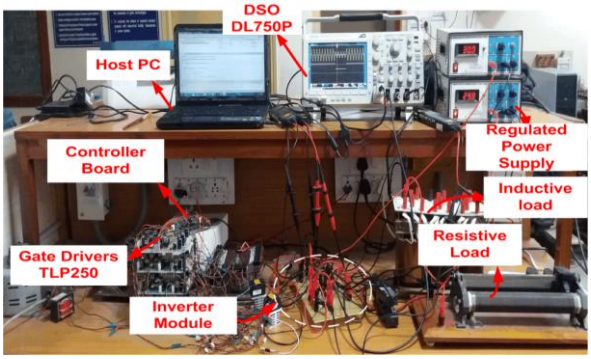
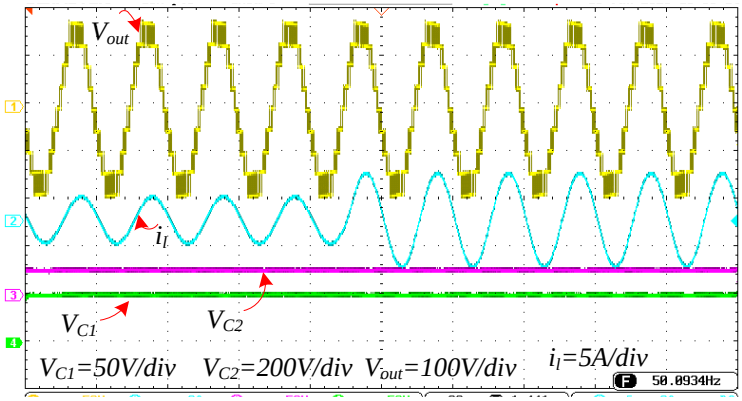
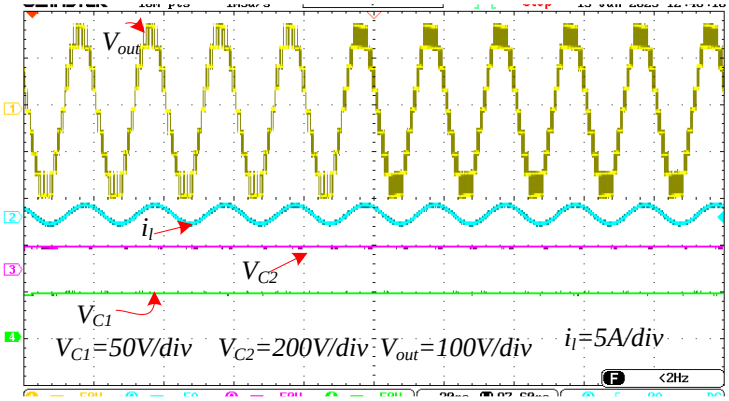


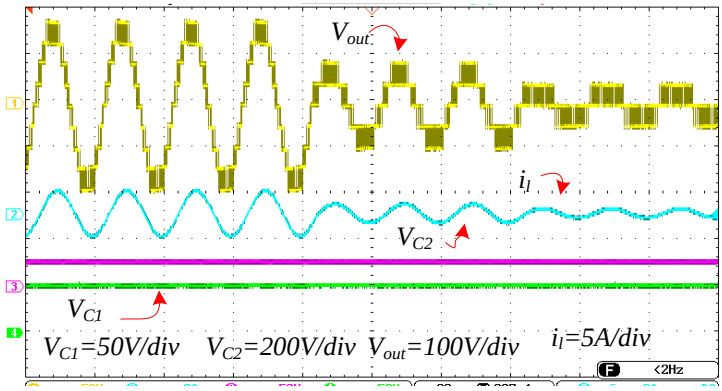
Figure 6 Prototype Module


V_{out}
i_l
V_{C1}
V_{C2}
V_{C1}=50V/div V_{C2}=200V/div V_{out}=100V/div i_l=5A/div
50.0934Hz

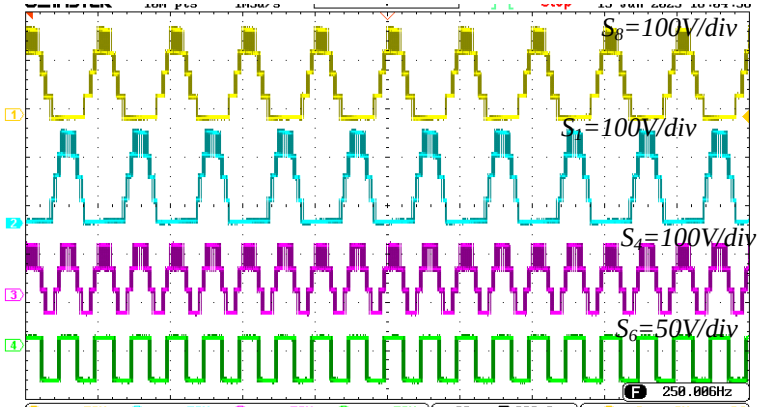
(a)


V_{out}
i_l
V_{C2}
V_{C1}
V_{C1}=50V/div V_{C2}=200V/div V_{out}=100V/div i_l=5A/div
<2Hz

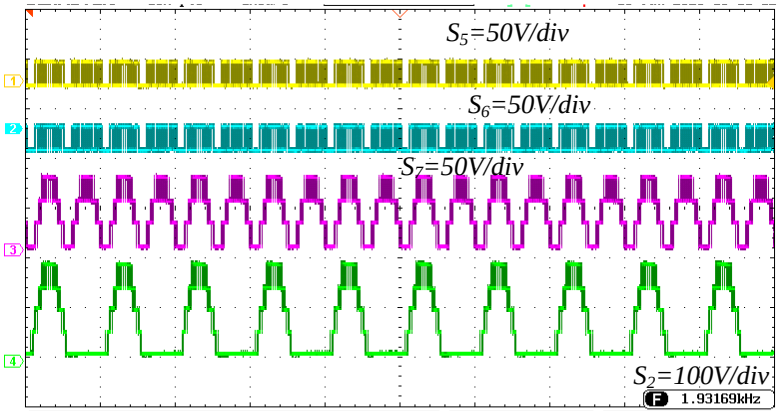
(b)


V_{out}
i_l
V_{C2}
V_{C1}
V_{C1}=50V/div V_{C2}=200V/div V_{out}=100V/div i_l=5A/div
<2Hz

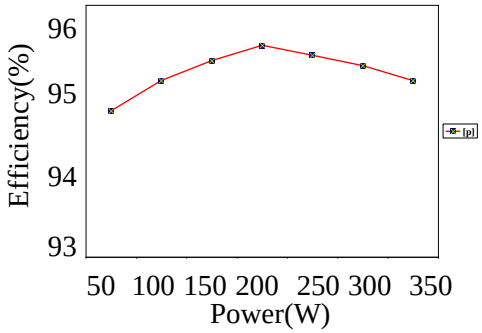
(c)


S_8=100V/div
S_1=100V/div
S_4=100V/div
S_6=50V/div
250.006Hz

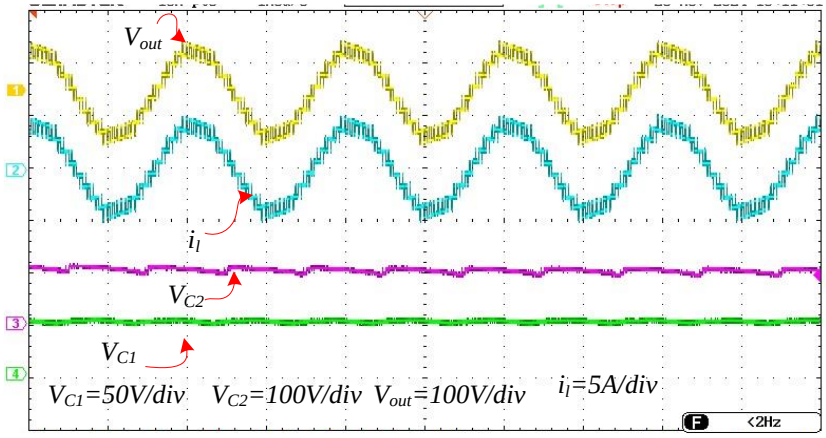
(d)



(e)



(f)



(g)

Figure 7 shows the experimental outcomes of the PT(a) change in load(b) change in switching(c) change in modulation index(d-e)voltage stress on individual switches(f) efficiency Vs power graph(g)At unity power factor

Table I Valid Switching Patterns

A	B	C	D	E

1	S_2, S_5, S_7, S_9	Δ	-	*0*
2	S_2, S_5, S_7, S_8	Δ	-	$+1V_{DC}$
3	S_2,S_3,S_6,S_8	∇	Δ	$+2V_{DC}$
4	S_2,S_4,S_5,S_8	-	∇	$+3V_{DC}$
5	S_2,S_4,S_6,S_8	∇	∇	$+4V_{DC}$
6	S_1 ,S_5,S_7,S_8,	Δ	-	*0*
7	S_1 ,S_5,S_7,S_9	Δ	-	$-1V_{DC}$
8	S_1 ,S_3 ,S_6, S_9	∇	Δ	$-2V_{DC}$
9	S_1 ,S_4 ,S_5, S_9	-	∇	$-3V_{DC}$
10	S_1 ,S_4 ,S_6, S_9	∇	∇	$-4V_{DC}$
A: State, B: Active switch, C: Effect of C_1, D: Effect of C_2, E: Output voltage, "-": idle				

Table II. Voltage And Current Stress Of The Individual Switches

Switches	Voltage stress	Current stress
S_1 ,S_2 ,S_8, S_9	$4V_{DC}$	i_{load}
S_7	$3V_{DC}$	i_{c1}
S_3 ,S_4	$2V_{DC}$	i_{c1}
S_5 ,S_6 ,	$1V_{DC}$	i_{c1}

Table III. Simulation & Experimental Parameters

Input supply (V_{DC})	50V
Capacitance (C_1)	$1100\mu F$
Capacitance (C_2)	$2200\mu F$
Modulation Index (*MI*)	0.95
Carrier frequency (f_c)	2kHz
Resistive-Inductive Load	80Ω-120mH
Fundamental frequency (f)	50Hz
IGBTs	IGW50N60T, IKW30N60T

Table IV. Comparison with recent SCMLI topologies

Ref	N_l	N_{sw}	N_d	N_c	N_{dri}	A	B	C	$F_{C/L}$	CF
[20]	7	12	-	2	11	5.3	2	3	3.57	4.32
[21]	7	16	-	2	15	5.3	1	3	3.57	5.47
[22]	7	8	2	2	8	6	3	3	2.85	3.71
[19]	9	12	-	3	12	6	1	1	3	3.66
[16]	9	10	4	4	10	19	1	1	3.11	5.22
[17]	9	11	-	3	10	5	1	2	2.66	4.14
[18]	9	11	-	2	11	5.2	1	2	2.66	3.24
[14]	9	10	-	2	10	4.5	2	4	2.44	2.94

[12]	9	12	-	3	12	6	4	4	3	3.66
[13]	9	8	3	3	8	5.7	4	4	2.44	3.07
[7]	9	13	8	3	13	6.3	4	4	3.22	3.92
[8]	9	8	6	3	8	8	4	4	2.77	3.66
[9]	9	10	3	3	10	6.3	4	4	2.88	3.58
[10]	9	10	4	4	10	8.5	1	1	3.11	4.1
[3]	5	10	-	4	10	11	1	1	4.8	7
[6]	6	7	2	4	6	6	2	2.5	3.16	4.16
[15]	9	19	3	3	19	4.8	1	4	4.88	5.42
[23]	9	9	8	4	9	8.25	1	1	3.33	4.25
[P]	9	9	1	2	9	6	4	4	2.33	3
[PT]: PT, A: TSV_{pu}, B: Max. Blocking voltage, C: Gain										

Table V. Efficiency analysis with the recent SCMLIs

Ref	N_l	N_{sw}	N_d	N_c	N_{dri}	A	B	CF	Efficiency
[16]	9	10	4	4	10	YES	1	5.22	93.3%
[13]	9	8	3	3	8	YES	4	2.72	93%
[8]	9	8	6	3	8	YES	4	3.66	91.6%
[11]	9	8	3	4	8	N0	1	3.58	92.8%
[15]	9	19	3	3	19	YES	4	5.42	88.9%
[PT]	9	9	1	2	9	YES	4	3.0	95.7%
A: $self-balancing$, B: Gain									

Table VI Cost comparison of 9-level topology with the PT

Component	Part Number	Rating	Unit price ($)	[47]	[15]	[12]	[17]	[PT]
MOSFET*	IGW50N60TFKSA1	600V, 100A	5.22	-	-			2
	IKW30N60TFKSA1	600V, 60A	5.24	-	-	2		4
	ISL9V5036P3-F085	390V, 46A	4.55	11	19	8	11	3
	IHW40N120R5	1200V, 80A	5.04	4				-
Diode*	VS-20ETF06SLHM3	600V, 20A	3.1	-	3			1
Capacitor*	ALF20G102KL600	600V, 1000μF	48.62		-			-
	ALS81H102DE350	300V, 1000μF	10.55		-	2	3	1
	ALF20G102EC200	200V, 1000μF	7.31	3	3	1		1
	ELG108M100AR2AA	100V, 1000μF	3.18					-
Gate driver	IR2110		1.8	15	19	8	11	9

		Total cost( )		119.14	151.8	89.65	101.5	82.21

*www.digikey.com