Development of a Three Phase Regenerative Programmable Electronic AC Load with Harmonic Load Emulation Capability

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Abstract: In this paper, the development of a three-phase AC regenerative programmable electronic load is presented. The AC load consists of two parts: a three-phase AC to DC current-controlled PWM voltage source converter as the programmable electronic load and a DC to AC grid-connected PWM voltage source inverter as the regeneration system. The AC to DC converter can operate in constant current, constant power, and constant impedance modes to emulate various load profiles. In the constant current mode, the system can emulate current harmonics with programmed amplitude and phase to emulate nonlinear load profiles. Due to its harmonic current control capability, a proportional-resonant current controller with harmonic compensators is used in the AC to DC converter. On the other-side, the DC to AC converter regulates the DC-link voltage and regenerates the power received by the electronic load by injecting it into the grid. To improve the robustness of the DC-link voltage control system against power oscillations caused by the electronic load in the constant current mode with harmonic current, the DC-link voltage controller is modified by adding a multi-frequency notch filter, and its performance is verified. Simulation and experimental results confirm the effectiveness of the proposed electronic load control system.

Keywords: ***Electronic AC load, harmonic load emulator, notch filter, PR current control***

1. Introduction

The burn-in test should be carried out to ensure appropriate efficiency and performance at the final stage of development of electrical equipment such as uninterruptible power supplies (UPS), AC power sources, and similar devices. Harmonic load emulation using the AC Programmable Electronic Load (AC-PEL) has received significant attention in recent years. Due to its programmable harmonic order, amplitude, and phase angle capability of the AC-PEL, it can be used to emulate leading/lagging power factor linear loads and non-linear harmonic load profiles such as saturated magnetic systems, rectifiers, and electronic loads. Most existing industrial products only allow AC electronic loads to emulate linear or pre-defined nonlinear loads with variable crest factor, peak current, and similar parameters; however, harmonic amplitude and phase control is not possible [1]. In [2], an automated load bank is presented which is controlled by a microcontroller and a relay control board. The proposed system can only emulate limited load types and values. Hardware topologies for the programmable electronic AC loads are reviewed in [3], presenting traditional hardware topologies that can be utilized in programmable AC loads. The control system of the programmable load and the operation mode and performance are not discussed. Heat dissipation in programmable loads is a significant challenge because the energy received from the equipment under test (EUT) must either be dissipated or re-injected into the grid. An investigation into efficient heat dissipation mechanisms for programmable DC electronic load is discussed in [4], and the suitable low cost heat dissipation method for DC electronic load circuit for laboratory purpose is analyzed. A three-phase nonlinear load emulator for diode rectifier load model emulation using a power electronic converter is presented in [5]. The proposed system can only emulate diode rectifier load models and cannot handle other nonlinear load models with different harmonic current configurations. In emulators with a coupled DC-link, circulating zero-sequence current creates an additional load on the power switches. The currently available control methods require additional hardware as common-mode filters to effectively reduce this current. An electrical machine load emulator with reduced zero-sequence current is presented in [6]. The proposed modulation algorithm suppresses the zero-sequence current more effectively via direct compensation of common-mode voltage, and thus, no additional hardware filters are needed. In [7]-[8], a voltage-following strategy is utilized for shared DC bus programmable electronic loads to reduce zero-sequence current, phase current error, and switching losses. An energy recycling DC electronic load with inductor current step control for fast load transient is presented in [9]. In [10]-[12], a programmable electronic AC load is proposed to emulate various types of static loads, high frequency harmonic load and unbalanced load profiles for aerospace applications. The control system can emulate harmonic load profiles, but it does not address active power oscillations caused by current harmonics. A predictive current controller based programmable AC electronic load is proposed in [13] to emulate linear active and reactive loads. A regenerative active electronic load with voltage, current, and frequency control is proposed in [14] for power transformer testing applications. In this paper, an AC regenerative programmable electronic load (AC-RPEL) that enables emulating programmable power factor and harmonic load profiles is presented. The proposed AC-RPEL is able to emulate various types of loads such as constant-current (CC), constant-power (CP), and constant-impedance (CI). In CC operating mode, the AC-PEL sinks the programmed current waveform

independently from the EUT. This is the most commonly used mode for programmable electronic loads. Current-controlled grid-connected converters are examples of active CC load type. Saturated magnetic system and electronic loads can also be considered as CC loads. In CP mode, the AC-RPEL absorbs programmed active and reactive power out of the EUT. To test a voltage source EUT in CP mode, the AC-RPEL will regulate its current to absorb the programmed active and reactive power values. Inverter-Based Sources (IBSs), electronically controlled grid-connected regulated output electronic loads are examples of CP loads [15]-[16]. A constant power load modelling is presented for programmable impedance control strategy in [17]. In CI mode, the AC-RPEL sinks current proportional to the EUT voltage divided by the programmed impedance. Many practical passive loads can be considered as a CI load. To address complexity, the $\alpha\beta$ stationary reference frame is an effective method for controlling the fundamental EUT current and harmonics with frequencies up to one-sixth of the switching frequency [10]. Several studies have shown that the Proportional-Resonant (PR) controller is an effective choice for controlling AC currents [18]. PR controllers can achieve similar performance as proportional-integral (PI) controllers in the stationary reference frame. Additionally, parallel PR controllers tuned for harmonic frequencies make the control of harmonic components possible. In this paper, PR current controller is used to control the EUT-side current of the proposed AC-RPEL. The general structure of the proposed AC-RPEL is shown in Fig. 1. The DC link of the AC-PEL converter is supplied using a grid-connected inverter which is responsible for regulating the DC-link voltage by injecting active power received from the EUT into the grid. It is assumed that the EUT is galvanically isolated from the grid, which is required to prevent circulating current. The inner current control loop of the DC-link voltage regulation system is PLL-Less based on the PR controller which is proposed in [19]. In the CC mode of the proposed AC-RPEL, the active power of the EUT has *6k*-order harmonic components due to the programmed current harmonics and affects the performance of the DC-link voltage regulation system and increases the grid-side current THD if not compensated. To address this, a novel control system is proposed for the DC-link voltage regulation system. The proposed voltage controller for the DC-link voltage regulation system consists of a PI controller in series with a multi frequency notch filter (MFNF) to compensate *6k*-order harmonic components of the DC link voltage. PI+Notch voltage controllers are commonly employed in PFC rectifiers to compensate the 2nd harmonic of the DC link voltage [20]-[21]. In this paper, the notch filter is modified to compensate *6k*-order harmonic contents. The remainder of this paper is organized as follows: Section 2 discusses the AC-RPEL structure and control system; Section 3 presents simulation and experimental results, and Section 4 provides a brief conclusion. 2. AC-RPEL Architecture and control An AC-RPEL consists of two main parts: an AC-PEL, which functions as a programmable current source, and a grid-side converter for DC-link voltage regulation.

2. AC-RPEL Architecture and control

An AC-RPEL consists of two main parts: an AC-PEL, which functions as a programmable current source, and a grid-side converter for DC-link voltage regulation.

2.1. AC-PEL Architecture

The AC-PEL and its proposed control system are shown in Fig. 2. Assuming that the grid side converter regulates the DC-link voltage, the DC-link of the AC-PEL is modeled as a DC voltage source. The current controller of the AC-PEL is a PR controller, which is one of the most popular solutions for regulating AC current. With its harmonic compensation (HC) capability, this controller is well-suited for controlling harmonic load profiles. To avoid stability problems associated with infinite gain at the resonant frequency, a non-ideal PR controller, as described in Eq. (1), can be used where, K_p is the proportional gain term, K_r is the resonant gain term, and ω_0 is the resonant frequency, and ω_c is the cut-off frequency [18].

$$G_{PR}(s) = K_p + K_r \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{1}$$

In addition to single-frequency resonant control, multi-resonant compensation can be achieved by cascading harmonic-frequency resonant controllers [18]. This feature is used to control the harmonic load profiles using the AC-RPEL. A non-ideal PR controller with harmonic controllers is expressed in Eq. (2).

$$G_{PR}(s) = K_p + K_r \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} + \sum_{(h=5,7,11,13,\ldots)} K_{rh} \frac{2\omega_{ch} s}{s^2 + 2\omega_{ch} s + (h\omega_0)^2} \tag{2}$$

$K_{rh,}$ ω_{ch} represent the individual resonant gain and cut-off frequency for h_{th} harmonic order.

The current control system, illustrated in Fig. 2, operates in the αβ stationary reference frame and incorporates proportional, fundamental, and harmonic resonant terms. The reference current in the αβ frame is calculated based on the user's command. In CC mode, reference current for phases a, b, and c, and in $\alpha\beta$ frame, is defined by Eq. (3) and Eq. (4), respectively. $I_{h(i)}$ and $\theta_{h(i)}$ are the amplitude and phase angle of the reference current for i^{th} harmonic and ω is the angular frequency of the EUT voltage.

$$\begin{cases} i_{aCC} = I_{h(1)}\sin(\omega t+\theta_{h(1)}) + \sum_{k=1,2,\ldots}(I_{h(6k\pm1)}\sin\left((6k\pm1)\omega t+\theta_{h(6k\pm1)}\right)) \\ i_{bCC} = I_{h(1)}\sin((\omega t-\frac{2\pi}{3})+\theta_{h(1)}) + \sum_{k=1,2,\ldots}(I_{h(6k\pm1)}\sin\left((6k\pm1)(\omega t-\frac{2\pi}{3})+\theta_{h(6k\pm1)}\right)) \\ i_{cCC} = I_{h(1)}\sin((\omega t+\frac{2\pi}{3})+\theta_{h(1)}) + \sum_{k=1,2,\ldots}(I_{h(6k\pm1)}\sin\left((6k\pm1)(\omega t+\frac{2\pi}{3})+\theta_{h(6k\pm1)}\right)) \end{cases} \quad (3)$$

$$\begin{cases} i_{\alpha CC} = I_{h(1)}\sin(\omega t+\theta_{h(1)}) + \sum_{k=1,2,\ldots}(I_{h(6k\pm1)}\sin\left((6k\pm1)\omega t+\theta_{h(6k\pm1)}\right)) \\ i_{\beta CC} = -(I_{h(1)}\cos(\omega t+\theta_{h(1)}) \pm \sum_{k=1,2,\ldots}(I_{h(6k\pm1)}\cos\left((6k\pm1)(\omega t)+\theta_{h(6k\pm1)}\right))) \end{cases} \quad (4)$$

Assuming sinusoidal voltage and currents, the active and reactive power in the $\alpha\beta$ frame are as Eq. (5), and the reference currents for CP mode in the $\alpha\beta$ frame can be explained as Eq. (6), where P and Q are the reference for active and reactive power and $v_{\alpha EUT}$ and $v_{\beta EUT}$ are the EUT voltages in the $\alpha\beta$ frame.

$$\begin{cases} P = \frac{3}{2}(v_{\alpha EUT}i_{\alpha CP} + v_{\beta EUT}i_{\beta CP}) \\ Q = \frac{3}{2}(v_{\beta EUT}i_{\alpha CP} - v_{\alpha EUT}i_{\beta CP}) \end{cases} \quad (5)$$

$$\begin{cases} i_{\alpha CP} = \frac{2}{3}\frac{(Pv_{\alpha EUT} + Qv_{\beta EUT})}{(v_{\alpha EUT}^2 + v_{\beta EUT}^2)} \\ i_{\beta CP} = \frac{2}{3}\frac{(Pv_{\beta EUT} - Qv_{\alpha EUT})}{(v_{\alpha EUT}^2 + v_{\beta EUT}^2)} \end{cases} \quad (6)$$

In CI mode, the reference current for phases a, b and c, and in the $\alpha\beta$ frame, are as Eq. (7) and Eq. (8), respectively. Z is the magnitude and θ_Z is the phase angle of the reference impedance and $V_{M\,EUT}$ is the amplitude of the EUT voltage. As is expressed in Eq. (7) and Eq. (8), the reference current in CP and CI modes is calculated without using the phase angle of the EUT voltage and therefore the system is PLL-Less.

$$\begin{cases} i_{aCI} = \frac{V_{M_{EUT}}}{Z}\sin(\omega t-\theta_Z) \\ i_{bCI} = \frac{V_{M_{EUT}}}{Z}\sin(\omega t-\frac{2\pi}{3}-\theta_Z) \\ i_{cCI} = \frac{V_{M_{EUT}}}{Z}\sin(\omega t+\frac{2\pi}{3}-\theta_Z) \end{cases} \quad (7)$$

$$\begin{cases} i_{\alpha CI} = \frac{v_{\alpha EUT}\cos(\theta_Z) + v_{\beta EUT}\sin(\theta_Z)}{Z} \\ i_{\beta CI} = \frac{v_{\beta EUT}\cos(\theta_Z) - v_{\alpha EUT}\sin(\theta_Z)}{Z} \end{cases} \quad (8)$$

2.2. DC-Link Voltage Regulation System Architecture

The DC-link voltage of the AC-RPEL can be implemented using either passive or active methods. In the passive method, the DC voltage source is a large capacitor in parallel with a dissipative resistive load [10]. In the active method, the DC-link of a galvanically isolated grid-connected converter can serve as the voltage source, preventing circulating currents in the system. In

this method, the power received from the EUT is recycled and injected into the grid with the desired power factor, typically unity. The DC-link voltage control system is shown in Fig. 3. As illustrated in Fig. 3(b), the DC-link voltage controller determines the active power reference, while the reactive power reference is user-configurable for the desired power factor. The grid-side reference current in the $\alpha\beta$ frame is calculated using Eq. (9), and the PR current controller regulates the grid-side current. This is also a PLL-Less scheme, as discussed in [19].

$$\begin{cases} i_{\alpha Ref} = \dfrac{2}{3}\dfrac{(P_{Ref}v_{\alpha G} + Q_{Ref}v_{\beta G})}{(v_{\alpha G}^2 + v_{\beta G}^2)} \\ i_{\beta Ref} = \dfrac{2}{3}\dfrac{(P_{Ref}v_{\beta G} - Q_{Ref}v_{\alpha G})}{(v_{\alpha G}^2 + v_{\beta G}^2)} \end{cases} \tag{9}$$

As expressed in Eq. (10), in CC mode, active power has *6k*-order harmonics in addition to the DC component. The traditional PI controller will reduce these harmonics for low bandwidth DC-link voltage controllers. However, the transient response will be slower, which may not be acceptable in some applications, so high bandwidth is preferred, and these harmonics may adversely affect control performance.

$$P_{CC} = \frac{3}{2}V_{M_{EUT}}(I_{h(1)}\cos(\theta_{h(1)}) + \sum\nolimits_{k=1,2,\ldots}(\pm I_{h(6k\pm1)}\cos((6k)\omega t \pm(-\theta_{h(6k\pm1)})))) \tag{10}$$

In order to mitigate harmonic frequencies in a high bandwidth DC-link voltage control loop, an MFNF is used in series with traditional PI controller [20]-[21]. The transfer function of the notch filter is expressed in Eq. (11), where ω_N is the notch frequency and ζ is the damping coefficient.

$$G_{NF} = \frac{s^2 + \omega_N^2}{s^2 + 2\zeta\omega_N s + \omega_N^2} \tag{11}$$

The transfer function of the proposed controller is presented in Eq. (12). As illustrated in Fig. 4, the DC-link voltage controller attenuates the *6k*-order harmonics and improves the performance of the control system in the presence of harmonics.

$$G_{MFNF+PI} = (K_{pv} + \frac{K_{iv}}{s})(\frac{s^2 + (6\omega_0)^2}{s^2 + 2\zeta(6\omega_0)s + (6\omega_0)^2})(\frac{s^2 + (12\omega_0)^2}{s^2 + 2\zeta(12\omega_0)s + (12\omega_0)^2})(\ldots) \tag{12}$$

3. Simulation and Experimental Results

3.1. Simulation Results

In order to verify the performance of the proposed system, the system with the specifications expressed in Table 1 is simulated in MATLAB/Simulink environment. The DC-link voltage of the AC-RPEL is set to 900V to prevent the over-modulation of the converter. The system has been simulated in CC, CP, and CI modes. The DC-link voltage regulator is enabled at t=1s, and the AC-PEL is enabled at t=1.5s, respectively. In CC mode, the amplitude and phase angle of the reference current, up to 13th harmonic, are as expressed in Table 2. From t=2s to t=3s, the reference current consists of the harmonic components of a diode rectifier up to the 13th harmonic, emulating a diode rectifier current waveform. The amplitude and phase error of the EUT current is presented in Table 2. As detailed in Table 2, the proposed control system follows the reference value with high precision. The small error in tracking the reference current is the result of using the non-ideal resonant controller. The DC-link voltage, the grid-side current waveform and, the FFT of the DC-link voltage when using PI controller with higher (K_p=*1.1* and K_i=*68.9*) and lower (K_p=*0.55* and K_i=*8.6*) bandwidth and PI+MFNF controller with high bandwidth (K_p=*1.1* and K_i=*68.9*) are shown in Fig. 5 and Fig. 6, respectively. As is indicated, the THD of the grid-side current is 6.06%, 5.18%, and 4.87% for high bandwidth PI, low bandwidth PI, and high bandwidth PI+MFNF controller. Reducing the bandwidth of the controller reduces the THD of the grid-side current, but in applications where high bandwidth is required, this solution is not applicable, and the proposed PI+MFNF controller should be used, which has the best performance. The EUT-side voltage and current are shown in Fig. 7. The EUT voltage amplitude is reduced to 250V at a constant slope from t=2.5s to t=2.75s, and as shown in Fig. 7, the EUT current remains unchanged since the AC-RPEL operates in the CC mode.

In CI mode, the reference impedance is 60Ω from t=1.5s to t=2s, and 24-36j Ω from t=2s to t=3s, respectively. The PI+MFNF controller is used as the DC-link voltage controller. The DC-link voltage, grid-side voltage and grid-side current are shown in Fig. 8, and the EUT-side voltage and current are shown in Fig. 9. To validate the operation of the proposed systems in CI mode,

the EUT voltage amplitude is reduced to 250V at a constant slope from t=2.5s to t=2.75s, and as shown in Fig. 9, the EUT current also reduced to remain the voltage to current division constant and equal to programmed impedance. As illustrated in Fig. 8, the injected power to the grid is reduced in square relation with time as the EUT voltage is reduced from t=2.5s to t=2.75s, since the active power of the EUT is changed as Eq. (13), where S_{EUT} is the apparent power of the EUT.

$$S_{EUT} = \frac{v_{EUT}^2}{Z} \tag{13}$$

In CP mode, the reference values for active and reactive power are 3000 W, 0 VAr from t=1.5s to t=2s, and 2400 W, 1800 VAr from t=2s to t=3s, respectively. The PI+MFNF controller is used as the DC-link voltage controller. The DC-link voltage, grid-side voltage and grid-side current are shown in Fig. 10, and the EUT-side voltage and current of the EUT are shown in Fig. 11. To validate the performance of the proposed systems in CP operation mode, the EUT voltage amplitude is reduced to 250V at a constant slope from t=2.5s to t=2.75s, and as shown in Fig. 11, the EUT current increased to remain the active and reactive power constant and equal to the programmed values. As shown in Fig. 10, the injected current and power to the grid is unchanged from t=2.5s to t=2.75s, since the AC-RPEL is in CP mode and the active power of the EUT is constant.

3.2. Experimental Results

To validate the performance of the proposed system with experimental setup, a laboratory prototype is developed. The experimental setup is shown in Fig. 12, and its system specifications are listed in Table 3. The utilized components are not optimal for the system and are selected from existing laboratory components. In the experimental system, the grid voltage is considered as the EUT and a resistive load is inserted at the DC-link of the converter. The performance of the experimental system is validated in the CC and CP modes. The grid voltage and current waveforms in CC mode for different current references are shown in Fig. 13 to Fig. 17. The magnitude of the 1st harmonic is selected 3A for all scenarios to have the DC-link voltage of 120V.

The performance of the experimental system is also validated for CP operating mode and the grid voltage and current for different reference values are shown in Fig. 18, Fig. 19, and Fig.20. The active power reference is selected 180W for all scenarios to make the DC-link voltage 120V.

4. Conclusion

In this paper, an AC-RPEL is proposed which is able to emulate various types of load profiles such as CC, CI, and CP loads. In the CC mode, in addition to linear loads the proposed system has the ability to emulate the current harmonics of nonlinear loads. The current controller of the proposed AC-RPEL is a PR+HC controller and is capable to control harmonic components of the reference current. To recycle the absorbed power of the AC-RPEL, a PLL-Less grid-connected inverter is employed. To address EUT-side active power oscillations caused by EUT current harmonics, the performance of a traditional PI DC-link voltage controller with varying bandwidths is compared against a modified PI+MFNF controller. The analysis demonstrates that the PI+MFNF controller provides superior performance, particularly in high-bandwidth applications. Simulation results verify the performance of the proposed system and a laboratory prototype is used to verify the performance of the AC-RPEL controller through experimental results. The simulation and experimental results validate the effectiveness of the proposed system.

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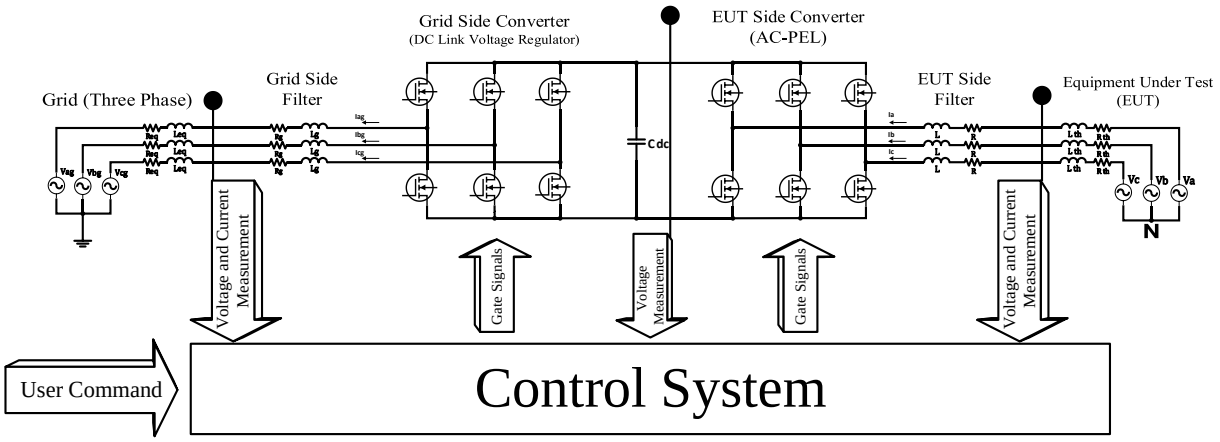
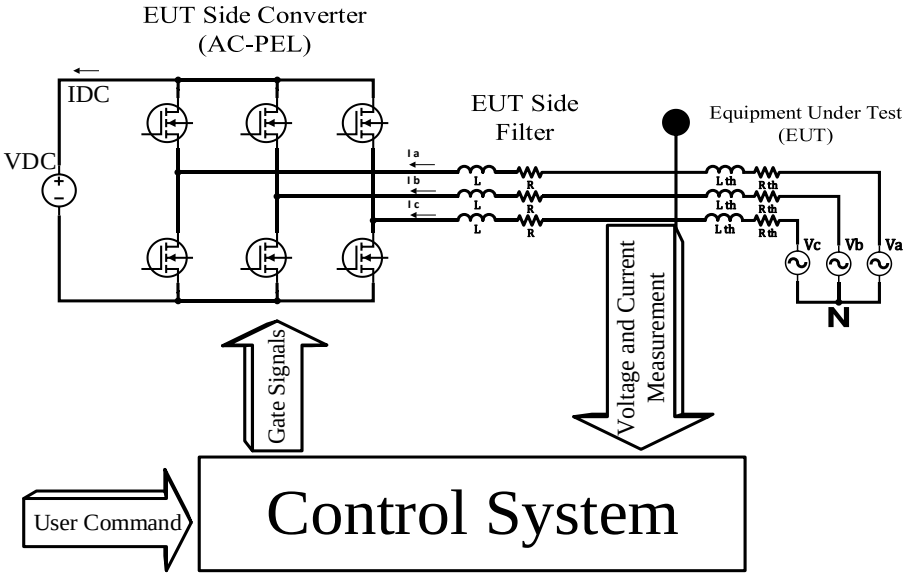


Fig. 1. General structure of AC-RPEL



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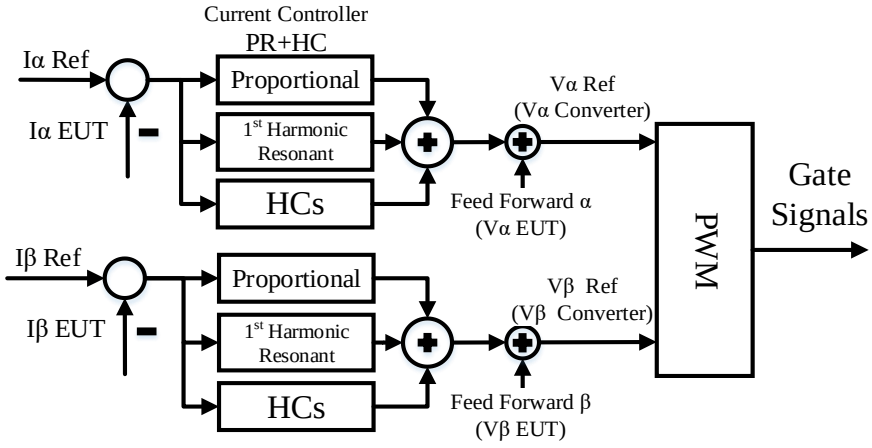
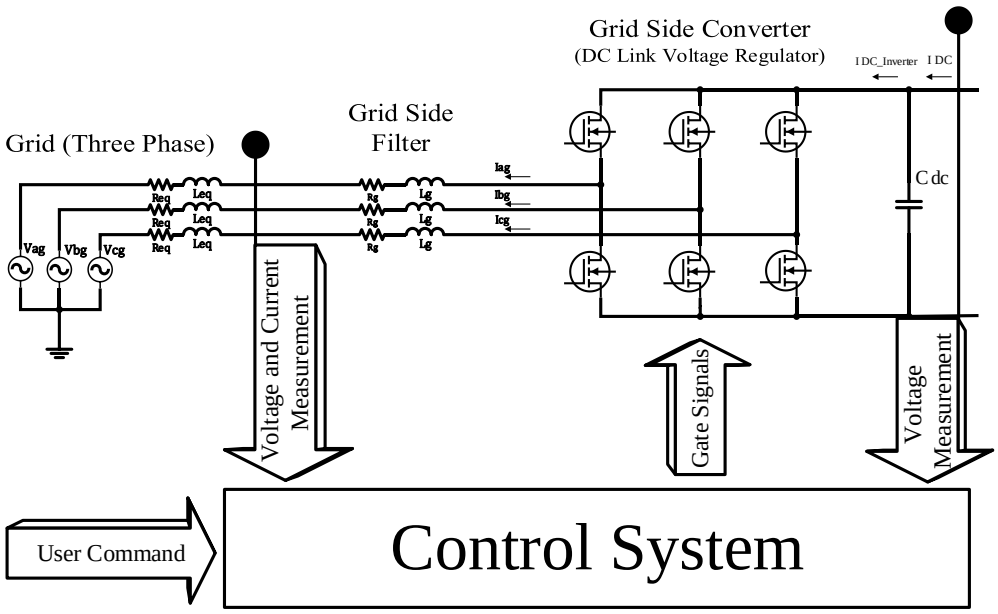


(b)

Fig. 2. EUT side converter (AC-PEL) a- circuit diagram and b- control scheme



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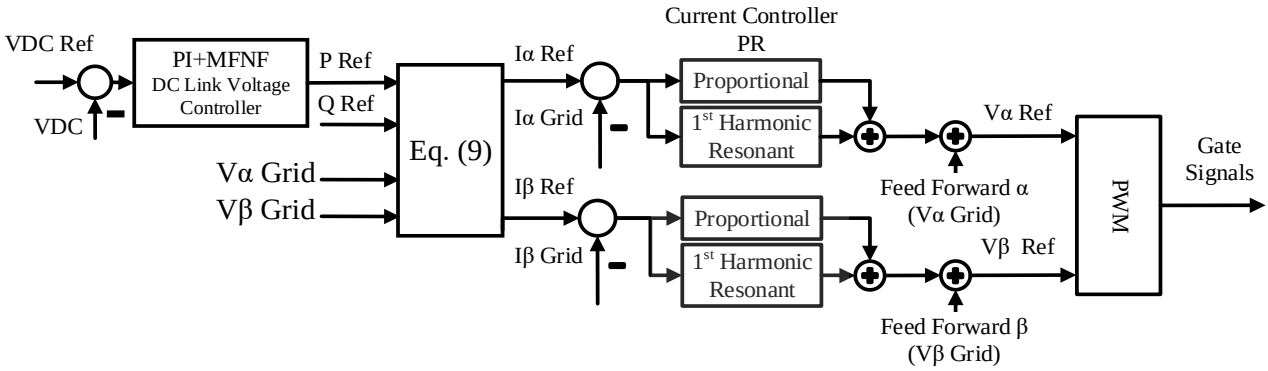


(b)

Fig 3. Grid side converter (DC link voltage regulator) a- circuit diagram and b- control scheme

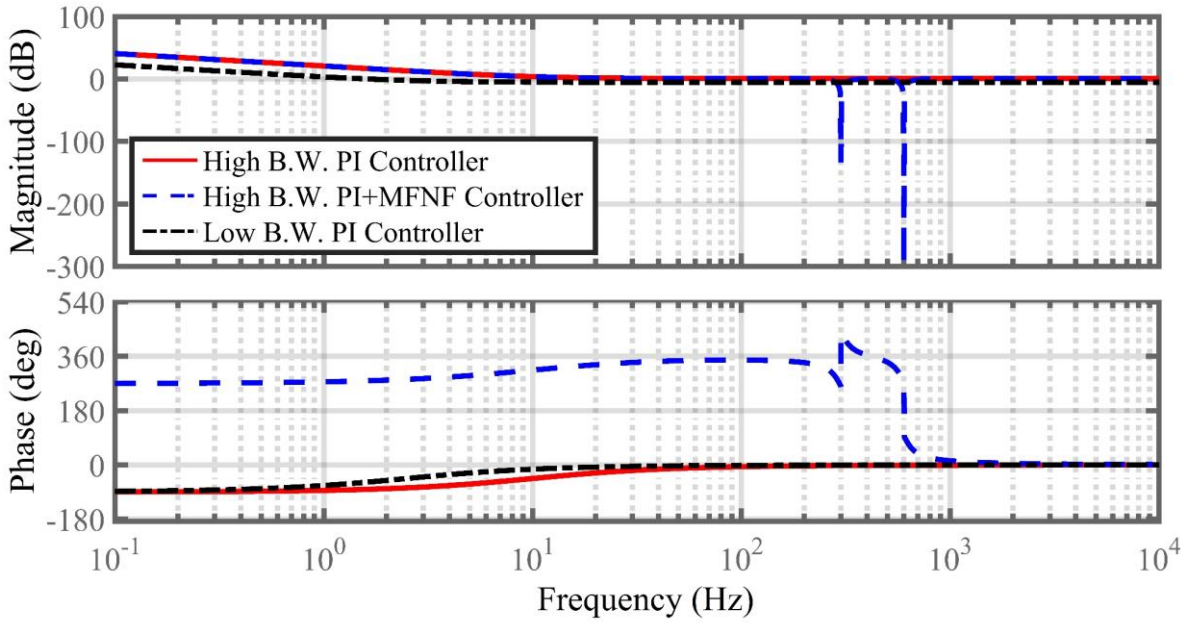


Fig.4. Bode diagram of a high bandwidth and low bandwidth PI and high bandwidth PI+MFNF (6th, 12th harmonics) controller

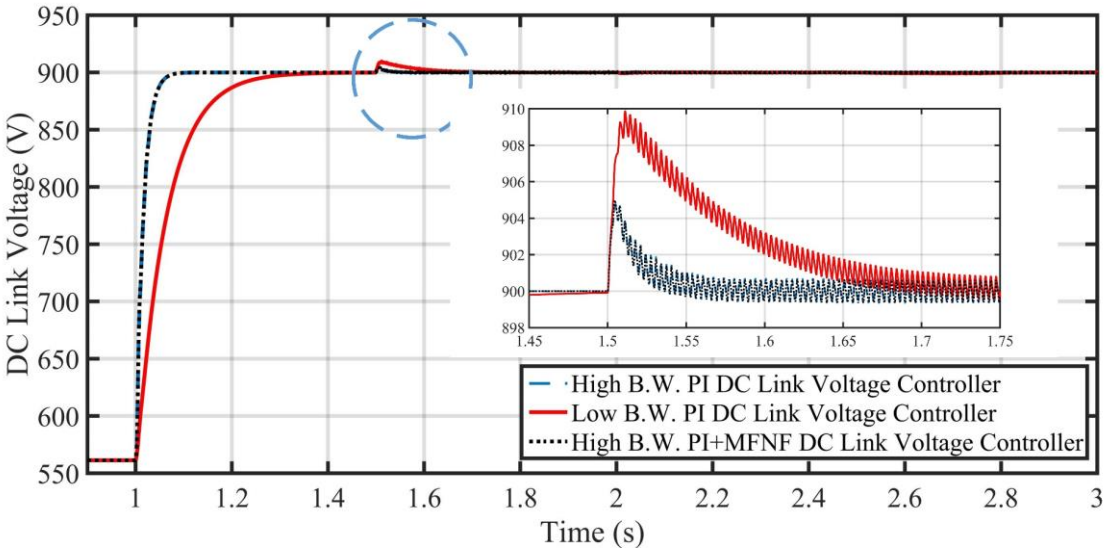
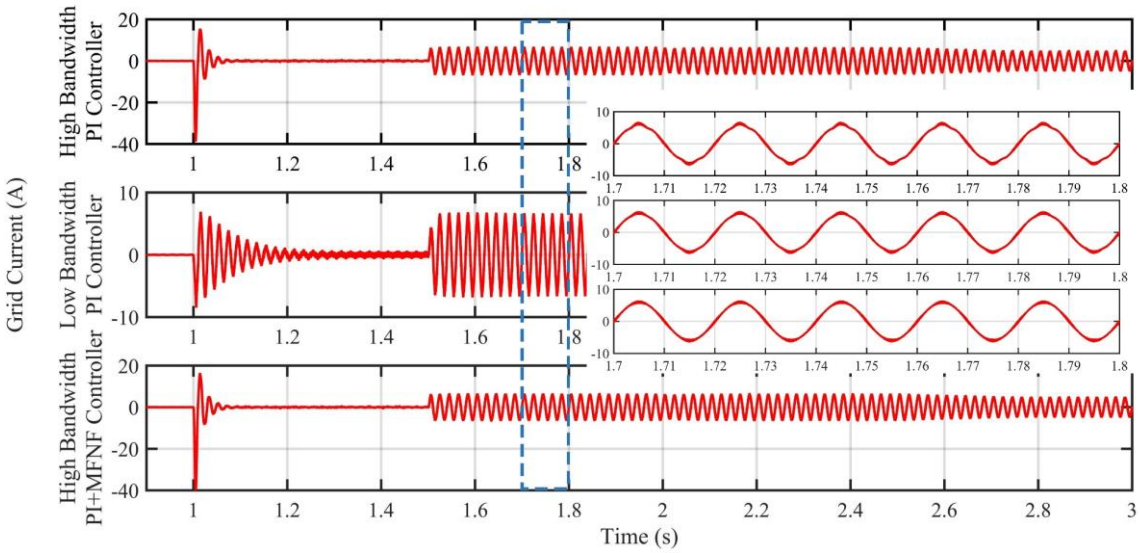
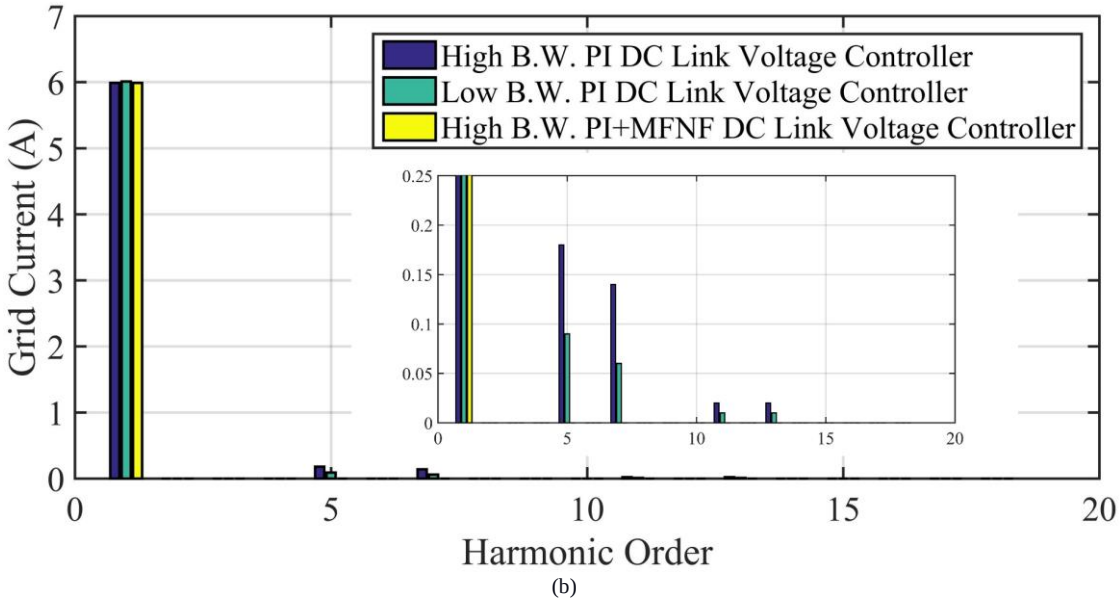


Fig. 5. DC link voltage comparison for different voltage control scenarios



(a)



(b)

Fig. 6. a- Grid current and its b- FFT for different voltage control scenarios

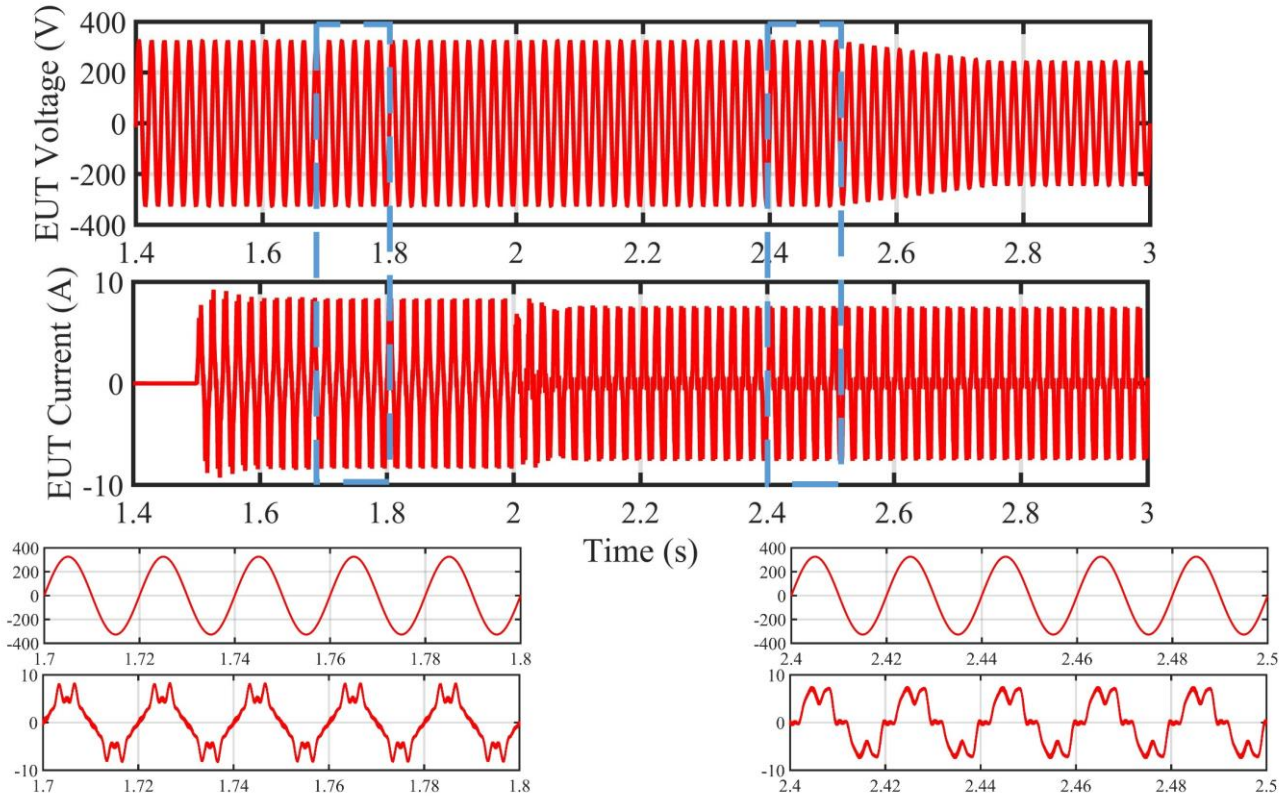


Fig. 7. EUT voltage and current waveform in CC mode

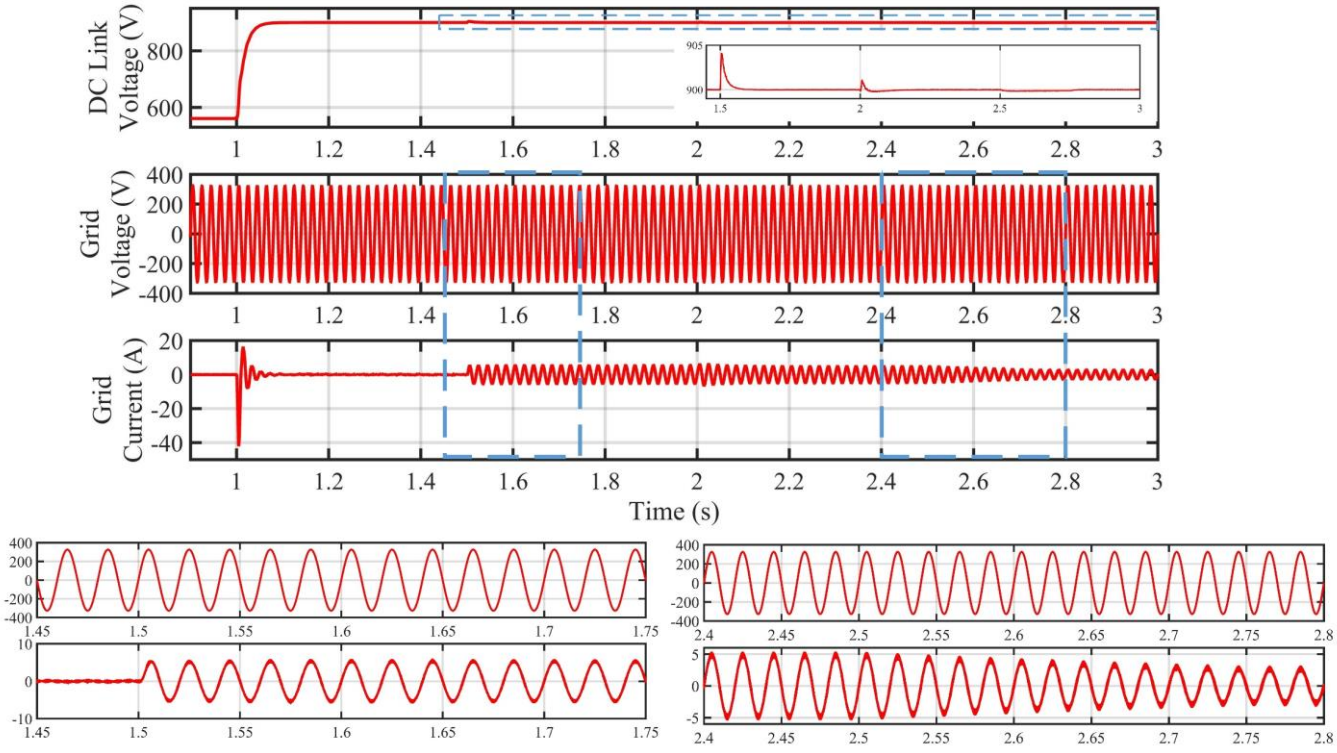


Fig. 8. DC link and grid voltages and current in CI mode

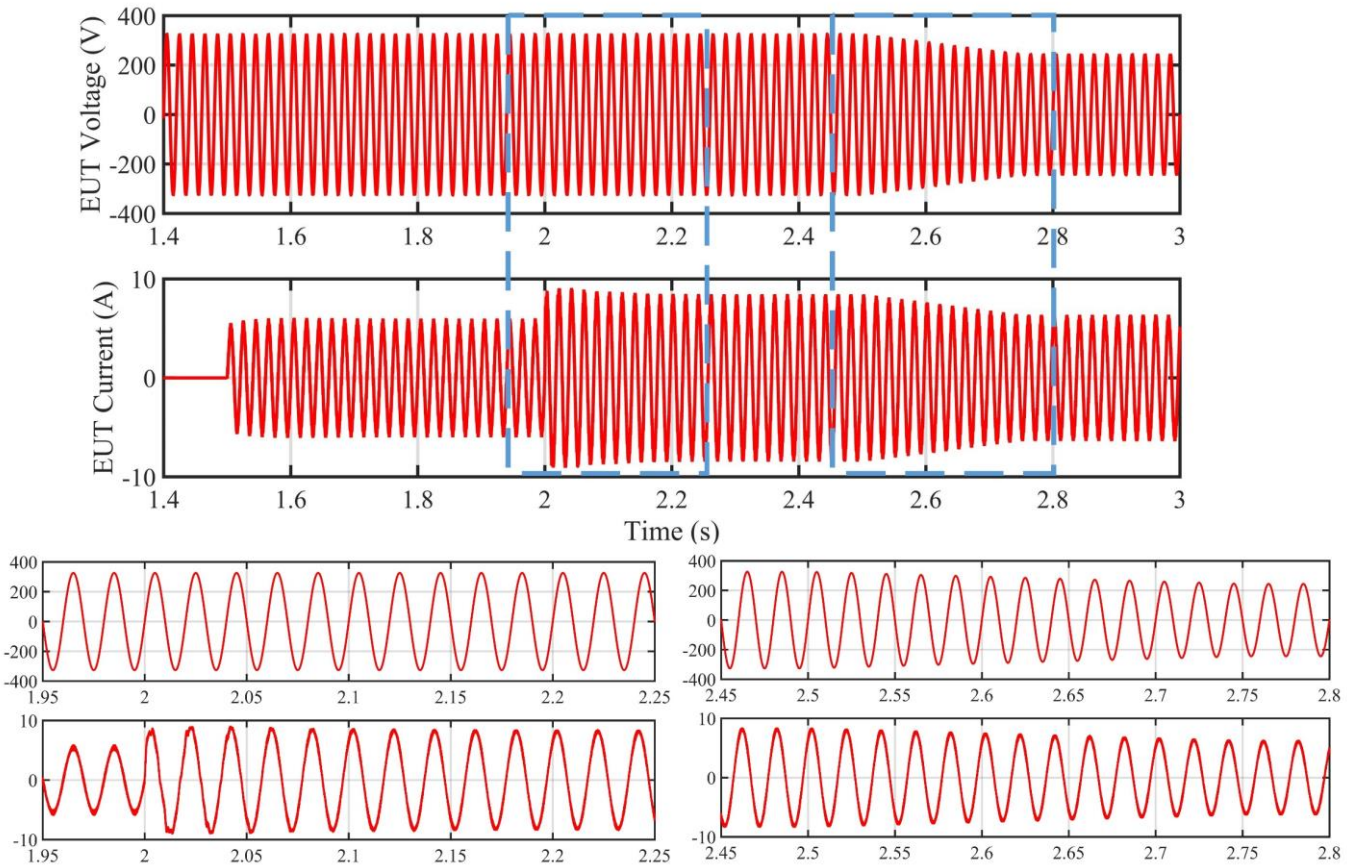


Fig. 9. EUT voltage and current in CI mode

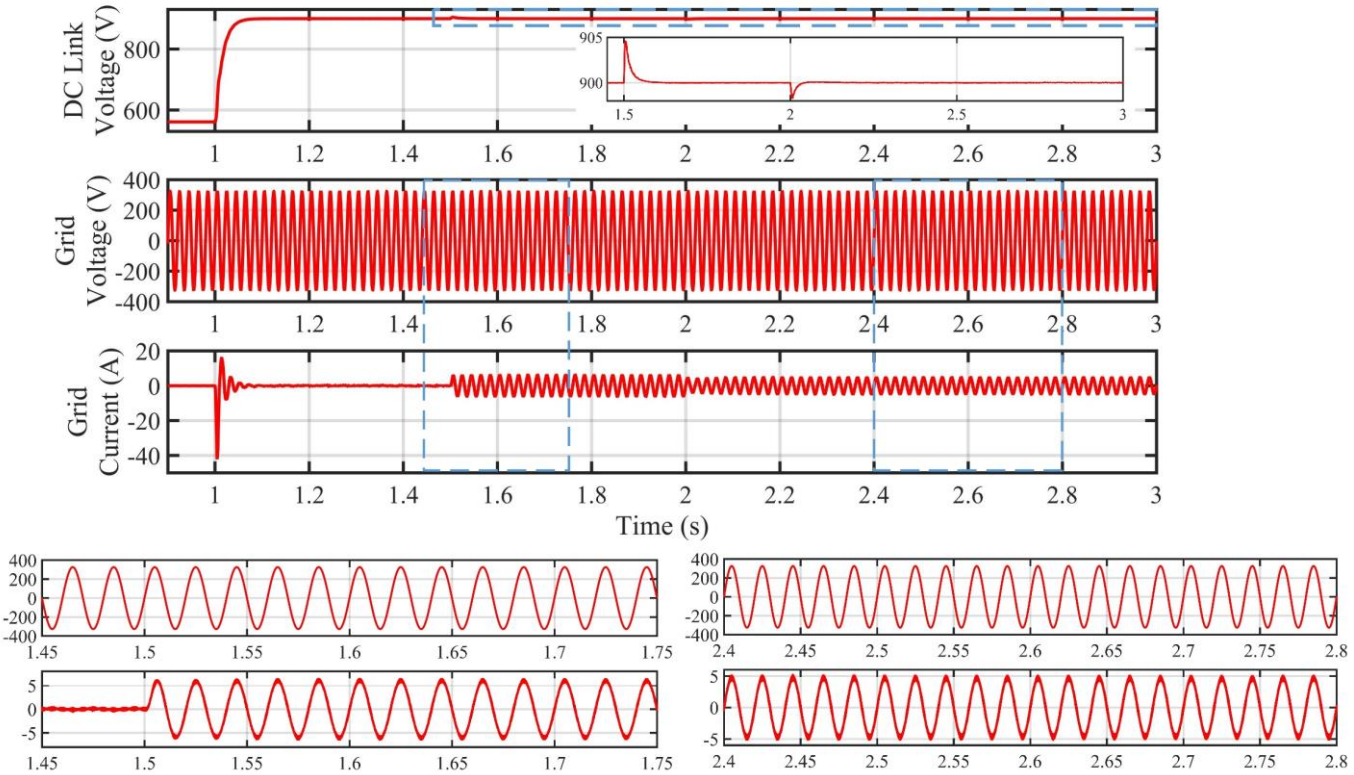


Fig. 10. DC link and grid voltages and current in CP mode

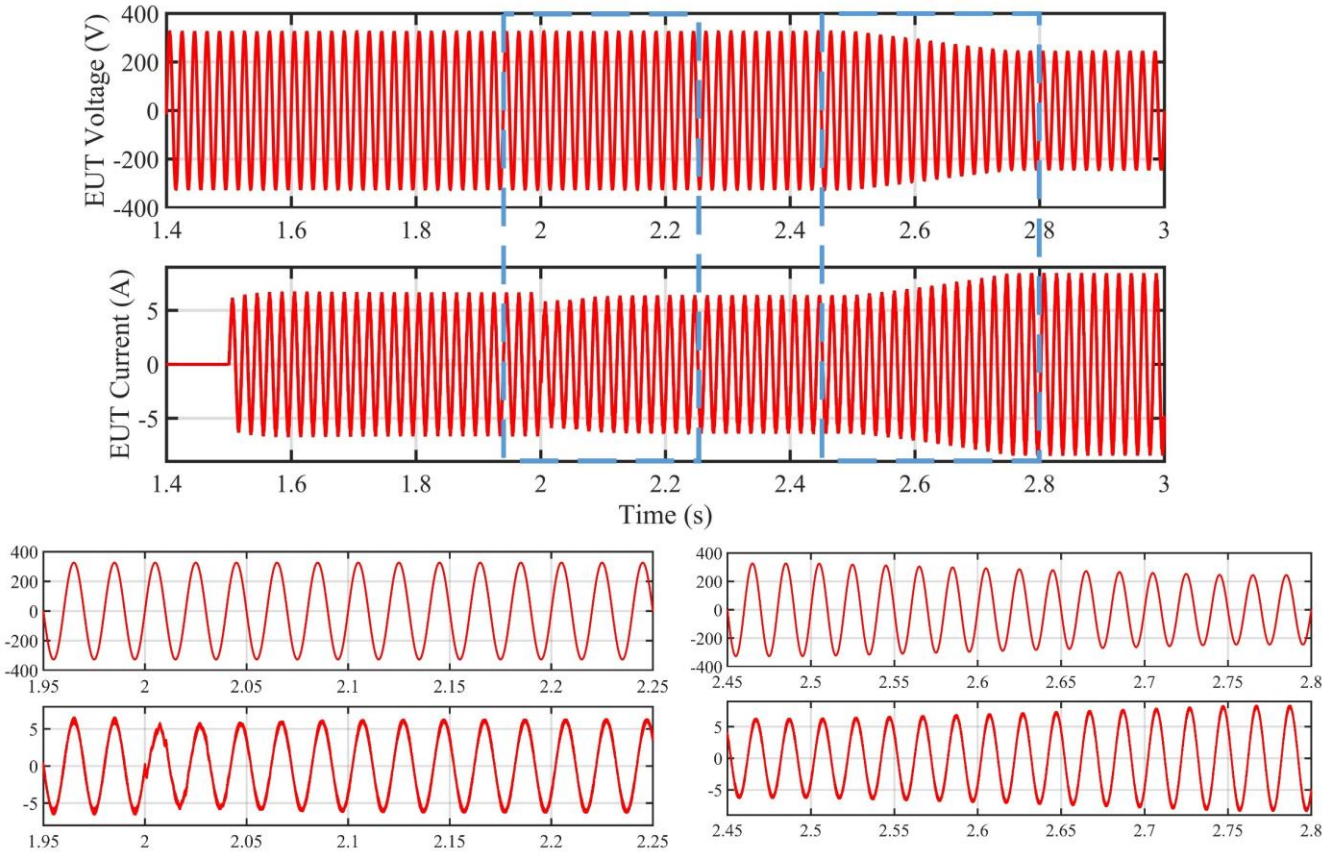
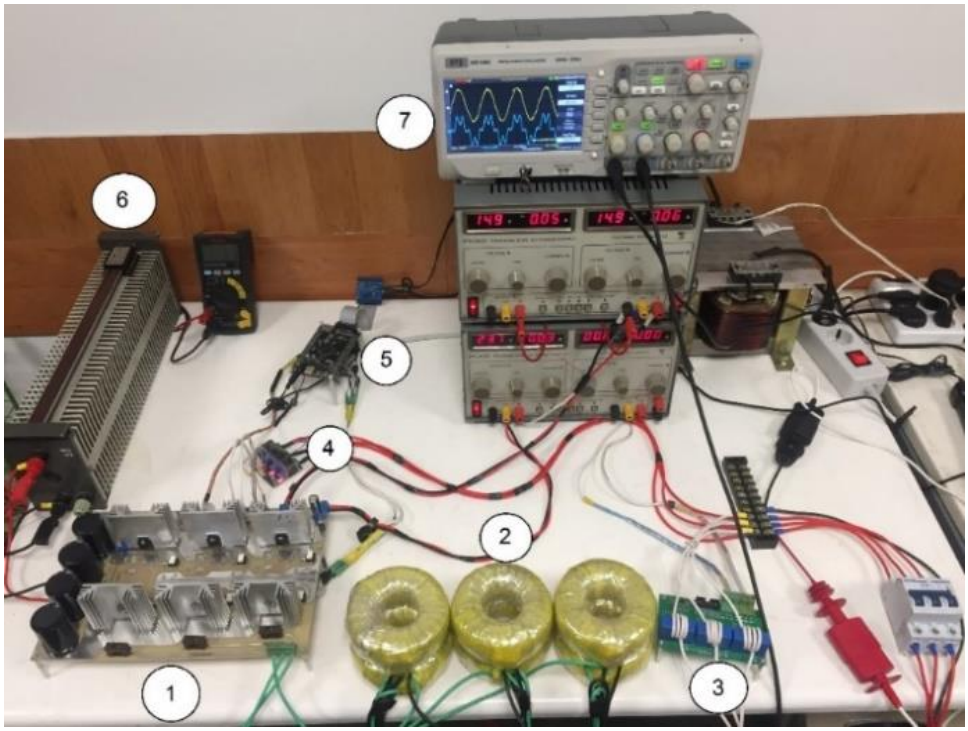
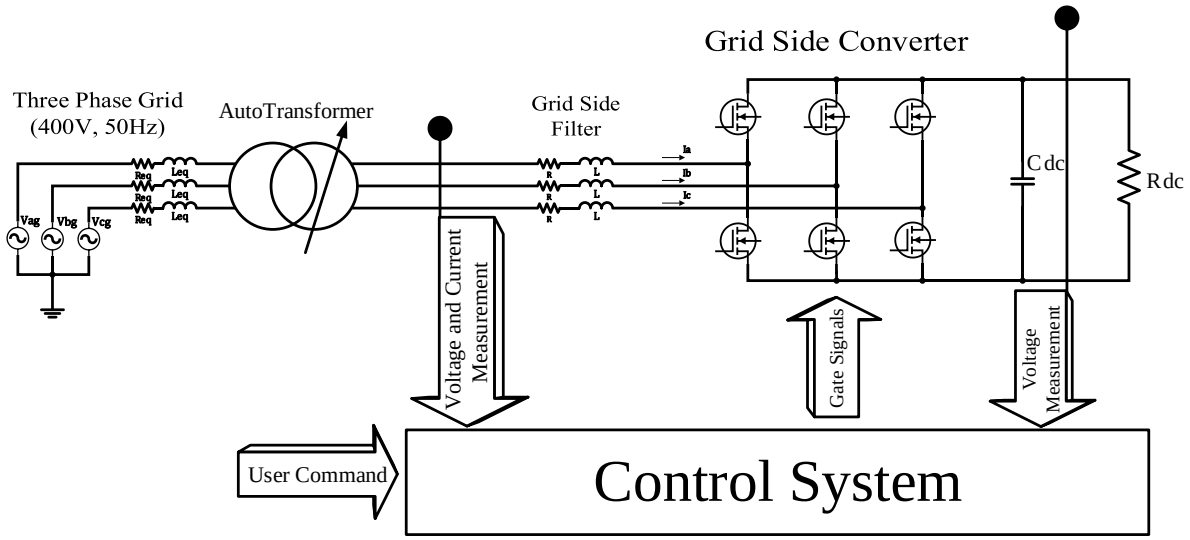


Fig. 11. EUT voltage and current in CP mode



(a)

(1) Converter board (2) Grid-side filter inductors (3) Grid-side current sensors (4) Grid-side voltage sensors (5) STM32F407ZGT6 development board (6) DC-Link load (7) Digital oscilloscope



(b)

Fig. 12. a- Experimental Setup, b- circuit diagram

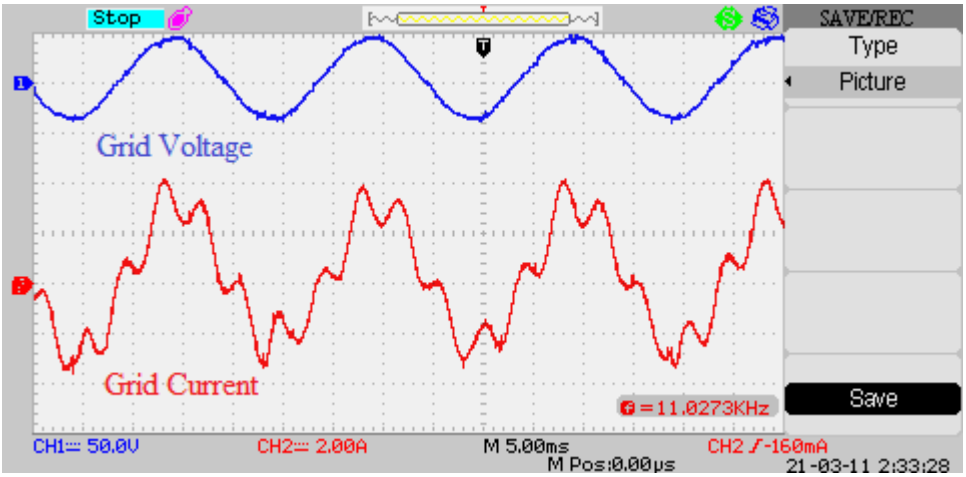


Fig. 13. Voltage and current waveform for 1st harmonic with 3A amplitude and 0° phase and 5th harmonic with 0.8A magnitude and 90° phase

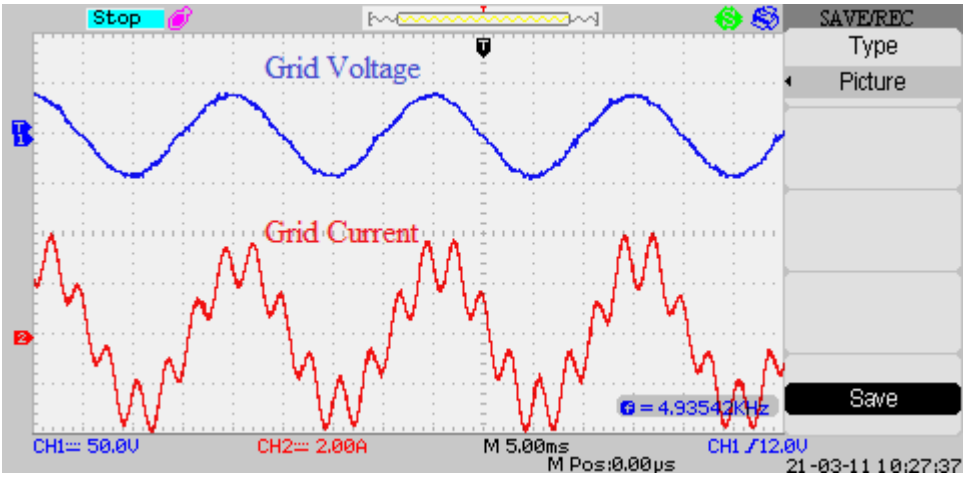


Fig. 14. Voltage and current waveform for 1st harmonic with 3A amplitude and 0° phase and 7th harmonic with 0.8A magnitude and 0° phase

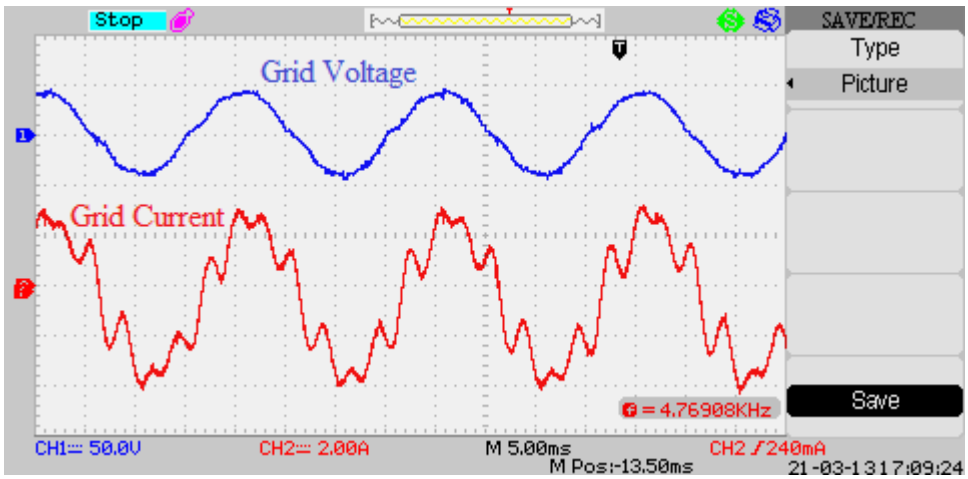


Fig. 15. Voltage and current waveform for 1st harmonic with 3A amplitude and 0° phase and 5th harmonic with 0.8A magnitude and 0° phase and 7th harmonic with 0.6A magnitude and 0° phase

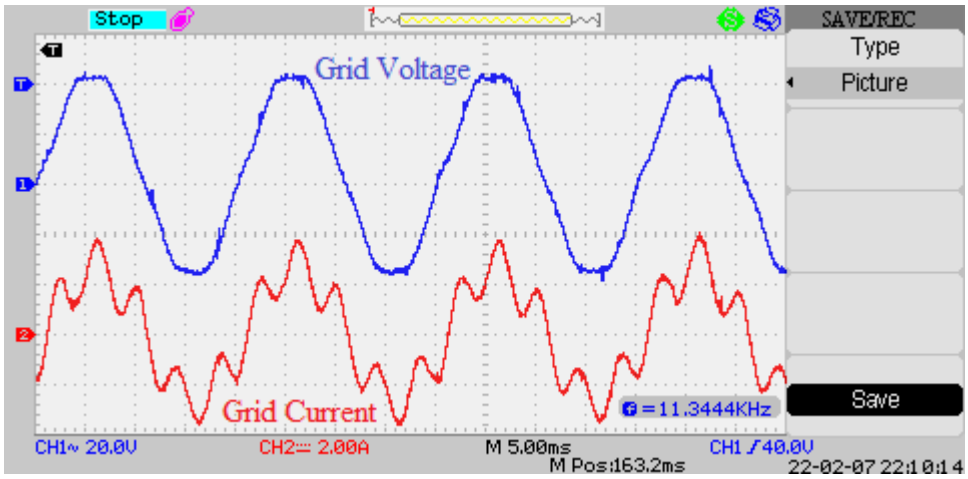


Fig. 16. Voltage and current waveform for 1st harmonic with 3A amplitude and 0° phase and 5th harmonic with 0.8A magnitude and 0° phase

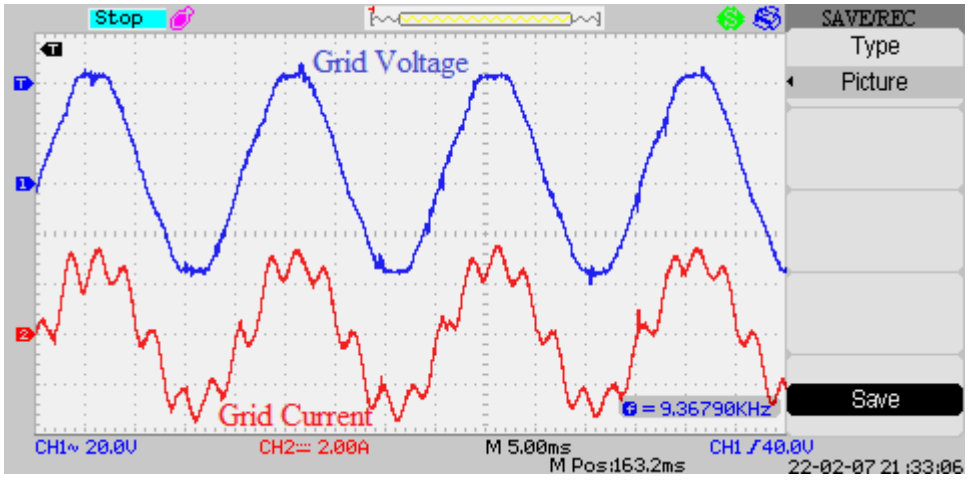


Fig. 17. Voltage and current waveform for 1st harmonic with 3A amplitude and 0° phase and 7th harmonic with 0.6A magnitude and 90° phase

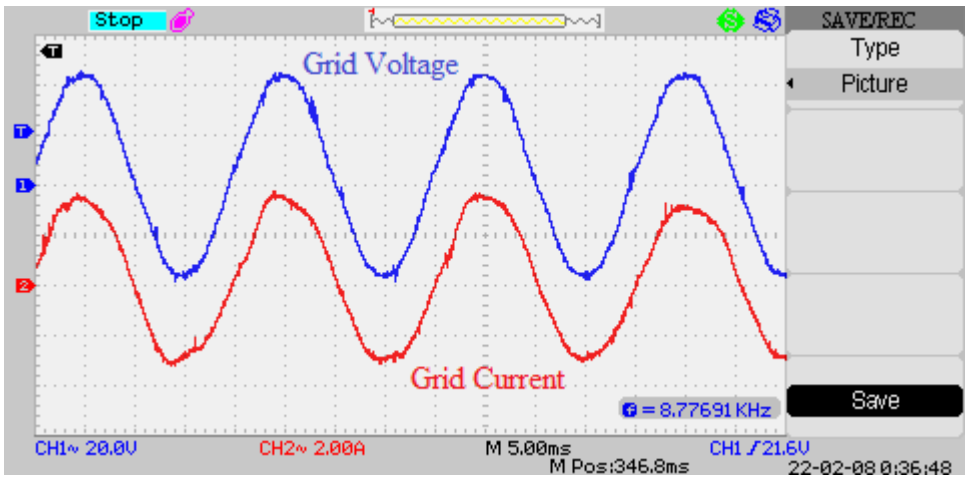


Fig. 18. Voltage and current waveform for 180W and 0VAr active and reactive power references

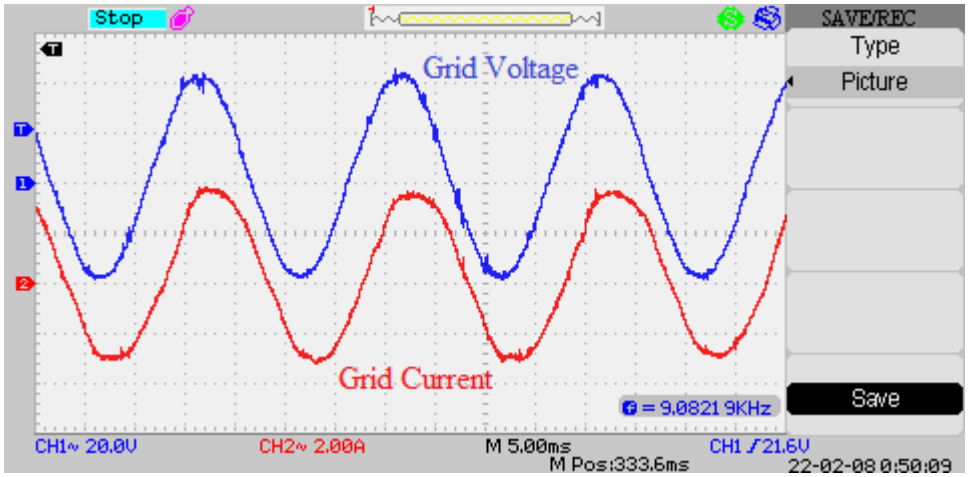


Fig. 19. Voltage and current waveform for 180W and 90VAr active and reactive power references

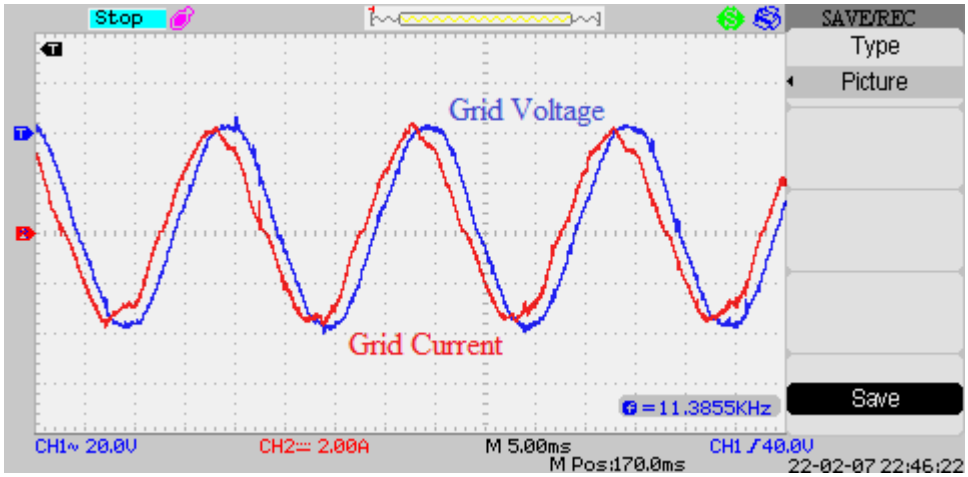


Fig. 20. Voltage and current waveform for 180W and -90VAr active and reactive power references

Table 1 System specifications for AC-PEL and DC Link voltage regulator

AC-PEL			DC Link Voltage Regulator		
S_{Rated}	Rated Power	3 KVA	S_{Rated}	Rated Power	3 KVA
$V_{L\text{-}L}{}^{EUT}$	Rms EUT line voltage	400 V	$V_{L\text{-}L}{}^{Grid}$	Rms Grid line voltage	400 V
L	Filter Inductance	9.2 mH	L_g	Filter Inductance	9.2 mH
R	Filter Resistance	0.1 Ω	R_g	Filter Resistance	0.1 Ω
V_{DC}	DC link voltage	900 V	C_{DC}	DC link capacitor	1200 µF
F_{SW}	Switching Frequency	10 kHz	F_{SW}	Switching Frequency	10 kHz

Table 2 Reference and EUT current for simulation in the CC mode

Harmonic Order	From t=1.5s to t=2s							From t=2s to t=3s						
	Reference		EUT Current		Amplitude Error (A)	Phase Error (Deg.)	Phase Error (µs)	Reference		EUT Current		Amplitude Error (A)	Phase Error (Deg.)	Phase Error (µs)
	Amplitude (A)	Phase (Deg.)	Amplitude (A)	Phase (Deg.)				Amplitude (A)	Phase (Deg.)	Amplitude (A)	Phase (Deg.)			
1	6.12	0	6.113	-0.8	0.007	-0.8	44.4	6.41	-15.8	6.403	-16.6	0.007	-0.8	44.4
5	1.22	180	1.22	179.5	0	-0.5	5.55	1.87	90.5	1.87	90.0	0	-0.5	5.55
7	0.87	0	0.87	-0.6	0	-0.6	4.76	0.52	149.9	0.52	149.3	0	-0.6	4.76
11	0.56	180	0.56	179	0	-1.0	5.05	0.38	197.6	0.38	196.6	0	-1.0	5.05
13	0.47	0	0.47	-1.2	0	-1.2	5.13	0.22	213.2	0.22	212.0	0	-1.2	5.13

Table 3 Experimental setup specifications

$V_{L\text{-}L}{}^{Grid}$	RMS AC-Side line Voltage	50 V
L	Filter Inductance	8 mH
V_{DC}	DC-Link Voltage	120 V
F_{SW}	Switching Frequency	10 kHz

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