Title: A Simple and Practical PLL for Single-Phase Grid-Tied Inverters Facing with Abnormal Grid Voltage Conditions

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Abstract

As the number of distributed generation (DG) systems connected to the utility grid is increasing, the issue of synchronization between the DGs and the grid is becoming more profound. This paper presents a simple phase-locked loop (PLL) for properly operating the inverters even when the utility grid voltage is subjected to considerable abnormal conditions, such as changes in frequency and voltage amplitude or the presence of grid voltage harmonics. The proposed PLL is based on zero-crossing points, which makes it robust and compatible with various grid voltage frequencies and amplitudes. Since in the proposed PLL the grid voltage phase and amplitude are extracted without the Park matrix and notch filter, it demands a lower number of clocks for the calculations with respect to the existing methods. This feature is practically desired since the proposed PLL can be executed on a simple and low-cost microcontroller. The performance of the proposed PLL has been evaluated by simulation and experimental tests. The results demonstrate the functionality of the proposed PLL on a 1.3 kW single-phase inverter.

Keywords: Distributed generation, Solar panels, phase locked loop (PLL), abnormal grid voltage, zero-crossing PLL.

I. Introduction

Renewable energies have been considered a very important source in recent years to reduce greenhouse gas generation. Accordingly, as a main member of renewable resources, solar photovoltaic (PV) systems are becoming widespread. Based on new reports the total global installed capacity of PV systems exceeds 295 GW [1]. PV systems generate electrical energy in DC current and require high-power inverters to connect them to the electric grid. Therefore, the inverter output voltage phase must be exactly the same as that of the grid voltage to avoid fault currents for the inverters. Due to the increasing number of grid-tied inverters, their synchronization to the utility grid plays an important role. Thus, Phase-Locked Loop (PLL) controllers are used to synchronize the inverter output voltage waveform with that of the grid. From a control viewpoint, a PLL is a feedback control system that is able to generate an output signal, whose phase and frequency are synchronized with the input reference signal [2].

Figure 1 presents a generic block diagram of a PLL. According to Figure 1, PLL can be divided into three blocks. The first block is set to detect the phase of the input signal of the system (X) and is called the phase detector (PD). The second block is a loop filter (LF) that originally is a low-pass filter, and the third one is a voltage-controlled oscillator (VCO) that produces the output signal (Y) using the phase signal extracted in the first block [3], [4].

Single-phase PLLs are classified into two major categories: power-based PLLs (PPLLs) [5], [6] and quadrature signal generation-based PLLs (QSG-PLLs) [7]-[10]. This classification is mainly based on the PD of PLLs. The PPLLs employ a mixer or product-type PD for generating the phase error information. A by-product of such PD is a double-frequency disturbance term, which results in double-frequency oscillatory errors. One of the disadvantages of PPLL is that it does not provide any information about the grid voltage amplitude. Low-pass filter-based PPLL, (LPF-PPLL) [8] and notch-filter based PPLL (NF-PPLL) [12] are the most important PLLs in this category, which respectively use LPF and notch filter in the PLL control loop to mitigate the double-frequency disturbance. The double frequency signal omission using the LPF necessitates a low cut-off frequency for the LPF. This LPF consequently leads to a significant phase delay in the PPLL control loop which results in a very slow transient behavior in the PPLL closed loop structure. It is worth mentioning that the LPF-PPLL has the capability of high harmonic filtering and electromagnetic compatibility. The most important issue of

NF-PPLLs is their vulnerability against changes in the grid voltage frequency. In [9], exclusion of the double-frequency term by using an infinite impulse response non-adaptive filter (IIR-NF) is recommended. The IIR-NF bandwidth determination strictly depends on the predictable variations range of the grid operation frequency. In occasions with large frequency drifts, a wide bandwidth for the NF should be deliberated. This determination significantly removes the double-frequency signal. However, the same as previous method a considerable phase delay is generated resulting in a slow transient response in this type of PPLL [10].

The QSG-PLLs are also known as single reference frame PLLs (SRF-PLLs) equipped with an additional circuit/filter/algorithm that is responsible for the provision of a fictitious quadrature signal [11], [12]. The first category of QSG-PLLs is the transfer delay PLL (TD-PLL) [13], which uses transfer delay to produce an orthogonal beta signal. The main disadvantage of TD-PLL is that if the grid voltage frequency is non-nominal, the beta component will not be orthogonal, and this leads to the production of double-frequency and offset errors. To mitigate the aforementioned problems of the standard TD-PLL, the non-frequency dependent PLL (NTD-PLL) is introduced in [14], [15]. However, this method leads to a similar non-orthogonality existing between V_α and V_β under significant frequency drift conditions. The other type of OSG-PLLs works based on inverse Park transform (IPT) namely IPT-PLLs [7]. In IPT-PLLs, the artificial orthogonal signal is generated by applying the IPT to the filtered dq-axis voltage components. By doing so, selecting the number of filtering modules involves a tradeoff between the detection accuracy and computational load [8],[16]. As another type of QSG-PLLs, second-order generalized integrator-PLL (SOGI-PLL) [17] provides the artificial orthogonal signal by integration of the main signal. The main limitation of SOGI-PLL is the slow frequency response. The synthesis circuit PLL (SC-PLL) [18], [19] constructs the orthogonal signal by using the estimated amplitude and phase angle. The attendance of harmonics in the SC-PLL input reduces its functionality. In derivative PLL (DPLL), the fabricated orthogonal signal is produced by using a differentiator [20].

In the aforementioned PLLs, the proper operation is resulted at the expense of high-level calculations. These complex calculations demand high-performance and expensive microcontrollers. In addition, in most of the existing PLLs, the proper functionality of the closed-loop system is very sensitive to the existing noise. Moreover, multiple items and feedback signals result in poor performance in abnormal grid voltage conditions where the frequency and amplitude of the grid

voltage vary considerably. More importantly, in the mentioned PLLs, the control parameters of PLL are tuned for a nominal frequency and they face deficiency when the grid voltage frequency changes.

This paper proposes a Zero-Crossing method based PLL for non-ideal power grid or abnormal grid voltage conditions. The main benefit of the proposed PLL is a simple parameter tuning for proper operation of the inverter in abnormal grid voltage conditions, such as changes in frequency and voltage amplitude or the presence of harmonics in the grid voltage. In the proposed PLL, a part of an EPLL is also used to calculate the peak grid voltage [21].

The remaining paper is organized as follows: Section II presents the theoretical aspects of the topology of the proposed PLL. In Section III the performance of the proposed PLL method has been evaluated by simulating in the MATLAB/Simulink environment. Section IV presents the experimental results and their analysis for demonstrating the validity of the proposed PLL on a 1.3 kW prototype.

II. PROPOSED PLL

The proposed PLL is depicted Figure 2. This PLL is based on zero-crossing points of signals, which are divided into three sections, as shown in Figure 2. The first section is the main part of the proposed PLL that estimates the grid voltage phase, and the second and third sections are optional to use in a grid-tied inverter current control loop and are responsible for calculating the peak of the grid voltage. The third section generates the signal that is orthogonal with the grid voltage, which is used in the current control loop of the single-phase grid-tied inverters. The first section consists of the PD section, PI controller, and integrator. The principle of operation of the PD section is shown in Figure 3.

A. Operation Principle of the proposed PD section

The PD section is responsible for detecting the phase error between the estimated and the real grid voltages. In Figure 3, V_g is the grid voltage, theta is the PLL output phase and flags are responsible for the PD section to work on the edges. The PD section compares the zero-crossing points of grid voltage with the PLL output phase. The output of the PD section will be either 0, 1, or -1 and this output is obtained based on fuzzy logic mechanism. According to this mechanism, if the grid voltage becomes zero earlier than the PLL output phase, as shown in Figure 4, then the fuzzy logic controller output of the PD section will be 1, in Δt time interval. Once the PLL output phase becomes zero earlier than the grid voltage, the output of

the PD will decrease by one unit. As a result, the fuzzy logic controller is responsible in each half cycle and around the zero crossing points to reduce the time of Δt so that the zero crossing points coincide.

The accuracy of the matching of two signals depends on the clock frequency of the microcontroller, which usually cannot be considered too large to avoid the input noise in the control loop and is usually considered below 50 kHz. Since the PI acts like a low-pass filter the oscillations between (-1) and (+1) with a frequency of 24 kHz will be completely attenuated and will not be transmitted to the output of the PI.

The transfer function of this PI controller is given in (1).

$$G_{PI}(S) = K_p + \frac{K_i}{S} \tag{1}$$

Optimized values of K_P and K_i give a proper trade-off between stability and dynamic response. The output of the PI controller will be set to the corresponding $\Delta\omega$ by controlling the error, as given in (2). Therefore, the zero crossing points of the PLL output phase will match those of the grid voltage.

$$\Delta\omega = \frac{2\pi}{\Delta t} \tag{2}$$

B. Guidelines for Designing PI Coefficients

It should be noted that the control parameters of the proposed PLL are designed using the symmetrical optimum method [22], so that the maximum possible stability margin for the proposed PLL is achieved and it has to remain synchronized with the grid voltage during the abnormal grid voltage conditions.

Based on the first section of Figure 2, the small-signal model of the proposed PLL can be obtained, as shown in Figure 5. In Figure 5, *D(s)* is a disturbance input to the PLL small-signal model. From Figure 5, the closed-loop transfer function can be written as

$$\hat{\theta}(S) = G(S)\left[\theta(S) + D(S)\right] \tag{3}$$

,where

$$G(S) = \frac{K_p S + K_i}{S^2 + K_p S + K_i} \tag{4}$$

The system stability is guaranteed, if K_P and K_i are positive. Note that, in addition to this condition, the proposed PLL open-loop bandwidth must be appropriately determined to ensure a robust dynamic response. The open-loop transfer function of the proposed PLL can be derived as

$$G_{ol}(S) = \frac{K_p\left(S + \frac{K_i}{K_p}\right)}{S^2} \tag{5}$$

Based on [22], the phase margin (PM) is maximized when the proportional gain K_P is equal to the crossover frequency ω_c. The value of the crossover frequency is determined based on the restrictions mentioned in [23].

$$K_P = \omega_c \quad ; \quad K_i = \frac{\omega_c^2}{K} \tag{6}$$

where K is a constant value. From (5) and (6), PM can be derived as

$$PM = tan^{-1}(K) \tag{7}$$

The recommended value for a proper phase margin is [24]

$$\pi/6 < PM < \pi/3 \tag{8}$$

To meet this, we need

$$0.58 < \mathrm{K} < 1.73 \tag{9}$$

C. Interrelation of the Proposed PLL and Inverter Current Control Loop

In many single-phase grid-tied inverter control methods, employing park transformation, it is necessary to generate (V_α) and (V_β) signals [25], [26]. (V_α) is the same as the grid voltage but (V_β) is orthogonal with the grid voltage. So, to make an interrelation between the proposed PLL and inverter control loop, the equations (10-13), the second and the third sections of Figure 2, are implemented in digital form to be used in the microcontroller [27], [28].

$$error = \left(V_g[n] - V_g^{peak}[n]\right).\sin(\theta) \tag{10}$$

$$out[n] = error\ .V_g^{peak}[n].\sin(\theta) \tag{11}$$

$$V_g^{peak}[n] = \frac{\left(out[n] + out[n-1]\right)}{f_s} + V_g^{peak}[n-1] \tag{12}$$

$$V_\beta[n] = b_0\left(u[n] - u[n-2]\right) + a_1\ .\ V_\beta[n-1] + a_2\ .V_\beta[n-2] \tag{13}$$

In equations (10-13), V_g is the grid voltage, V_g^{peak} is the peak value of grid voltage, θ is the PLL output phase, f_s is the sampling frequency and b_0, a_1, a_2 are given in (14-16):

$$b_0 = \frac{\left(\omega_n\ .T_S\right)}{\left(\omega_n\ .\ T_S + \omega_n^{\,2}.T_s^{\,2} + 4\right)} \tag{14}$$

$$a_1 = \frac{\left(8 - 2\left(\omega_n^{\,2}.\ T_s^{\,2}\right)\right)}{\left(\omega_n\ .\ T_S + \omega_n^{\,2}\ .\ T_s^{\,2} + 4\right)} \tag{15}$$

$$a_2 = \frac{\left(\omega_n\ .T_S - \omega_n^{\,2}\ .\ T_S^{\,2} - 4\right)}{\left(\omega_n\ .\ T_S + \omega_n^{\,2}\ .\ T_s^{\,2} + 4\right)} \tag{16}$$

In order to prove the functionality of the proposed PLL in the closed-loop single-phase inverter, this paper has tried to use the desired PLL in the converter current control, as shown in Figure 6.

D. Comparing the proposed PLL with existing single-phase PLLs

Table I compares the performance of the proposed PLL with some common single-phase PLLs. The most significant advantage of the proposed method is its simple tuning for proper operation under abnormal grid voltage conditions. Since this method operates based on zero-crossing points, if its bandwidth is appropriately

selected, it performs well over a wide frequency range. The instability of EPLL is very high with frequency variations, and efforts have been made to address this issue in [29]. Additionally, although the proposed PLL does not have harmonic rejection capability, it demonstrates good performance under voltage distortion conditions due to the absence of the double frequency component in the PLL control system. In contrast to the LPF-PPLL and NF-PPL methods, which use filters to eliminate this component and result in phase delay at their outputs, the output phase of the proposed PLL has no delay. Furthermore, a part of an EPLL has also been used complementarily in the proposed PLL structure to calculate the grid voltage amplitude while maintaining the simplicity of the proposed PLL's structure and ensuring that the proposed PLL remains stable under the grid voltage sag conditions.

III. SIMULATION RESULTS

In this section, the proposed PLL for a single-phase inverter that is connected to the grid is considered, and its performance in abnormal grid conditions is evaluated through MATLAB/Simulink. The specification of the considered case study is provided in Table II.

To have a stable PLL, an appropriate PI controller is designed with the values of K_P and K_i in Table II. Figure 7 Presents the bode diagram of the closed loop of the proposed PLL.

With the parameters of TABLE II, different scenarios for the grid voltage abnormal conditions are considered and the performance of the proposed PLL is assessed.

A. Grid Voltage Frequency Change

Unexpected frequency variation from nominal value indicates an emergency situation where quick response should be taken into account. The proposed PLL has been tuned to minimize the steady state error and settling time. Since the PD part is based on the zero-crossing points, the proposed PLL works well in different frequencies, as shown in Figure 8 and Figure 9. In Figure 8, the grid frequency is 50 Hz, at 2s, has changed to 55Hz and drops by to 50Hz at 4s. Figure 9- (a) and (b) also show the PLL output phase of the system when the grid voltage frequency is 50Hz and 60Hz, respectively, and based on that, the zero crossing points of the PLL output phase are completely consistent with the grid voltage, and it can be concluded that the proposed PLL is very flexible against frequency change.

B. Grid Voltage Sag

In Figure 10 the amplitude of the single-phase grid voltage drops by 50% at 0.5s and it increases by 50% at 1s. It can be concluded, that the proposed PLL detects the change of the grid voltage amplitude and has a proper transient.

C. Grid Voltage Harmonic Distortion

The acquired result is shown in Figure 11 reveal that even when the grid voltage THD is 10% and has the harmonic content of 9.5%, 5%, and 1 % for 3^{rd} , 5^{th} and 7^{th} harmonics, respectively, after 0.35 seconds, the PLL output sinusoidal signal matches the grid voltage, and the proposed PLL performs optimally.

Although the grid voltage has a relatively high THD, the single-phase grid-tied inverter has become stable and the proposed PLL has correctly found the grid voltage phase. As a result, the presence of harmonics in the grid voltage does not cause the wrong detection of zero crossing points.

D. All Abnormal Grid Voltage Conditions

In order to evaluate the performance of the proposed PLL in very challenging conditions, this paper assumed that the harmonic distortion of the grid voltage is similar to section C and at the same time, its amplitude and frequency changes. The results of this simulation are shown in Figure 12. The frequency of the grid voltage decreases from 50 Hz to 47 Hz at 1 s, and the amplitude of the single-phase grid voltage drops by 50% at 1s, as shown in Figure 12- (a). As can be seen, after 4 cycles, the PLL output sinusoidal signal matches the input signal. Similarly, in Figure 12-(b), the frequency of the grid voltage increases from 47 Hz to 50 Hz at 2 s and the amplitude of the single-phase grid voltage increases by 50% at 2s, and the PLL output sinusoidal signal is synchronized with the input signal after 5 cycles.

The simulation results prove the robust performance of the proposed PLL in abnormal grid conditions. Despite the simple structure of the proposed PLL, it has provided an acceptable performance in the presence of severe grid disturbances and is not much influenced by these disturbances.

IV. EXPERIMENTAL RESULTS

In this section, the performance of the proposed PLL has been evaluated in a laboratory environment. The proposed PLL is implemented on an STM32 H743ZIT6 ARM microcontroller. The experimental setup of the single-phase grid-tied inverter is shown in Figure 13. The experimental tests contain two sections. In the first section, the proposed PLL operation is tested with a function generator that

can inject arbitrary sine wave frequencies simulating an artificial grid with different frequencies. In addition, different artificial grid voltage amplitude can be applied by the function generator. In the second section, the proposed PLL operation is tested in close-loop control of an inverter that is connected to the grid. The specification and important parameters of this inverter are presented in TABLE III. The current control system provided in Figure 6 is used to control this inverter. For safety purposes, the grid voltage is reduced to 110 V using a variable transformer. To ensure the reliability of IGBTs and manage the power loss, the switching frequency is considered to be 8 kHz. Additionally, short circuit current limiting techniques for IGBTs have been used to avoid IGBT failures [30]. More importantly, to cease shoot-through currents, a negative bias for IGBT gate drivers is provided [31].

Different abnormal scenarios are tested to verify the functionality of the proposed PLL. In addition, its performance is verified in both the off-grid and on-grid operation of the inverter.

I. Artificial grid frequency applied by the function generator

In this test, the function generator is used to provide various sine wave signals as input for the PLL block diagram.

A. Grid Voltage Frequency Change

Since the PD part of the proposed PLL is based on the zero-crossing points, The PLL output phase changes according to the frequency change of the input voltage, and its zero-crossing points will coincide with the zero-crossing points of the input voltage at different frequencies, as shown in Figure 14 . One of the advantages of this PLL is that the PI coefficients in all three tests will not need to be changed, this will cause the proposed PLL to be stable at different frequencies.

B. Voltage Sag

Figure 15 shows the grid voltage sample change. As can be seen, after 1 cycle, the grid voltage sample peak value is estimated. As can be seen, the estimated peak value is exactly equal to the grid peak value.

C. Harmonic Distortion and Change of Frequency

In consistency with the simulation procedure, the same process is carried out in the experiment to justify the performance of the presented PLL. Accordingly, a voltage with harmonics along with the frequency change was applied to the PLL input at a certain time. In Figure 16, and Figure 17, the performance of the presented

PLL has been checked by injecting harmonics into the input voltage and changing the input frequency from 47 to 50 Hz and 50 to 47 Hz. As it can be seen since the PD part is based on the zero-crossing points of the signals, PLL performs correctly. Since no filter is used in the proposed PLL, the input harmonics are transferred to the output. However, the priority of this article is simplicity and maintaining the stability of the grid-tied inverter.

II. The Overall Off-Grid and On-Grid Performance of the Single-Phase Inverter

In order to prove the functionality of the proposed PLL in the single-phase inverter control, this experiment has tried to use the desired PLL in the block diagram of a conventional current control shown in Figure 6. In the power tests of inverter Q^* is assumed to be zero. Therefore, the current must be in phase with the grid voltage.

In the first step, the performance of the inverter in an off-grid state is evaluated. Figure 18 presents the output power signals of the inverter. According to Figure 18, the inverter output voltage is completely in phase with the grid voltage. In addition, the inverter output current has the same phase as the inverter output voltage. Thus, it can be concluded that the PLL performs appropriately in off-grid conditions. Secondly, the performance of the PLL and the current control loop is assessed in on-grid conditions. Figure 19 presents the output power signals of the inverter connected to the grid. In a grid-connected state, also synchronism is provided and the inverter generates the unity power factor current. Figure 20, presents the output of the power analyzer to indicate the harmonic content of the inverter current. As can be seen in Figure 20, the grid current THD is 2.4%, and the harmonic contents of the grid current in within the limits of IEEE 1547 standard.

V. Conclusion

This paper presented a PLL based on Zero-Crossing using a fuzzy logic controller for a Non-ideal power grid. Experimental results implemented in the STM32H743ZIT6 ARM controller, show the effectiveness of the proposed PLL method for abnormal grid voltage conditions. To prove that the proposed PLL is less sensitive to the coefficients of the dedicated PI controller, the proposed PLL is tested on three different frequencies with the same coefficients of the PI controller. The achieved results indicate the proper operation of the PLL without adjusting the PI controller coefficients. The other experimental results show that the proposed PLL can work properly under abnormal grid voltage conditions such as changing voltage

amplitude and injecting harmonics in the grid voltage. Finally, its performance has been evaluated by using the proposed PLL in the current control loop of a 1.3 kW single-phase grid-tied inverter, which results show that this inverter is stable in connected to the grid and disconnected from the grid conditions.

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References

[1] Yang, H., Mingyu, L., Xin, Z., et al., "Comparative performance evaluation of orthogonal-signal-generators-based single-phase PLL algorithms—a survey," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3932–3944, May 2016, doi: 10.1109/TPEL.2015.2466631.

[2] Liming, L., Hui, L., Zhichao, W., et al., "A cascaded photovoltaic system integrating segmented energy storages with self-regulating power allocation control and wide range reactive power compensation," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3545–3559, Dec. 2011, doi: 10.1109/TPEL.2011.2168544.

[3]Saeed, G., Mohammad, M., Francisco D. F., et al., "Design and tuning of a modified power-based PLL for single-phase grid-connected power conditioning systems," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3639–3650, Aug. 2012, doi: 10.1109/TPEL.2012.2183894.

[4] Saeed, G., Mohammad, M., Francisco, D. F., et al., "Dynamics assessment of advanced single-phase PLL structures," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2167–2177, Jun. 2013, doi: 10.1109/TIE.2012.2193863.

[5] Furong, X., Lei, D., Li, L., et al., "A frequency-fixed SOGI-based PLL for single-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1713–1719, Mar. 2017, doi: 10.1109/TPEL.2016.2606623.

[6] Qingxin, G., Yu, Z., Yong, K., et al., "Single-phase phase-locked loop based on derivative elements," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4411–4420, Jun. 2017, doi: 10.1109/TPEL.2016.2602229.

[7] Timothy, T., Ruxi, W., Dong, D., et al., "Phase-locked loops using state variable feedback for single-phase converter systems," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Washington, DC, USA: IEEE, Feb. 2009, pp. 864–870. doi: 10.1109/APEC.2009.4802763.

[8] Rubens, M. S. F., Paulo, F. S., Porflrio, C. C., et al., "Comparison of three single-phase PLL algorithms for UPS applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2923–2932, Aug. 2008, doi: 10.1109/TIE.2008.924205.

[9] Francisco, D. F., Jesus, D., Oscar, L., et al., "Robust phase locked loops optimized for DSP implementation in power quality applications," in *2008 34th Annual Conference of IEEE Industrial Electronics*, Orlando, FL: IEEE, Nov. 2008, pp. 3052–3057. doi: 10.1109/IECON.2008.4758447.

[10] Saeed, G., Josep, M. G., and Gevork, B. G., "Five approaches to deal with problem of DC offset in phase-locked loop algorithms: design considerations and performance evaluations," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 648–661, Jan. 2016, doi: 10.1109/TPEL.2015.2408113.

[11] Ashish, Abhishek, Sonam, G., et al., "A comparative analysis of SRF-PLL and EPLL for grid connected converter," in *2023 11th National Power Electronics Conference (NPEC)*, Guwahati, India: IEEE, Dec. 2023, pp. 1–6. doi: 10.1109/NPEC57805.2023.10384922.

[12] Gerardo, E., Luis, I., Jesus E. V., et al., "Nonlinear stability analysis of the conventional SRF-PLL and enhanced SRF-EPLL," *IEEE Access*, vol. 9, pp. 59446–59455, 2021, doi: 10.1109/ACCESS.2021.3073063.

[13] Mohd., A. A., Suman, S., and Ramandip, S., "A second look on nonfrequency-dependent transport delay-based PLL: performance enhancement under frequency deviations," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13365–13371, Dec. 2021, doi: 10.1109/TPEL.2021.3090955.

[14] Saeed, G., Josep, M. G., Ana, V., et al., "Small-signal modeling, stability analysis and design optimization of single-phase delay-based PLLs," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3517–3527, May 2016, doi: 10.1109/TPEL.2015.2462082.

[15] Mohd., A. A., Suman, S., Dibyendu, P., et al. "A systematic approach to design amplitude estimators for NTD-PLL: performance improvement under abnormal grid disturbances," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 5456–5468, Apr. 2023, doi: 10.1109/TPEL.2022.3226242.

[16] Naima, I., Abdelahdi, B., Ahmed, H., et al., "PLL synchronization method based on second-order generalized integrator for single phase grid connected inverters systems during grid abnormalities,"

in *2019 International Conference on Wireless Technologies, Embedded and Intelligent Systems (WITS)*, Fez, Morocco: IEEE, Apr. 2019, pp. 1–5. doi: 10.1109/WITS.2019.8723856.
[17] Sherla, V. P., Satyabrata, B., Venkata, R. N. N., et al., "SOGI-PLL based control technique for the single-phase single-stage grid connected PV system," in *2023 First International Conference on Cyber Physical Systems, Power Electronics and Electric Vehicles (ICPEEV)*, Hyderabad, India: IEEE, Sep. 2023, pp. 1–5. doi: 10.1109/ICPEEV58650.2023.10391943.
[18] Xiong, F., Yue, W., Ming, L., et al., "A novel frequency-adaptive PLL for single-phase grid-connected converters," in *2010 IEEE Energy Conversion Congress and Exposition*, Atlanta, GA, USA: IEEE, Sep. 2010, pp. 414–419. doi: 10.1109/ECCE.2010.5618000.
[19] Masoud, K. G., "*Enhanced phase-locked loop structures for power and energy applications*," 1st ed. Wiley, 2014. doi: 10.1002/9781118795187.
[20] Ilya, G., and Maxim, V., "Optimizing of sampling in a low-cost single-phase instantaneous AC-grid synchronization unit with discrete calculation of derivative function," in *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, Yokohama: IEEE, Nov. 2015, pp. 004538–004543. doi: 10.1109/IECON.2015.7392807.
[21] Santosh, K. B., Shiban, K. K., Ananjan, B., "Simultaneous measurement of oscillator amplitude and phase noise using phase detector based EPLL," in *2021 IEEE MTT-S International Microwave and RF Conference (IMARC)*, KANPUR, India: IEEE, Dec. 2021, pp. 1–4. doi: 10.1109/IMaRC49196.2021.9714531.
[22] Saeed, G., Mohammad, M., Francisco D. F., et al., "Design and tuning of a modified power-based PLL for single-phase grid-connected power conditioning systems," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3639–3650, Aug. 2012, doi: 10.1109/TPEL.2012.2183894.
[23] Narendra, B. Y. and Narayana, P. P., "Investigation of damping effect of PLL on low-frequency harmonic stability of grid-tied inverter with *αβ* and *dq* current control schemes," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 10, no. 1, pp. 1046–1060, Feb. 2022, doi: 10.1109/JESTPE.2021.3079463.
[24] Masoud, H. N., Mario, I., and Jorge, P. L., "Dynamic stability and control design of modern electric energy systems with large penetration of distributed generators," in *2010 IREP Symposium Bulk Power System Dynamics and Control - VIII (IREP)*, Rio de Janeiro, Brazil: IEEE, Aug. 2010, pp. 1–7. doi: 10.1109/IREP.2010.5563270.
[25] Mohammad, E., Sayed, A. K., and Masoud K., "Fast and robust single-phase DQ current controller for smart inverter applications," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3968–3976, May 2016, doi: 10.1109/TPEL.2015.2474696.
[26] Muhammad, W. J., *et al.*, "DQ transformation based control of single-phase grid-tied inverter," in *2021 31st Australasian Universities Power Engineering Conference (AUPEC)*, Perth, Australia: IEEE, Sep. 2021, pp. 1–6. doi: 10.1109/AUPEC52110.2021.9597712.
[27] Cheng, C., Peng, Y., Shuang, L., et al., "Analysis and modeling of hybrid analog-digital PLL," in *2021 IEEE 15th International Conference on Electronic Measurement & Instruments (ICEMI)*, Nanjing, China: IEEE, Oct. 2021, pp. 332–335. doi: 10.1109/ICEMI52946.2021.9679553.
[28] In-Woo, J., and Min-Seong, C., "Direct phase control in digital phase-locked loop mitigating loop delay effect inside digital filter," in *2023 International Conference on Electronics, Information, and Communication (ICEIC)*, Singapore: IEEE, Feb. 2023, pp. 1–2. doi: 10.1109/ICEIC57457.2023.10049900.
[29] Saeed, G., Jose, M., Abdullah, M. A., et al.,"More-stable EPLL," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 1003–1011, Jan. 2022, doi: 10.1109/TPEL.2021.3099839.
[30] Sadegh, M., Javad, N., and Kamyar, M., "Reliability enhancement of power IGBTs under short-circuit fault condition using short-circuit current limiting-based technique," *Energies*, vol. 14, no. 21, Art. no. 21, Jan. 2021, doi: 10.3390/en14217397.
[31] Amir, A. R., and Sadegh, M., "Investigating the effect of the power path parasitic inductance on Si-IGBT Crosstalk Using a Comprehensive Model," in *2022 13th Power Electronics, Drive Systems, and Technologies Conference(PEDSTC)*, Feb. 2022, pp. 414–419. doi: 10.1109/PEDSTC53976.2022.9767324.

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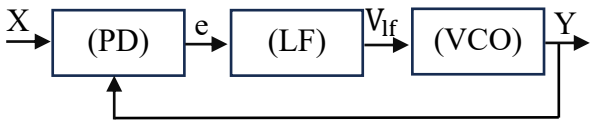


Figure 1: The Basic structure of a PLL

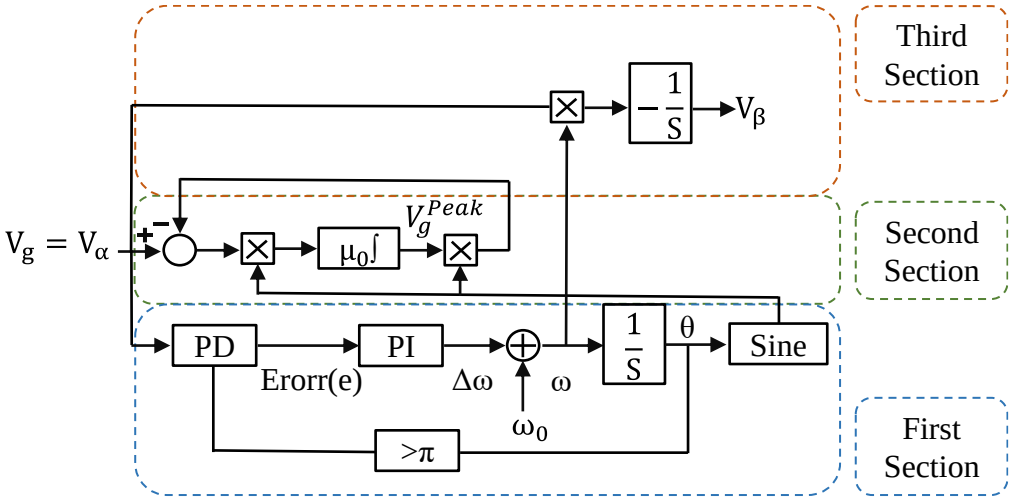
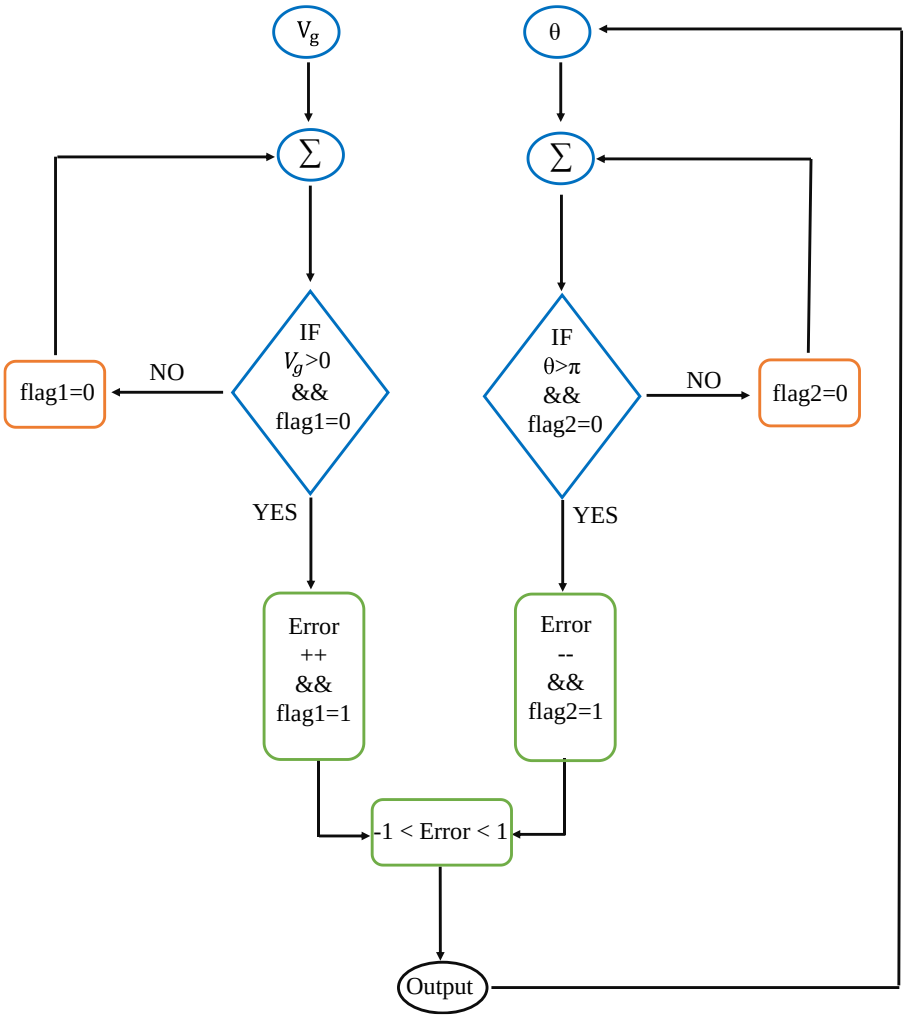


Figure 2: The structure of the proposed PLL.



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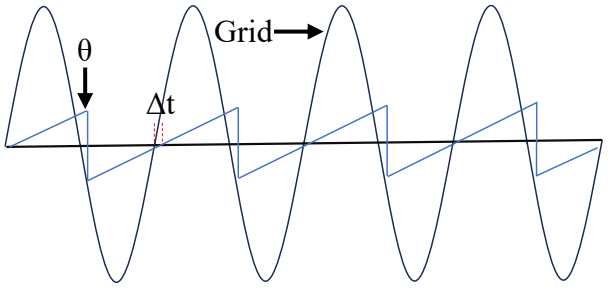


Figure 4: PLL output phase (θ) and grid voltage status when the grid voltage equals zero earlier than the PLL output phase.

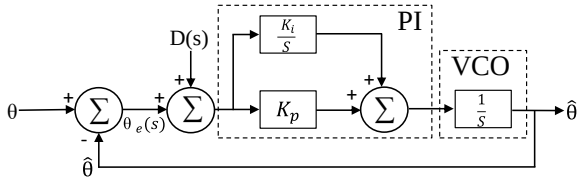


Figure 5: Small-signal model of the proposed PLL

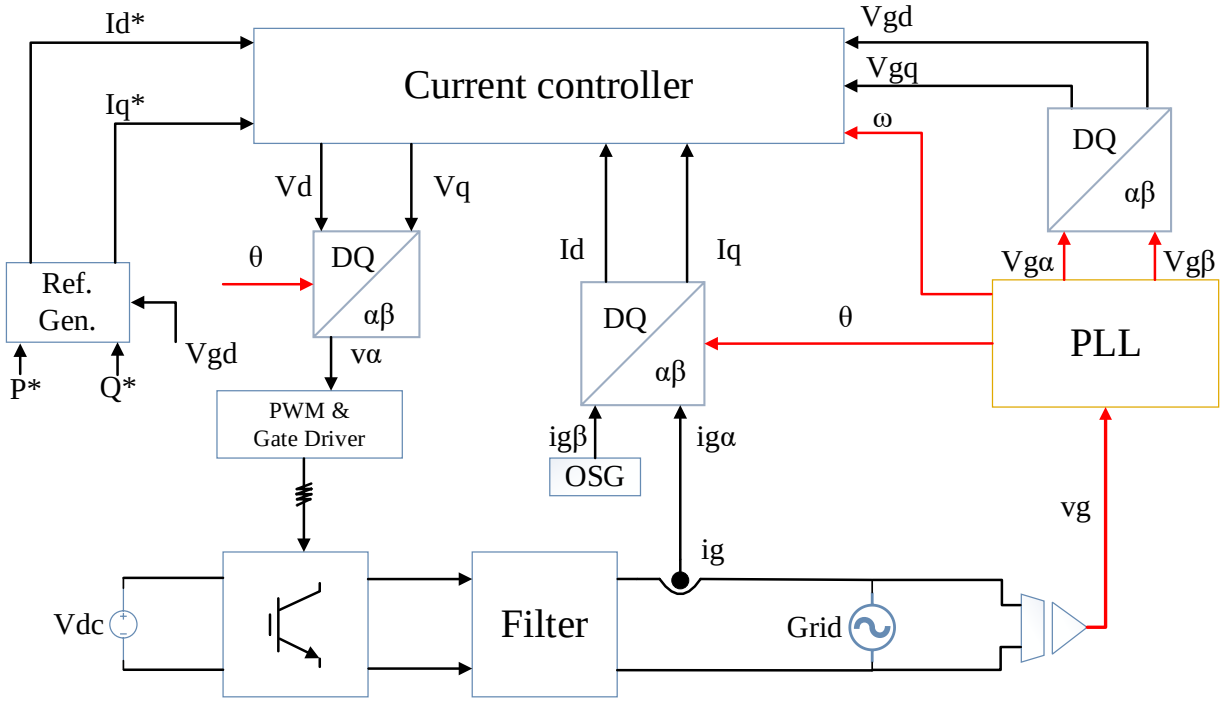


Figure 6: Block diagram of a current control single-phase grid-tied inverter using proposed PLL.

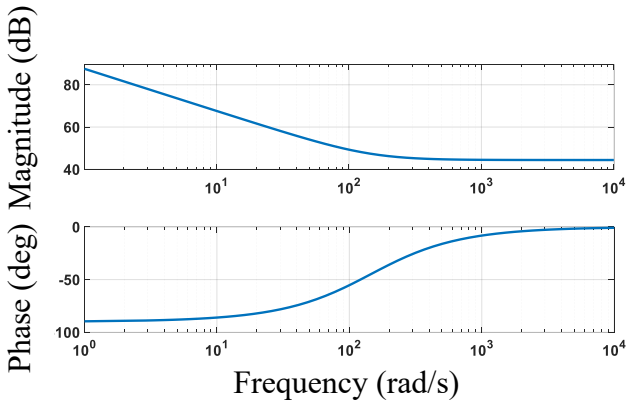


Figure 7: Bode diagram of the closed loop the proposed PLL.

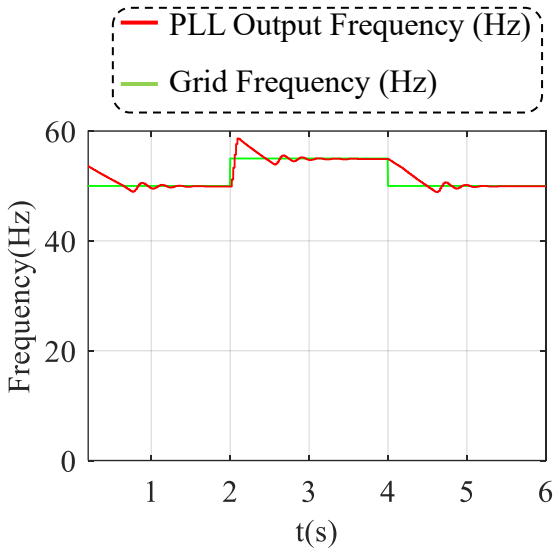
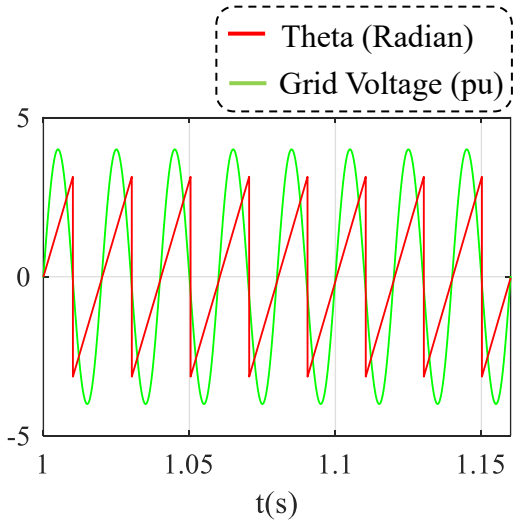
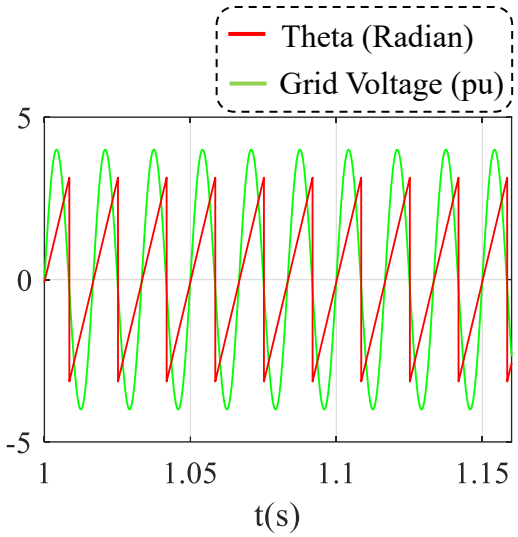


Figure 8: PLL output frequency when nominal grid frequency is at 50 Hz and this grid frequency changes.



(a)



(b)

Figure 9: PLL output phase and grid voltage at 50 Hz frequency (a). PLL output phase and grid voltage at 60 Hz frequency (b).

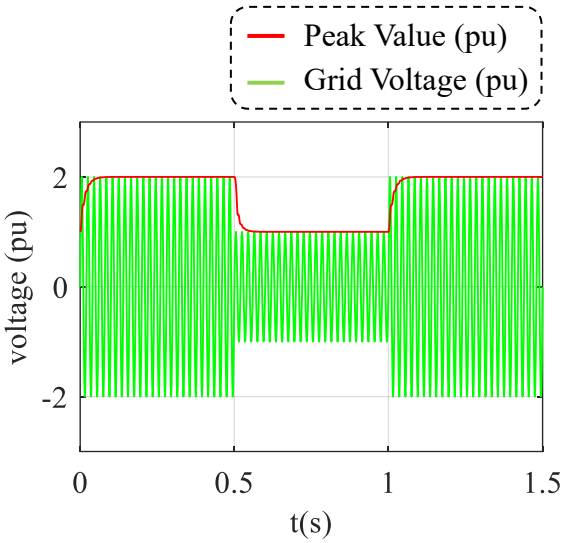


Figure 10: Simulation result, Peak value grid voltage detection.

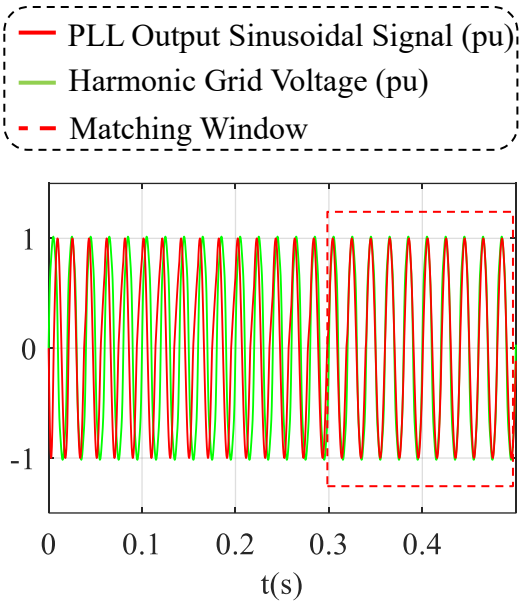
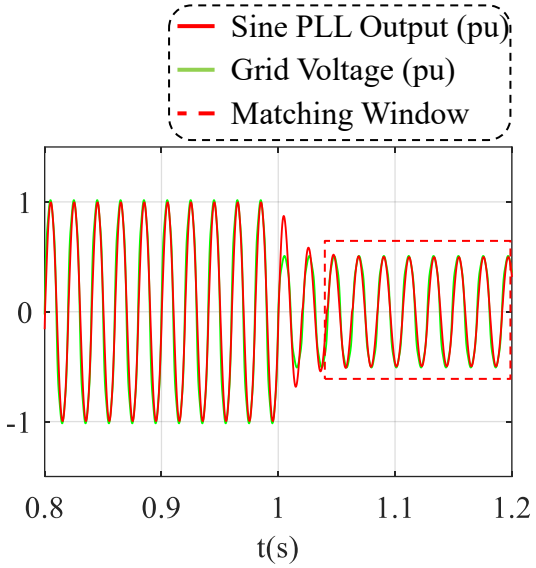
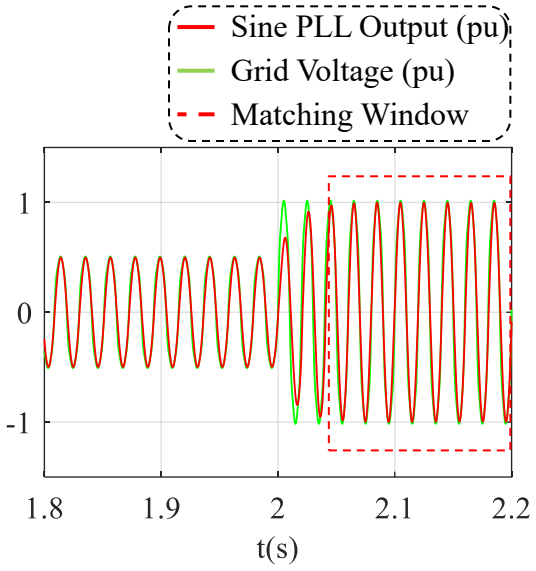


Figure 11: The PLL output sinusoidal signal and harmonic grid voltage (Grid voltage THD = 10%)



(a)



(b)

Figure 12: PLL outputs sinusoidal signal and grid voltage in the situation where the grid voltage has harmonic distortion and its amplitude and frequency decrease (a). PLL output sinusoidal signal and grid voltage in the situation where the grid voltage has harmonic distortion and its amplitude and frequency increase (b).

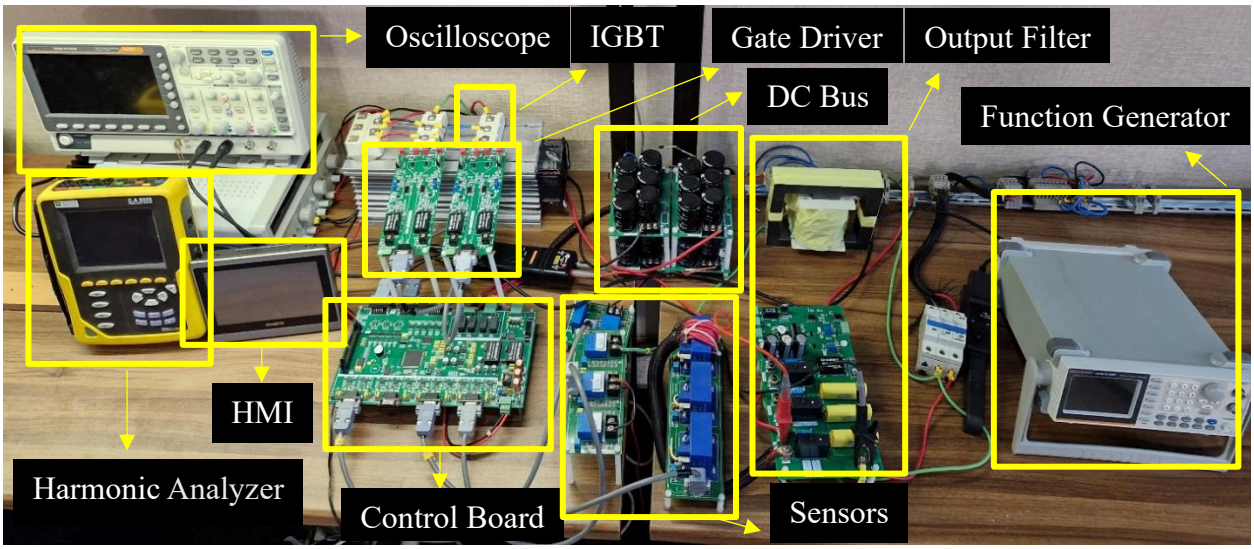
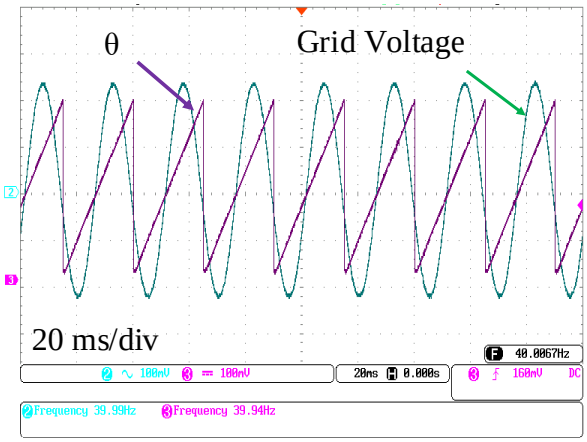
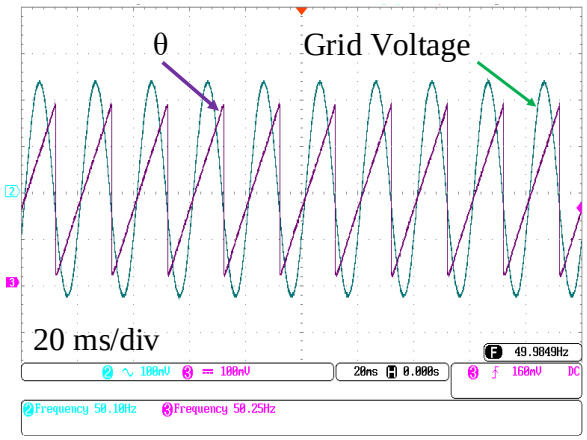


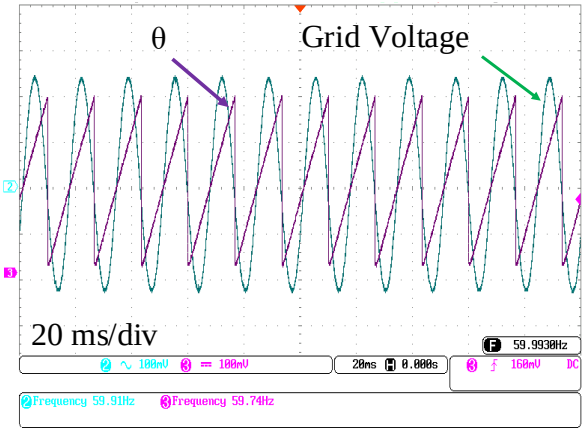
Figure 13: The experimental setup of the single-phase grid-tied inverter.



(a)



(b)



(c)

Figure 14: Experimental result, PLL output phase and grid voltage at 40 Hz frequency (a). Experimental result, PLL output phase and grid voltage at 50 Hz frequency (b). Experimental result, PLL output phase and grid voltage at 60 Hz frequency (c).

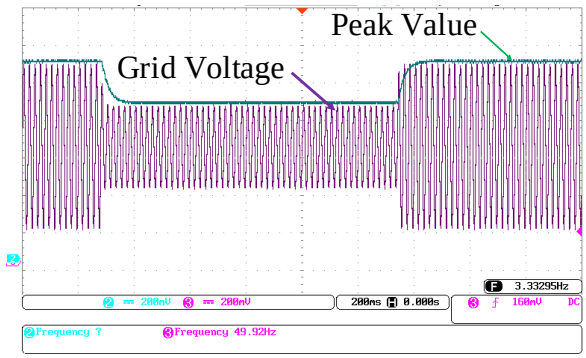


Figure 15: Experimental result, Peak value grid voltage detection.

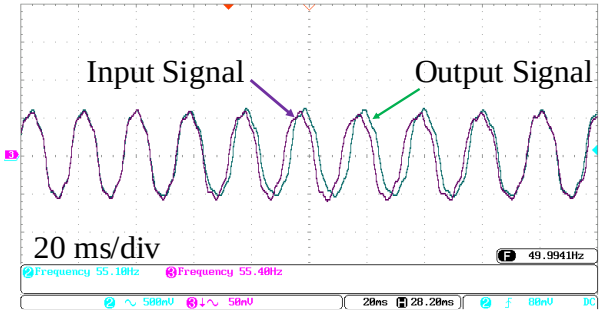


Figure 16: Experimental result, PLL output sinusoidal signal and PLL input harmonic signal with a frequency jump from 50 Hz to 47 Hz.

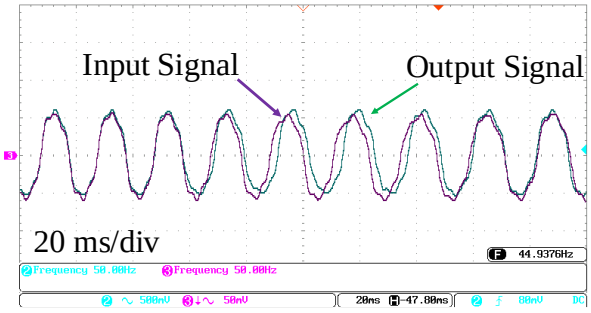


Figure 17: Experimental result, PLL output sinusoidal signal and PLL input harmonic signal with a frequency jump from 47 Hz to 50 Hz.

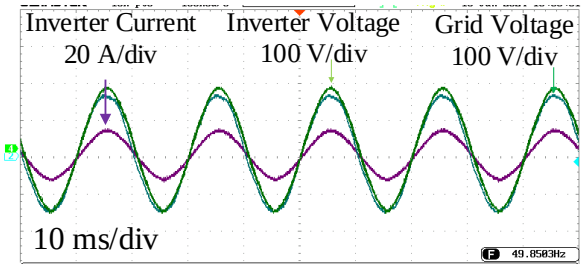


Figure 18: Experimental result, Off-grid grid test using the proposed PLL for synchronizing the inverter output signal with the grid signal.

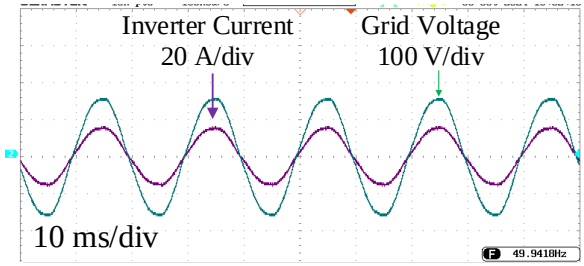


Figure 19: Experimental result, On-grid test using the proposed PLL for synchronizing the inverter output signal with the grid signal.

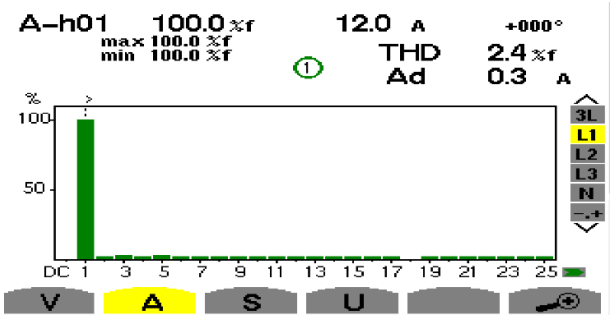


Figure 20: Experimental harmonic measurement for the grid current distortion test. P^* and Q^* are set to 1.3 kW and 0 VAR, respectively.

Table I: COMPARISON OF SINGLE-PHASE PLL METHODS.

	PPLL [6]	NF-PPLL [12]	SC-PLL [20]	EPLL [29]	Proposed PLL
Grid voltage amplitude calculation	-	-	+	+	+
Harmonic rejection	-	+	+	+	-
Simple calculation	+	+	-	-	+
Simple tuning	+	+	-	-	+
Frequency independence	-	-	-	-	+

Table II: SIMULATION PARAMETERS

Parameter	Value
DC link voltage	600 V
Grid voltage	110 V – 220 V (rms)
Grid frequency	40Hz - 60Hz
DC link capacitor	1 mF
Filter Resistance	0.5 Ω
Filter Capacitance	8 µF
Filter inductance	1 mH
Switching frequency	8 kHz
Sampling frequency	24 kHz
K_P	166.61
K_i	24000

Table III: EXPERIMENTAL PARAMETERS

Parameter	Value
DC link voltage	400 V
Grid voltage	110 V (rms)
Artificial grid frequency in the first section tests	47-55Hz
Grid frequency in on-grid tests	50 Hz
DC link capacitor	1 mF
Apparent Power	1.6 kVA
Filter Resistance	0.5 Ω
Filter Capacitance	8 µF
Filter inductance	1 mH
Switching frequency	8 kHz
Sampling frequency	24 kHz
K_P	166.61
K_i	24000

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