Integrated Modeling of Bidirectional Solid-State Transformers with an Arbitrary Number of H-bridge Converters

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Abstract- Solid state transformers (SST) are one of the newest and fastest growing components in the modern power systems. The extended SST has ac/dc, dc/dc and dc/ac stages for full network maneuvering and control. SST modeling is utilized in the analysis and simulation of applications with ac or dc input/output such as smart grids, dc micro grids, renewable energy applications and electrical transportation systems. Modeling, analyzing, designing, simulating and applying the SST is challenging and complex due to the large number of semiconductor switches. As a solution, the averaged models for any stages were presented but these models have some limitations which are number of modules in stages and dynamic and integrated modeling and those are dissolved in this paper. The proposed models are presented in two different forms which are mathematical differential equations; furthermore, equivalent electrical circuits and these models can be used for transient and steady-state analysis of each SST stages separately and interactively. The closed loop control structure has been built for all

SST stages. The averaged differential equations are simulated in SIMULINK/MATLAB software as the simulation results verified the proposed model.

Keywords: Solid State Transformer, Averaged Model, Dynamical Modeling, H-Bridge Topology, Equivalent Circuit.

1- Introduction

Modern electrical energy systems include a variety of electric power generators with different frequencies and amplitudes like wind and solar farm generators. The power electronic converters and traditional transformers may be used to connect these generators to power network. However, traditional transformers have a number of drawbacks that limit the development of smart grids and grid flexibility [1]. As a result of the advent of new forms of power converters and smart grids, researchers have developed a new type of transformer known as SST. These transformers, which are based on semiconductor switches, high frequency transformers and control and protection circuits have numerous advantages over traditional transformers. These electronic transformers considerably increase the network's maneuverability and control [2]. The usage of revolutionary SST technology improves energy transfer efficiency and power quality, in addition to the aforementioned benefits. SST outperforms standard transformers in several applications such as electric transportation systems, offshore power generation systems and the connectivity between distributed generation and smart grids [3,4].

The general structure of SST with high maneuvering and control is depicted in Figure 1. Several studies and research works have looked into this device [2, 5-9], and several ways have been proposed for the structure of Figure 1 to realized [2, 3,9-11]. The SST under investigation is made up of three stages: ac/dc, dc/dc and dc/ac.

In many applications, the input or output voltages level of SST is significantly different from the maximum allowable voltages of traditional switches. One solution is based on silicon-carbide (SiC) technology for power semiconductor switches and the emergence of switches with nominal voltages up to several kilovolts, certain SSTs with fewer modules and lower complexity have been designed and fabricated [6, 12-13]. SST implementation requires fast SiC semiconductors but commercial versions of these high-voltage switches are not yet available.

Another solution is the cascading technique which is used for modules. The number of series modules in these converters is significant therefore, SST has the large number of

semiconductor switches. Modeling, analyzing, designing, simulating and applying the SST is challenging and complex due to the large number of semiconductor switches.

The active H-bridge topology is used in investigated SST while it has many semiconductor switches and is inherently a complex switched system. As a solution,

the averaging theory is applied to the SST and the transformer is modeled in a simple and powerful method.

Considering the final number of switches in SST with numerous stages, it is almost impossible to simulate exact behavior. Consequently, it is essential to utilized averaging theory. The exact simulation with traditional software such as MATLAB/SIMULINK or Pspice is not possible. The investigated SST of this paper has 684 switches totally, therefore; the precise simulation is not reachable.

The previously presented averaged models of SST have some limitations in the type of inputs or outputs (ac or dc), number of modules of stages and dynamical and non-integrated modeling. The separate modeling of SST stages was presented by researchers. The integrated modeling is necessary for transient and steady state analysis and also for simulation of power transformer as a power system device. Moreover, the integrated models provide the required knowledge for SST analysis and simulation as well as controller design.

Simulation and control based on the average modelling strategy has used in [14]. Separate modelling of dc/dc stage has been proposed in [15]. Using the averaging theory and a dynamic model for dc/ac stage is provided in [16]. [17] shows how to model power converters in their fundamental states without taking into account the connection of several stage models. [18] uses the standard state space method for SST modeling and model predictive control and it has the limitation of converter stages. [19] focuses on static modelling of individual power electronic converter modules and proposes a static modelling technique that takes the interaction between models into account. The static modelling of power converters is addressed in [20] and [21]. [22] shows how to model a three-stage SST using PSCAD software. The static behavior is effectively demonstrated by the models offered for each stage. On the other side, these models can't be used to investigate transient state behavior. [23] differs from the current paper in terms of the input stage and the modulation methods used for the dc/dc and dc/ac stages. Moreover, this reference takes a different approach to the integration of stage models than the current paper. The most notable difference between these two articles is the modulation techniques. The [23] has the limitation on number of modules of stages and they are not applicable for higher than 1KV applications. [24] describes the small signal modelling of a

multilevel converter with DC input and DC or AC output. The Thévenin equivalent circuit given in this reference can be used to model solid state transformers. It uses the different topology and modulation method. In [25], the modeling approach is discrete-state event-driven and this approach for basic power electronics converters such as buck or boost is applicable but for SST converters with large number of semiconductors are not usable.

Basic Integrated Modeling of Bidirectional SST for only one-stage converters is done by authors in [26]. In this presented paper, by generalizing the previous researches, in ac/dc stage, the load is an isolated dc/dc converter and in dc/dc stage, the load is an dc/ac stage. In dc/ac stage, modeling is done in conditions where the input power is given by a dc/dc converter, and the methods presented in [8,16] are generalized for dc/ac stage modelling. The dynamical resulting model successfully integrates the SST and addresses the interaction between stages, despite its simplicity and is used for arbitrary number of module of stages. Therefore, it applicable for higher than 1KV input applications.

On the other hand, the electrical equivalent circuit is useful for analysis. The equivalent electrical circuits are presented in this paper for all stages separately and integrated. The averaged differential equations are simulated in SIMULINK/MATLAB software as the simulation results verified the proposed model.

In the second section of this paper, the basic modeling of the investigated transformer is described. The third section, addresses the generalization of the model. The results of simulations and related studies are examined in section four and a conclusion is reached at the end.

2-Basic Modeling

Various SST architectures have been described in [27-29]. The SST structure is illustrated in Figure 2. The names of the elements and variables are displayed in this figure. The SST under investigation is made up of three stages: ac/dc, dc/dc and dc/ac and the modulation methods including PWM, SPWM and Phase Shift Modulation (PSM) have been used, respectively. It can transfer power in both directions and perform tasks such as power factor correction, voltage regulation on ac and dc networks and so on.

a. The averaging theory

The averaging method is extensively used for modelling, simulation, and control of multilevel converters that are similar to the converters explored in this article. The averaging function is defined as:

$$\langle x(t)\rangle_{T_S} = \frac{1}{T_S}\int_0^{T_S} x(t)dt \qquad (1)$$

The period of $x(t)$ is represented by T_s in equation (1). In power electronic converters, the averaging operator $\langle . \rangle_{T_S}$ can be used to transform switched system equations to normal equations. Throughout the rest of the article, the averaged variables are used everywhere and the averaging operator's symbol is not written for the sake of brevity.

Each SST stage typically has a number of converters connected in series or parallel. The basic structure of the transformer is shown in Figure 3. On the other hand, modeling is done in this section for one converter in each stage that is illustrated in Figure 3. Modeling is done with the variables introduced in this figure. The following hypotheses are taken into account when modeling: power electronic devices are lossless, the switches are turned on and off instantly and passive devices operate in their linear area and the saturation phenomenon is ignored.

b. The ac/dc stage

The input stage converter takes an ac medium voltage input and outputs a dc low voltage. Cascaded H-bridge (CHB) converters are considered for the ac/dc stage in this paper. CHB is the most suited structure for the ac/dc stage in SST because of its advantages. The PWM approach is used at this stage. Figure 4 depicts the input stage, its variables and operating modes.

The conduction status of the switches Q1 to Q4 is determined by the output voltage of the H-bridge and the time variations of the duty cycle d_{CHB} over a period of the input voltage, as shown in Figure 5. The positive and negative states of d_{CHB} in this diagram correspond to the positive and negative voltage states. V_{CHB} also defines the H-bridge output voltage before it is applied to the capacitor. Based on the four operating modes of the circuit and the average of the circuit relations, the differential equations of the state space of this stage are derived as (2) and (3).

$$L_{CHB}\frac{dI_{L_{CHB}}}{dt} = V_{ac} - V_{CHB}d_{CHB} \qquad (2)$$

$$C_{CHB}\frac{dV_{CHB}}{dt}=I_{L_{CHB}}d_{CHB}-I_{DABi} \qquad (3)$$

The equivalent circuit of the H-bridge with the input inductor is obtained using these equations, as shown in Figure 6.(a)

c. The dc/dc stage

The dc/dc stage of SST is shown in Figure 3. For this stage, a single-phase dual active bridge (DAB) converter is used. Because the single-phase DAB is highly efficient and has a low number of passive elements, it can be used as a dc/dc converter in SST [8]. For this converter, the PSM is being considered. PSM is simple to implement and its low rms current results in lower rated power semiconductors [8]. Figure 6.(b) represents a simplified model of this stage. The transformer's input and output voltages are shown in Figure 7. The turn-on time of the semiconductor switch is assumed to be $\left[0\ ,\frac{T_s}{2}d_{DAB}\right]$ in this figure. The dc/dc converter is shown in Figure 8.(a), the equivalent circuit of the DAB in the time interval $\left[0\ ,\frac{T_s}{2}d_{DAB}\right]$ is shown in Figure 8.(b), and in the time interval $\left[\frac{T_s}{2}d_{DAB}\ ,\frac{T_s}{2}\right]$ is shown in Figure 8.(c).

In equation (4), the average half-cycle inductor voltage is shown, as well as its simplification equation (5).

$$\begin{aligned}\frac{L_{DAB}}{{n_{Tr}}^2}\frac{dI_{L_{DAB}}}{dt}=&\frac{V_{DABi}}{n_{Tr}}d_{DAB}+\frac{V_{DABi}}{n_{Tr}}\left(1-d_{DAB}\right)\\&-\left(-V_{DABo}\right)d_{DAB}-V_{DABo}\left(1-d_{DAB}\right)\end{aligned} \qquad (4)$$

$$\frac{L_{DAB}}{{n_{Tr}}^2}\frac{dI_{L_{DAB}}}{dt}=\frac{V_{DABi}}{n_{Tr}}+V_{DABo}\left(2d_{DAB}-1\right) \qquad (5)$$

Similarly, the average value of the capacitor current on the half cycle presented in equation (6) and simplified in equation (7).

$$\begin{aligned}C_{DABo}\frac{dV_{DABo}}{dt}=&\left(-I_{L_{DAB}}-\frac{V_{DABo}}{R}\right)d_{DAB}\\&+\left(I_{L_{DAB}}-\frac{V_{DABo}}{R}\right)\left(1-d_{DAB}\right)\end{aligned} \qquad (6)$$

$$C_{DABo}\frac{dV_{DABo}}{dt}=I_{L_{DAB}}\left(1-2d_{DAB}\right)-\frac{V_{DABo}}{R} \qquad (7)$$

The voltage and current waveforms of the L_{DAB} transmitted to the secondary of the transformer are shown in Figure 9.(a).

According to this figure, the average value of $V_{L_{DAB}}$ in the positive half cycle is equal to:

$$V_{L_{DAB}} = \frac{L_{DAB}}{{n_{Tr}}^2}\frac{dI_{L_{DAB}}}{dt} \cong \frac{L_{DAB}}{{n_{Tr}}^2}\frac{2I_{L_{DAB},max}}{\frac{T_S}{2}} = \frac{4L_{DAB}}{{n_{Tr}}^2 T_S} I_{L_{DAB},max} \quad (8)$$

Therefore using equation (5) and (8):

$$\frac{V_{DABi}}{n_{Tr}} + V_{DABo}\left(2d_{DAB} - 1\right) = \frac{4L_{DAB}}{{n_{Tr}}^2 T_S} I_{L_{DAB},max} \quad (9)$$

Figure 9.(b) shows the inductor current after crossing the H-bridge on the transformer's secondary side. The average inductor current in a half-switching cycle is $\frac{1}{2} I_{L_{DAB},max}$. As a result of the above, equation (10) yields the current after crossing the H-bridge on the secondary side of the transformer:

$$I_{DABo} = \frac{1}{2}\frac{\frac{V_{DABi}}{n_{Tr}} + V_{DABo}\left(2d_{DAB} - 1\right)}{\frac{4L_{DAB}}{{n_{Tr}}^2 T_S}} \quad (10)$$

The average input current of the DAB can be calculated using equation (11).

$$I_{DABi} = \frac{I_{DABo}}{n_{Tr}} = \frac{\frac{V_{DABi}}{n_{Tr}} + V_{DABo}\left(2d_{DAB} - 1\right)}{\frac{8L_{DAB}}{n_{Tr} T_S}} \quad (11)$$

According to equation (11) and the average model is shown in Figure 10, the averaged equivalent model of dc/dc stage is presented. Therefore, equation (12) is obtained for capacitor current using the average model that shown in Figure 10.

$$C_{DABo}\frac{d}{dt}V_{DABo} = \frac{\frac{V_{DABi}}{n_{Tr}} + V_{DABo}\left(2d_{DAB} - 1\right)}{\frac{8L_{DAB}}{{n_{Tr}}^2 T_S}} - I_{in-3P4L} \quad (12)$$

d. The dc/ac Stage

A two-level voltage source inverter is more practical than a multilevel inverter for this stage because it operates at low voltage. The causes for this are lower prices, simpler circuits, and the adoption of more widely accepted technology. The best structure for this stage is a three-phase four-leg converter, with SPWM as the control technique [8]. It describes and explains model extraction in depth.

Figure 11 shows the averaged equivalent circuit of the inverter stage based on the relations expressed in [8] and the naming of the circuit variables. In this figure, the parameters with "*" are related to the output filter and the parameters without "*" are related to the load. Also, considering the assumption that the model has no losses, the input current to this stage is equal to:

$$I_{in-3P4L} = \frac{\frac{3}{2}V_d i_d + \frac{3}{2}V_q i_q + 3V_0 i_0}{V_{DABo}} \qquad (13)$$

The equation (13) and equivalent circuit of Figure 11 is presented for first time in this article.

e. Integrating the stages

The integrated converter relationships are presented as nonlinear differential equations in the following.

$$\dot{x} = f\left(x, u_c, u_{uc}\right) \qquad (14)$$

Equation (14) consists of 9 state variables and equations, which are derived by combining the relations provided for each stage. In equation (14), the state variable is as follows:

$$x = \left[I_{L_{CHB}} V_{CHB} V_{DABo} V_d V_q V_0 i_d^* i_q^* i_0^*\right]^T \qquad (15)$$

Controlled and uncontrolled (perturbation) inputs are equal to:

$$\begin{aligned} u_c &= \left[d_{CHB}\, d_{DAB}\, d_d\, d_q\, d_0\right]^T \\ u_{uc} &= \left[v_{ac}\, i_d\, i_q\, i_0\right]^T \end{aligned} \qquad (16)$$

Finally, the description of the nonlinear equations of the SST model in the state space can be shown as follows.

$$L_{CHB}\frac{dI_{L_{CHB}}}{dt} = V_{ac} - V_{CHB} d_{CHB} \qquad (17)$$

$$C_{CHB}\frac{dV_{CHB}}{dt}=I_{L_{CHB}}d_{CHB}-\frac{T_S V_{CHB}}{8L_{DAB}}-\frac{V_{DABo}\,n_{Tr}T_S\left(2d_{DAB}-1\right)}{8L_{DAB}}$$

$$C_{DABo}\frac{d}{dt}V_{DABo}=\frac{n_{Tr}T_S V_{CHB}}{8L_{DAB}}+\frac{n_{Tr}{}^2T_S V_{DABo}\left(2d_{DAB}-1\right)}{8L_{DAB}}-\frac{3V_d i_d+3V_q i_q+6V_0 i_0}{2V_{DABo}}$$

$$C_{3P4L}\frac{d}{dt}V_d=i_d^*-i_d+\omega C_{3P4L}V_q$$

$$C_{3P4L}\frac{d}{dt}V_q=i_q^*-i_q-\omega C_{3P4L}V_d$$

$$C_{3P4L}\frac{d}{dt}V_0=i_0^*-i_0$$

$$L_{3P4L}\frac{d}{dt}i_d^*=V_{DABo}d_d-V_d+\omega L_{3P4L}i_q^*$$

$$L_{3P4L}\frac{d}{dt}i_q^*=V_{DABo}d_q-V_q-\omega L_{3P4L}i_d^*$$

$$\left(L_{3P4L}+3L_n\right)\frac{d}{dt}i_0^*=V_{DABo}d_0-V_0$$

3- Generalization of SST model

The modeling of different stages of a SST was presented in the second section, with one converter in each stage. With an arbitrary number of converters at the input and dc/dc stages, the model of the ac/dc and dc/dc stages is generalized and the complete model of the SST is obtained.

a. Generalization of the ac/dc stage

The input stages must be cascaded due to the extremely high voltage applied to this stage. In this case, the input voltage level is *n* times higher than in the basic modeling section. The following relations are considered:

$$C_{CHB,1} = C_{CHB,2} = \ldots = C_{CHB,3n} = C_{CHB}^{*} = C_{CHB} \quad (18)$$

$$L_{CHB}^{*} = L_{CHB} \quad (19)$$

The differential equations of the generalized model are obtained in the same way as the second section for one phase:

$$\begin{aligned} C_{CHB}\frac{d}{dt}V_{CHB,1} &= I_{L_{CHB}^{*}} \times d_{CHB,1} - I_{DABi,1} \\ C_{CHB}\frac{d}{dt}V_{CHB,n} &= I_{L_{CHB}^{*}} \times d_{CHB,n} - I_{DABi,n} \end{aligned} \quad (20)$$

$$L_{CHB}^{*}\frac{d}{dt}I_{L_{CHB}^{*}} = V_{ac} - \begin{pmatrix} V_{CHB,1}d_{CHB,1} \\ +V_{CHB,2}d_{CHB,2} \\ +\ldots+V_{CHB,n}d_{CHB,n} \end{pmatrix} \quad (21)$$

where. $d_{CHB,i} = d_{CHB}$,$i = 1,2,\ldots,n$

The equivalent circuit is shown in Figure 12 for one input phase. This section is presented for one phase and two other phases equations are similar.

b. Generalization of the dc/dc stage model

According to the model described in the third section, the secondary side current of the transformer after rectification has the following relation with regarding three phase input:

$$I_{DABo,i} = \frac{\frac{V_{DABi,i}}{n_{Tr}} + V_{DABo,i}\left(2d_{DAB,i} - 1\right)}{\frac{8L_{DAB,i}}{n_{Tr}^{2}T_{S}}} \quad (22)$$

$$L_{DAB,i} = L_{DAB} \quad (23)$$

in which: $d_{DAB,i} = d_{DAB}$, $V_{DABi,i} = V_{DABi}$, $V_{DABo,i} = V_{DABo}$ and $i = 1,2,\ldots,n,n+1,\ldots,2n$, $2n+1,\ldots,3n$.

The differential equation for the capacitor voltage will be as follows, according to the model shown in Figure 13:

$$\sum_{i=1}^{3n} I_{DABo,i} - I_{in-3P4L} = C_{DABo} \frac{d}{dt} V_{DABo} \qquad (24)$$

c. Integration of the stages

For the SST depicted in Figure 2, a generalized averaged model is obtained which is shown in Figure 14. The integrated equations are found based on equations (20)-(21), (22)-(24) and (12)-(17) as following equations in which x becomes for *a*, *b* and *c* (regarded to three phase input) and k represents *1,2,…,3n*.

$$L_{CHB}{}^{*} \frac{d}{dt} I_{L^{*}_{CHB},x} = V_{ac,x} - \sum_{i=1}^{3n} V_{CHB,i,x} d_{CHB,i,x}$$

$$C_{CHB} \frac{d}{dt} V_{CHB,k} = I_{L_{CHB}{}^{*}} \times d_{CHB,k} - \frac{T_S V_{CHB,k}}{8L_{DAB}} - \frac{V_{DABo} n_{Tr} T_S \left(2d_{CHB,k} - 1\right)}{8L_{DAB}}$$

$$C_{DABo} \frac{d}{dt} V_{DABo} = \sum_{i=1}^{3n} \frac{n_{Tr} T_S V_{CHB,i}}{8L_{DAB}} + \frac{n_{Tr}{}^{2} T_S V_{DABo} \left(2d_{DAB,i} - 1\right)}{8L_{DAB}} - \frac{3V_d i_d + 3V_q i_q + 6V_0 i_0}{2V_{DABo}} \qquad (25)$$

$$C_{3P4L} \frac{d}{dt} V_d = i_d^{*} - i_d + \omega C_{3P4L} V_q$$

$$C_{3P4L} \frac{d}{dt} V_q = i_q^{*} - i_q - \omega C_{3P4L} V_d$$

$$C_{3P4L} \frac{d}{dt} V_0 = i_0^{*} - i_0$$

$$L_{3P4L} \frac{d}{dt} i_d^{*} = V_{DABo} d_d - V_d + \omega L_{3P4L} i_q^{*}$$

$$L_{3P4L}\frac{d}{dt}i_q^* = V_{DABo}d_q - V_q - \omega L_{3P4L}i_d^*$$

$$\left(L_{3P4L} + 3L_n\right)\frac{d}{dt}i_0^* = V_{DABo}d_0 - V_0$$

4- Simulation and discussion

A 25KW and 20KV/400V SST is investigated for simulation. Because of 20 KV input voltage, the 19 modules are cascaded in input stage. The closed-loop control structure has been built for all three stages in addition to the recommended modelling. The differential equations derived from generalized modeling are implemented in the MATLAB/SIMULINK environment. The simulation results for each SST stage are reported in this section. Table 1 lists the SST simulation parameters.

First of all, for better comparison of the averaged and non-averaged models, the simulation of input rectifier (cascade H-bridge topology) is shown in Figure 15. The start-up output voltage and zoomed waveform are shown which verify the averaged approximation models.

Figures 16 illustrate the steady state operation signals of SST stages. The current and voltage of the SST input are shown in Figure 16.(a). For better display, the current has been magnified 1000 times in this figure. According to this diagram, the ac/dc stage's input voltage and current are in phase ($\mathrm{Cos}\Phi = 1$), and the medium voltage source does not generate reactive power. Figure 16.(b) exhibits the output voltage of the rectifier stage converter. The final value is extremely close to the value computed for each converter at dc/dc stage input voltage, i.e., 914V, as can be seen.

Figure 16.(c) depicts the steady state output voltage of the dc/dc stage which has a steady-state value of around 404V. Figure 16.(d) illustrates the three-phase output voltage of SST, which has the same characteristics as end-user required.

The transient response of SST at start-up and load variations are shown in Figures 17-20. The input voltage and current of SST at start-up are illustrated in Figure 17. The transient reaction is damped in approximately 0.2 seconds, and the converter is switched to the steady state mode. Figure 18 depicts the output voltage of the CHB stage for each converter. The overshoot and rising time are good due to the good selection of PID controller coefficients. The transient response of SST's output voltage and input current for load fluctuations are shown in Figures 19 and 20. The 10% load variation that happens at t=1s is compensated by closed loop controllers.

5- Conclusion

For three stages of ac/dc, dc/dc and dc/ac an integrated modeling of a bidirectional SST using averaging theory was being presented. The obtained models of three stages are interact to each other, resulting in a complete dynamic model for describing transformer behavior. The presented model is an extension of the results of other studies and the mathematical model and equivalent circuits was presented for extended models. The extracted models can be used in power system simulations and distribution networks, including SSTs, as well as analysis and design of transformer behavior in renewable energy and electrical transportation applications, due to their high accuracy and simplicity. Future researches will focus on dynamic simulations of SSTs in power systems and model development with loss elements of converters.

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In 2009, he joined MUSROC, Mashhad, Iran, where he works in different technical parts of signaling, electrical, communicational, engineering departments up to 2023. His research interests include the renewables energies, reliability, protection systems and electrical vehicles.

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Table 1. The simulation's parameter values

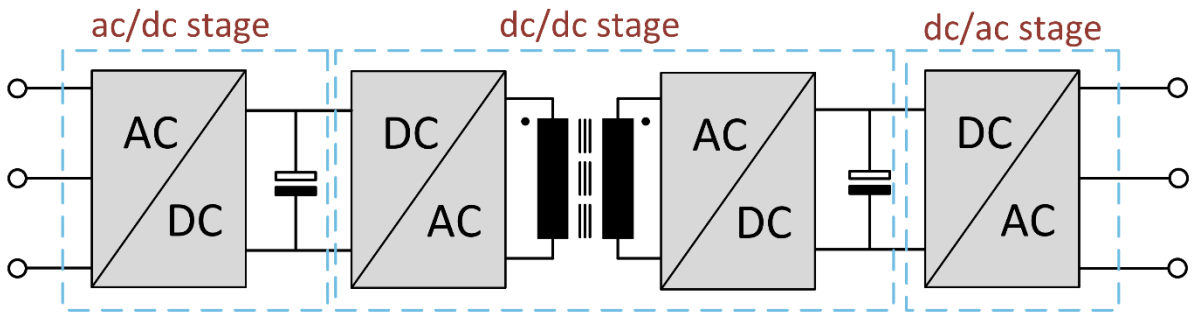

Figure 1

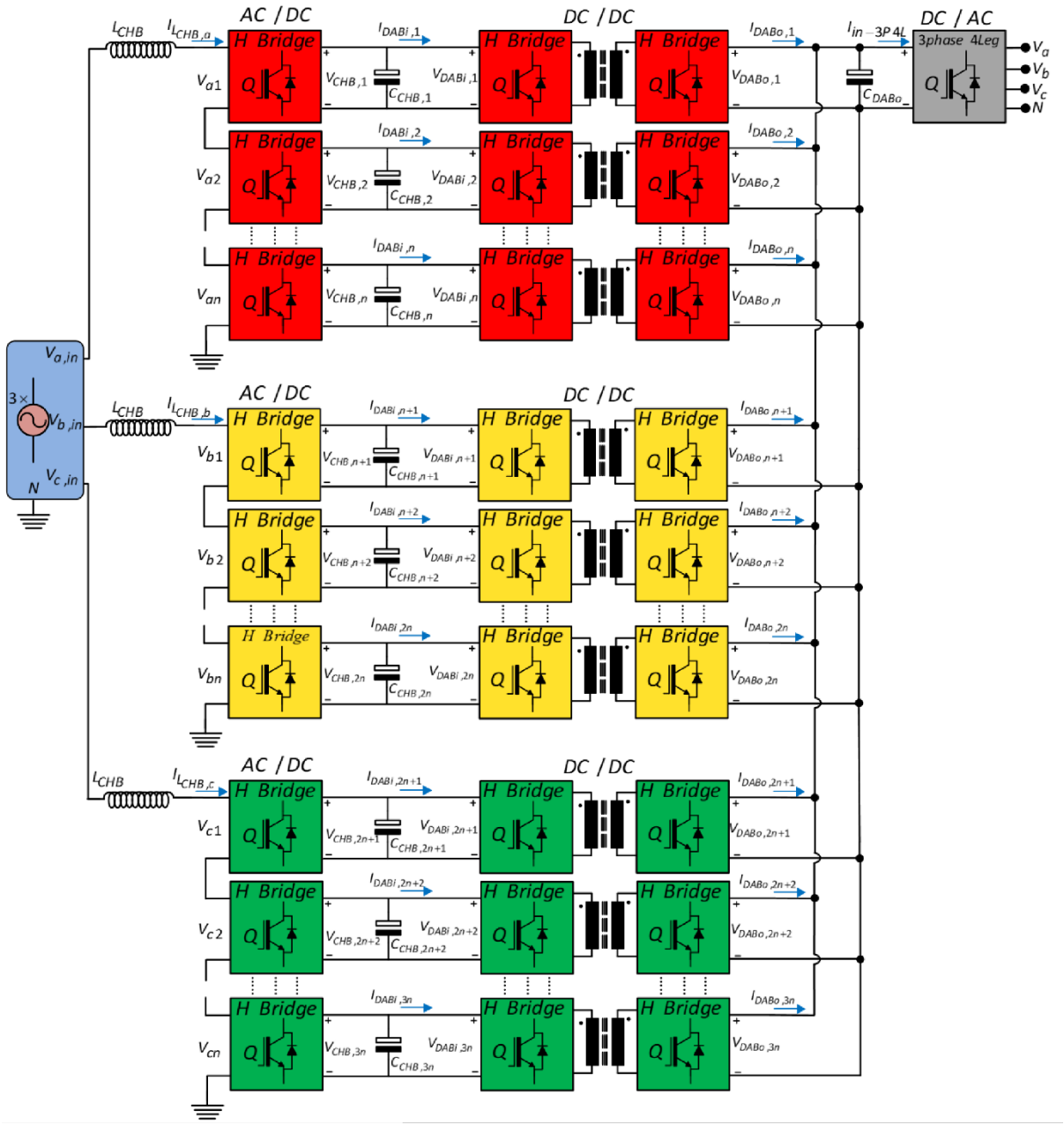

Figure 2

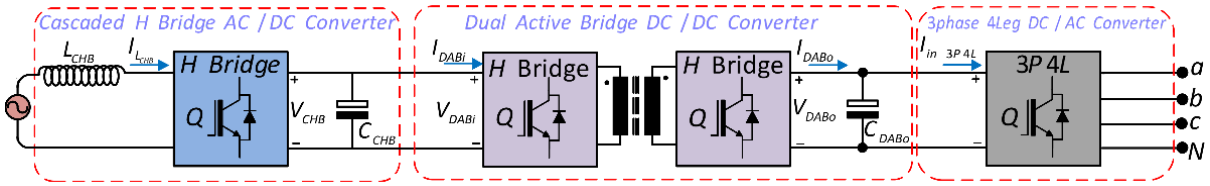

Figure 3

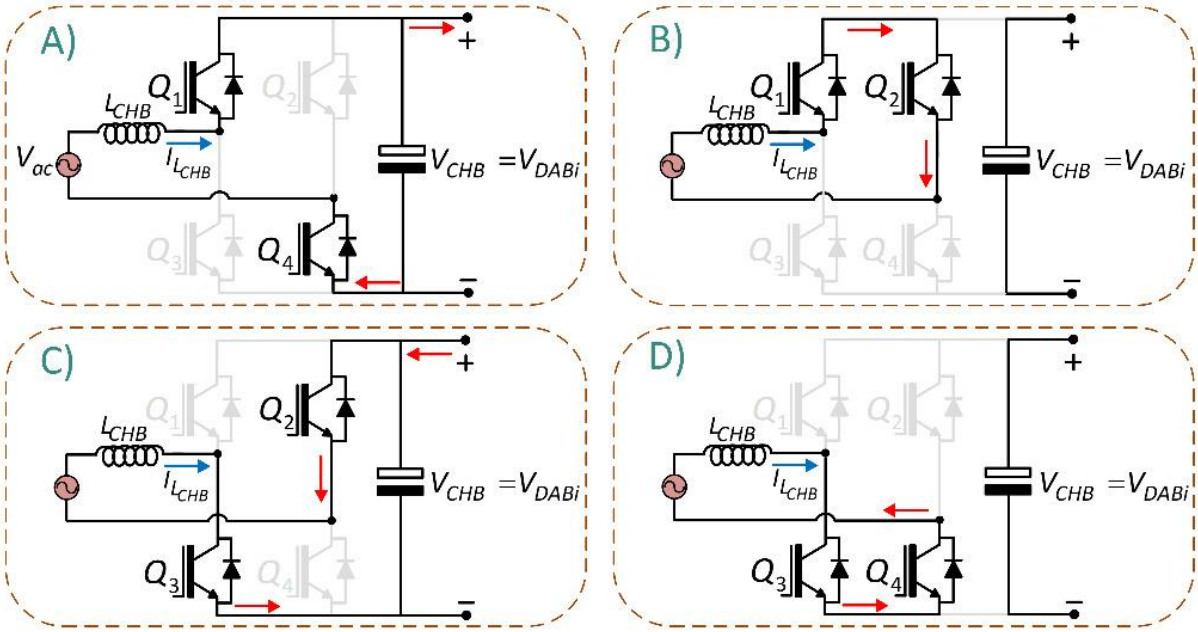

Figure 4

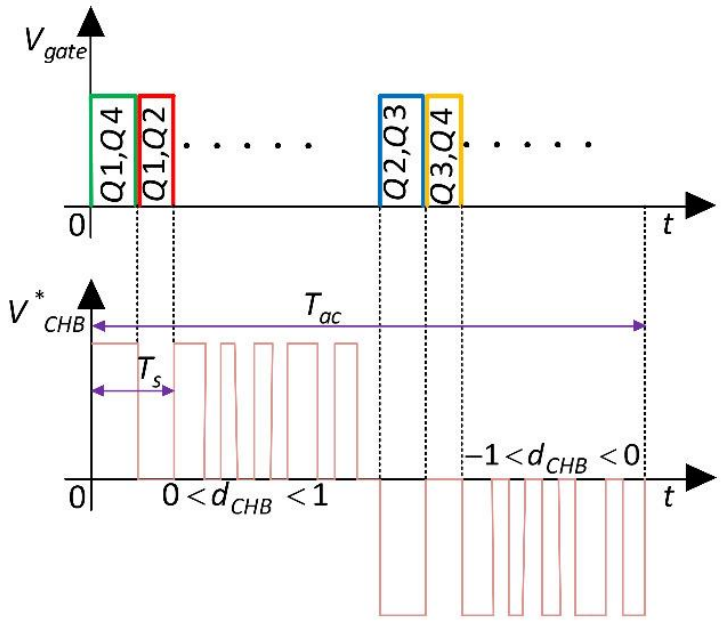

Figure 5

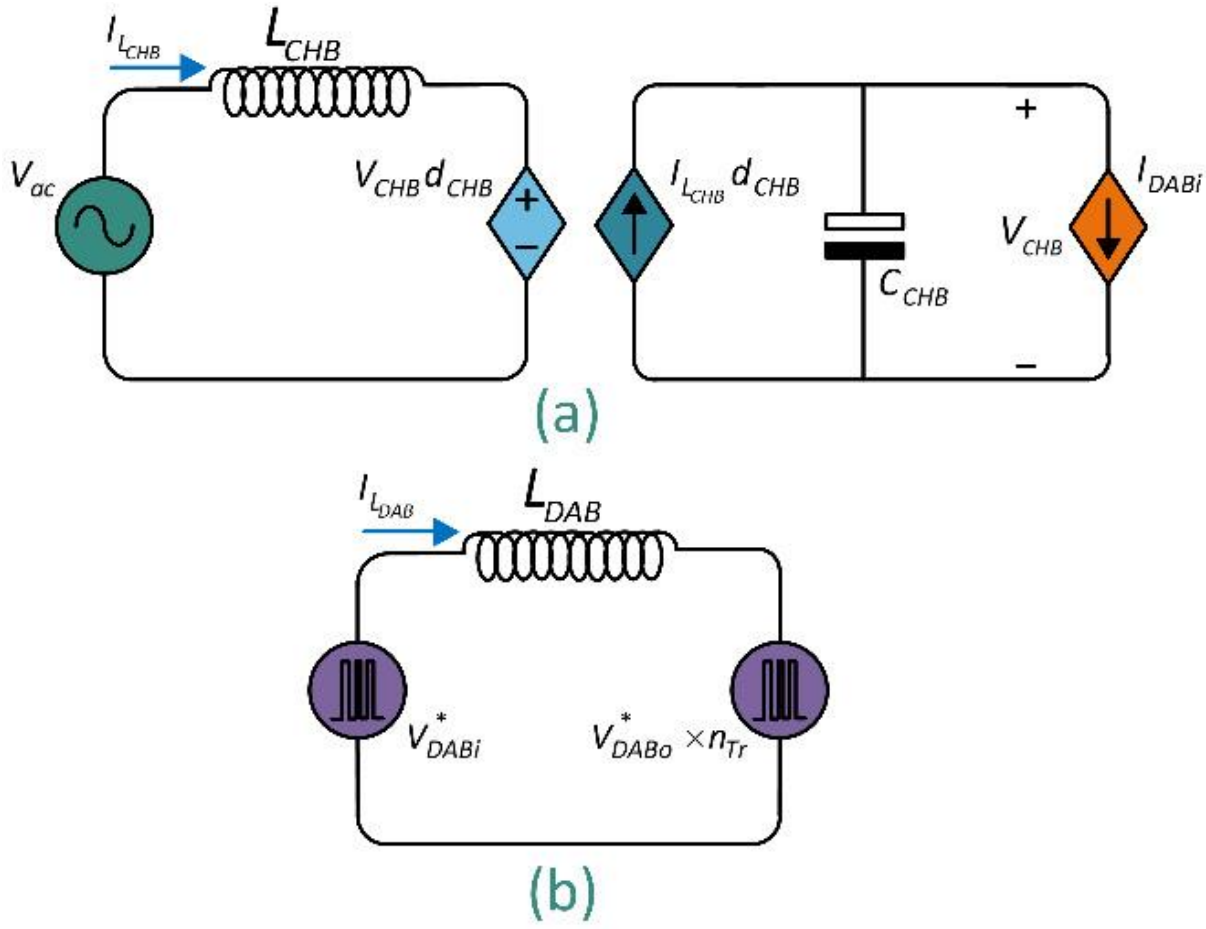

Figure 6

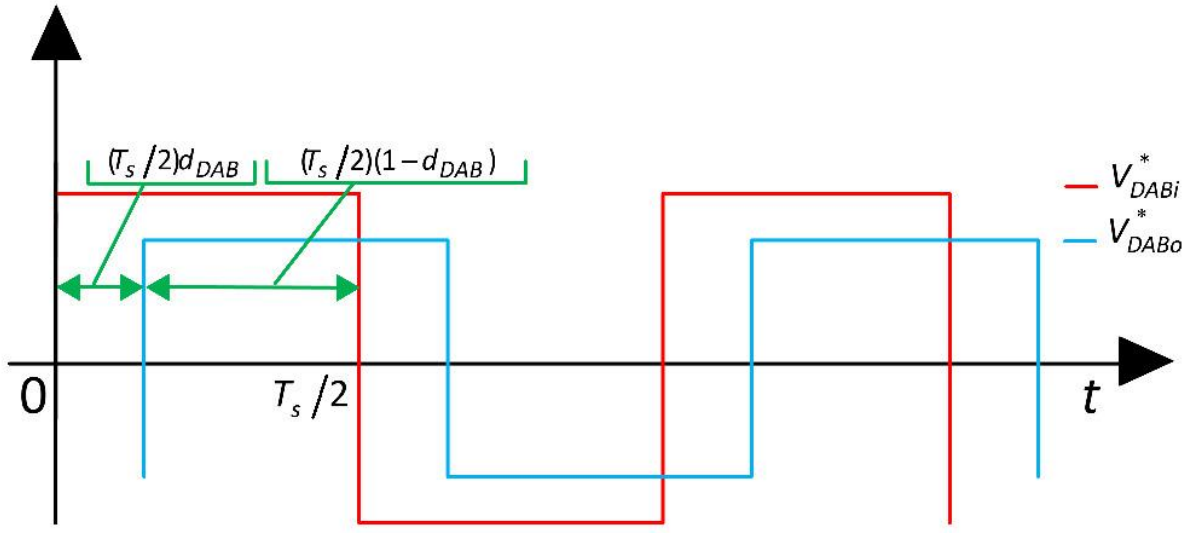

Figure 7

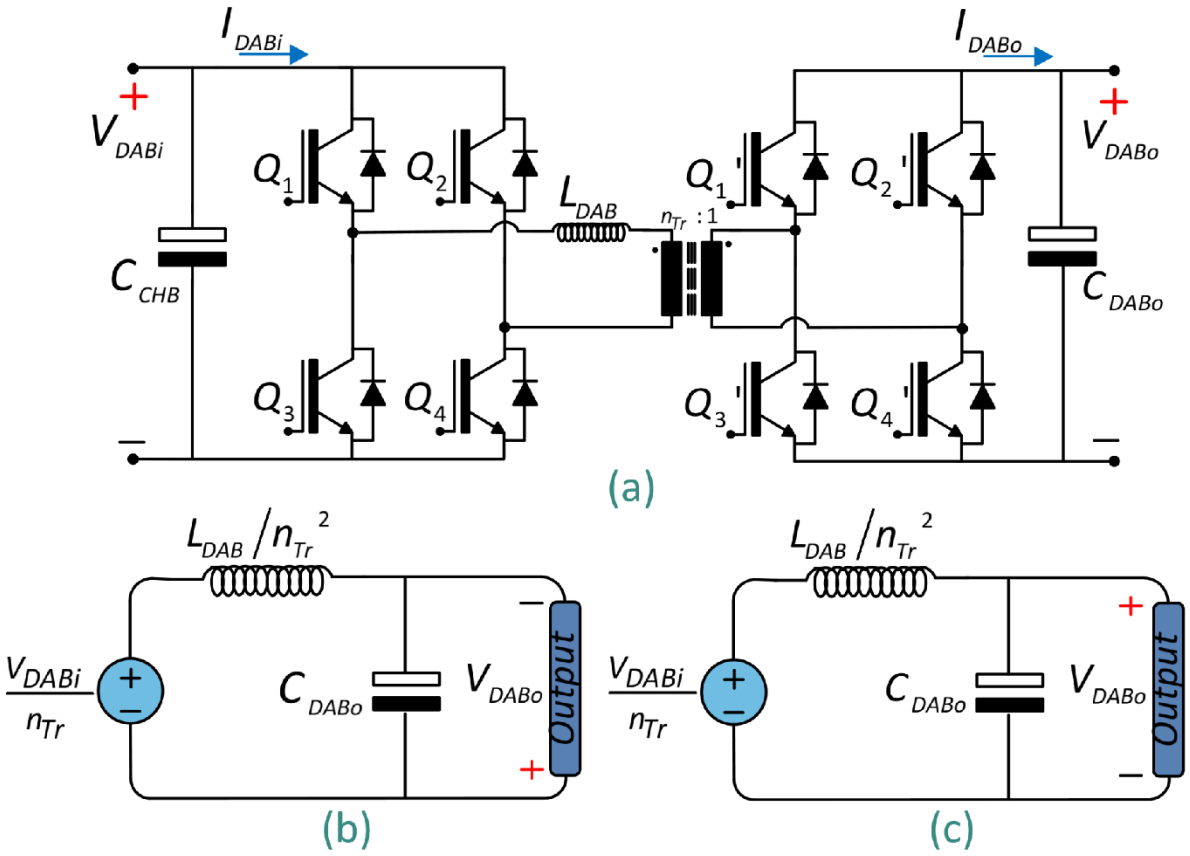
I DABi
V DABi
Q1
Q2
Q3
Q4
C CHB
L DAB
nTr :1
Q1'
Q2'
Q3'
Q4'
I DABo
V DABo
C DABo
(a)
L DAB /nTr 2
V DABi
nTr
C DABo
V DABo
Output
(b)
L DAB /nTr 2
V DABi
nTr
C DABo
V DABo
Output
(c)

Figure 8

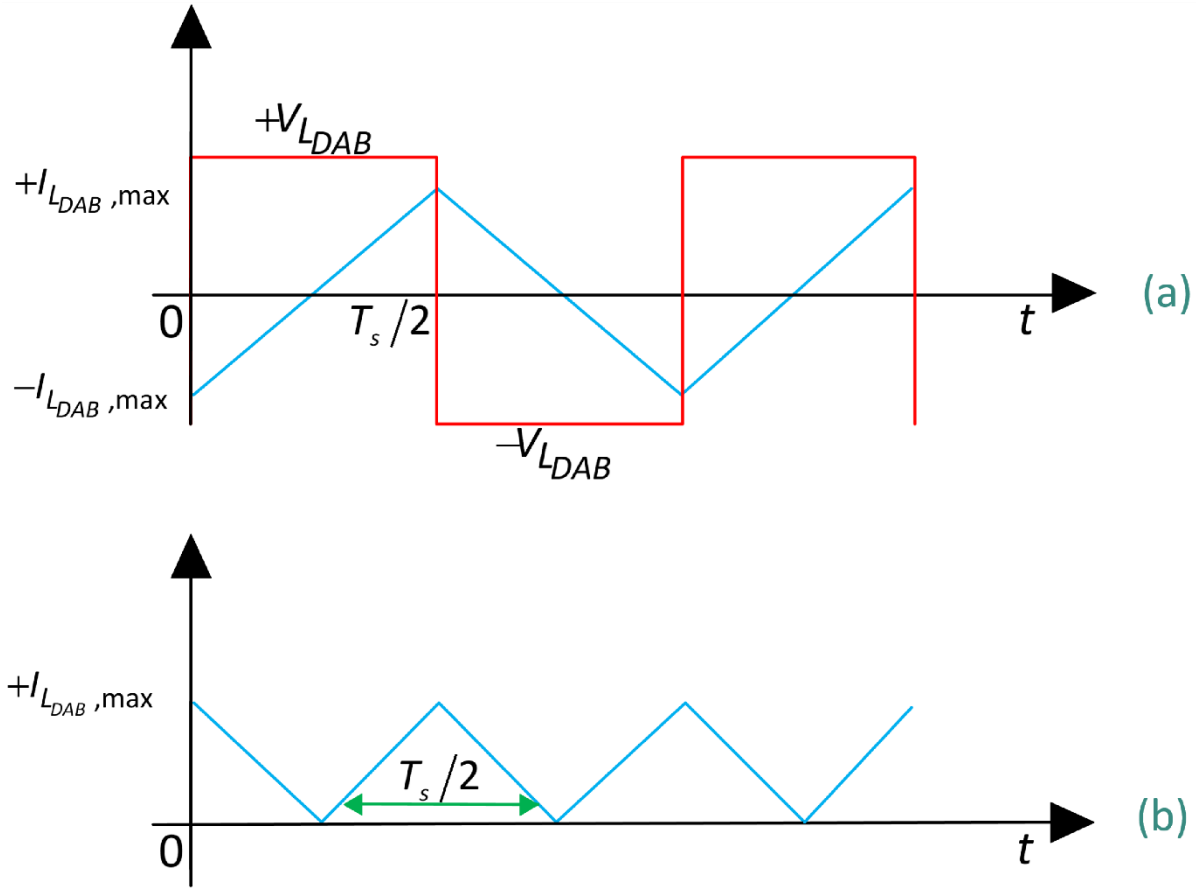

Figure 9

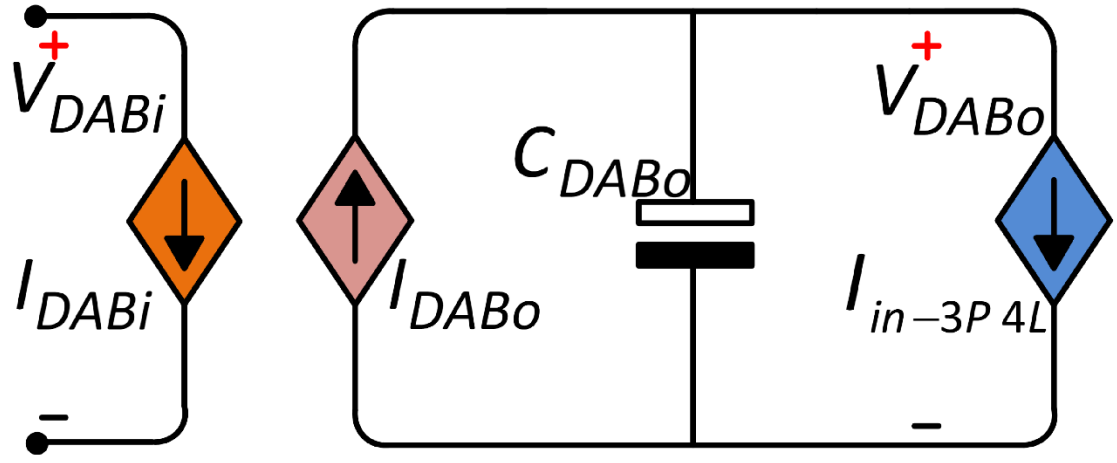

Figure 10

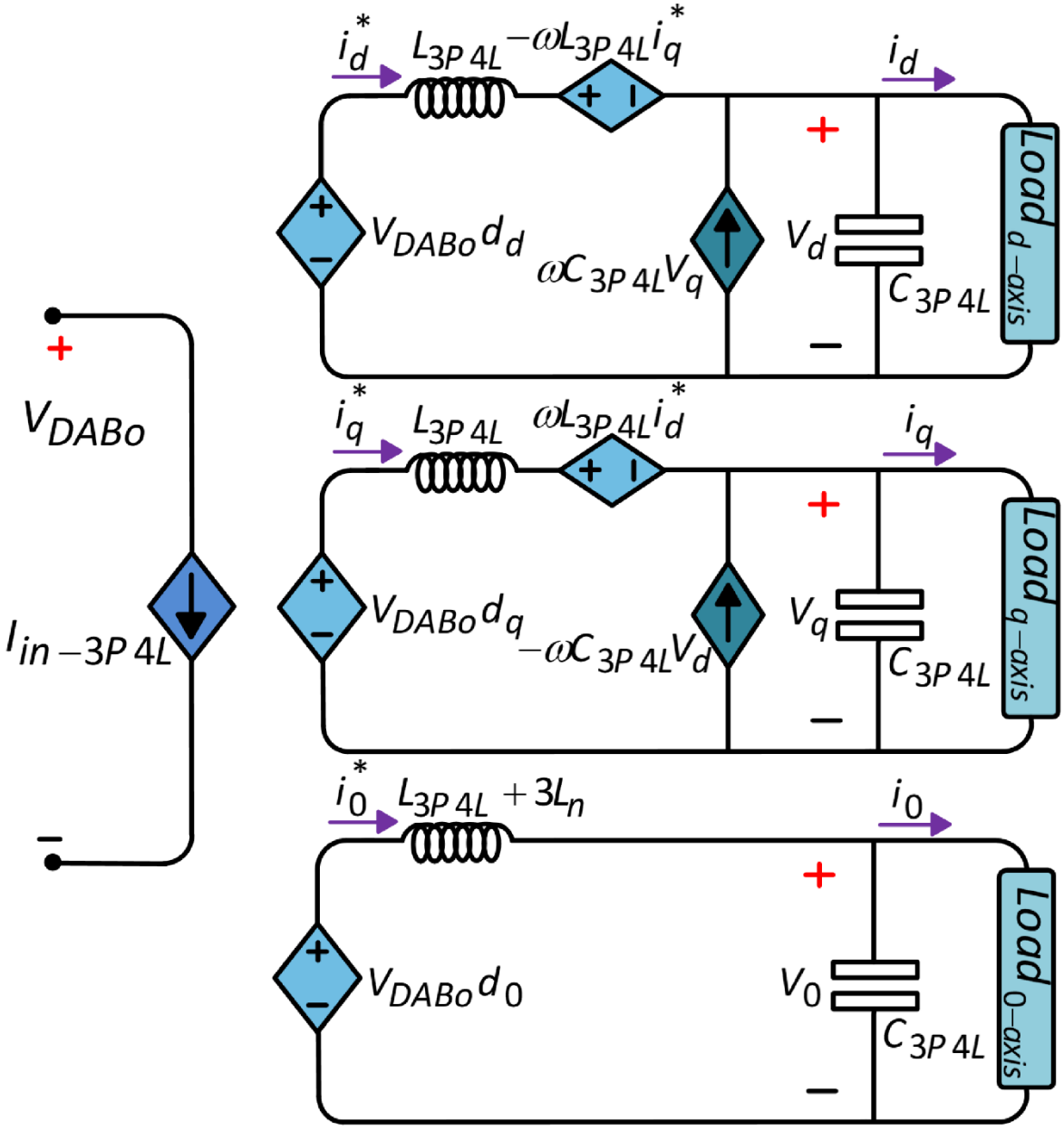
i_d^*
$L_{3P\,4L}$
$-\omega L_{3P\,4L} i_q^*$
i_d
$V_{DABo} d_d$
$\omega C_{3P\,4L} V_q$
V_d
$C_{3P\,4L}$
$Load_{d-axis}$
V_{DABo}
$I_{in-3P\,4L}$
i_q^*
$L_{3P\,4L}$
$\omega L_{3P\,4L} i_d^*$
i_q
$V_{DABo} d_q$
$-\omega C_{3P\,4L} V_d$
V_q
$C_{3P\,4L}$
$Load_{q-axis}$
i_0^*
$L_{3P\,4L} + 3L_n$
i_0
$V_{DABo} d_0$
V_0
$C_{3P\,4L}$
$Load_{0-axis}$

Figure 11

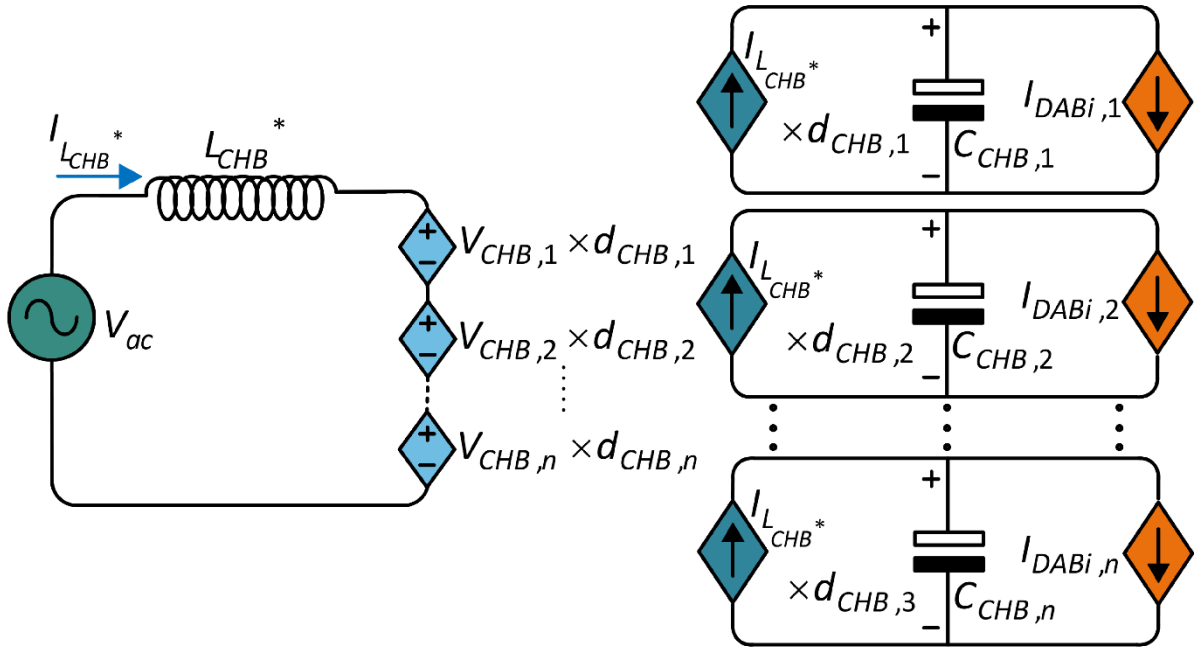

Figure 12

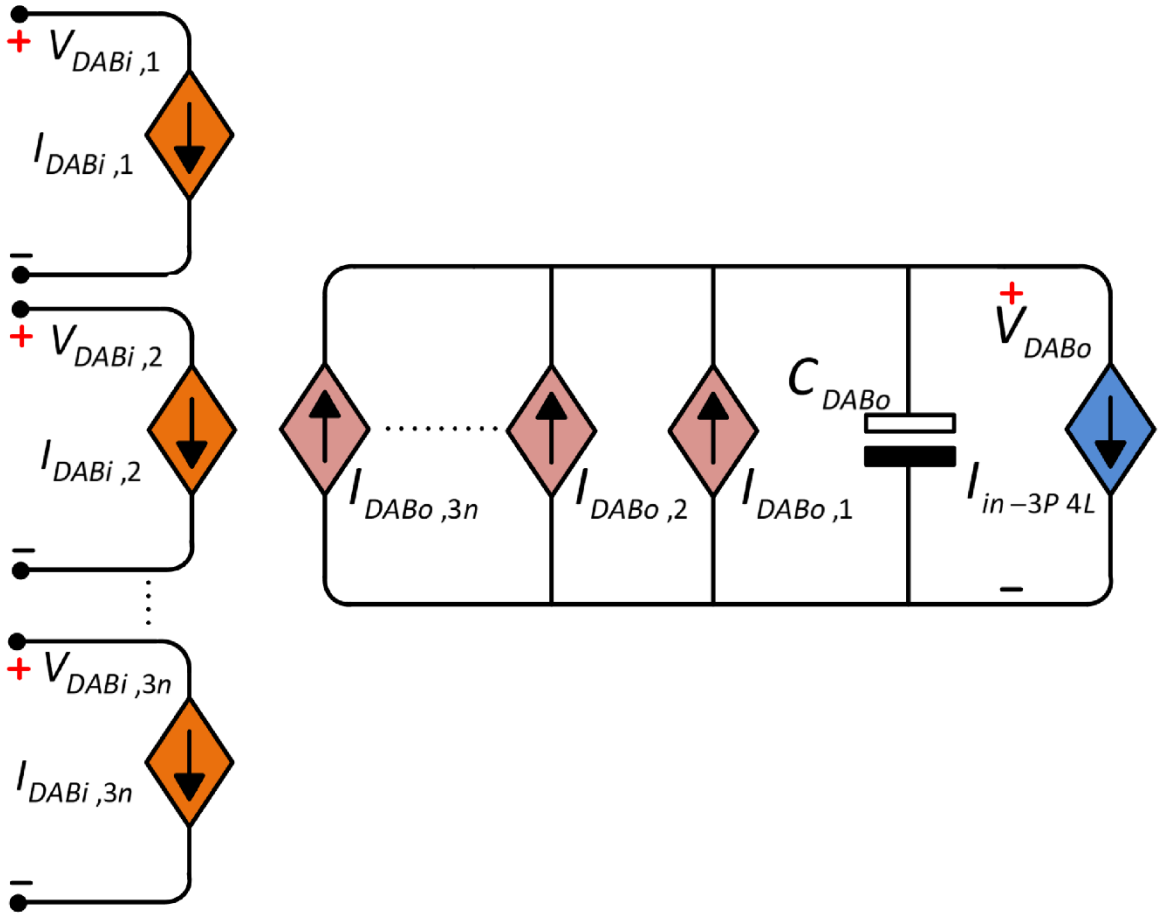

Figure 13

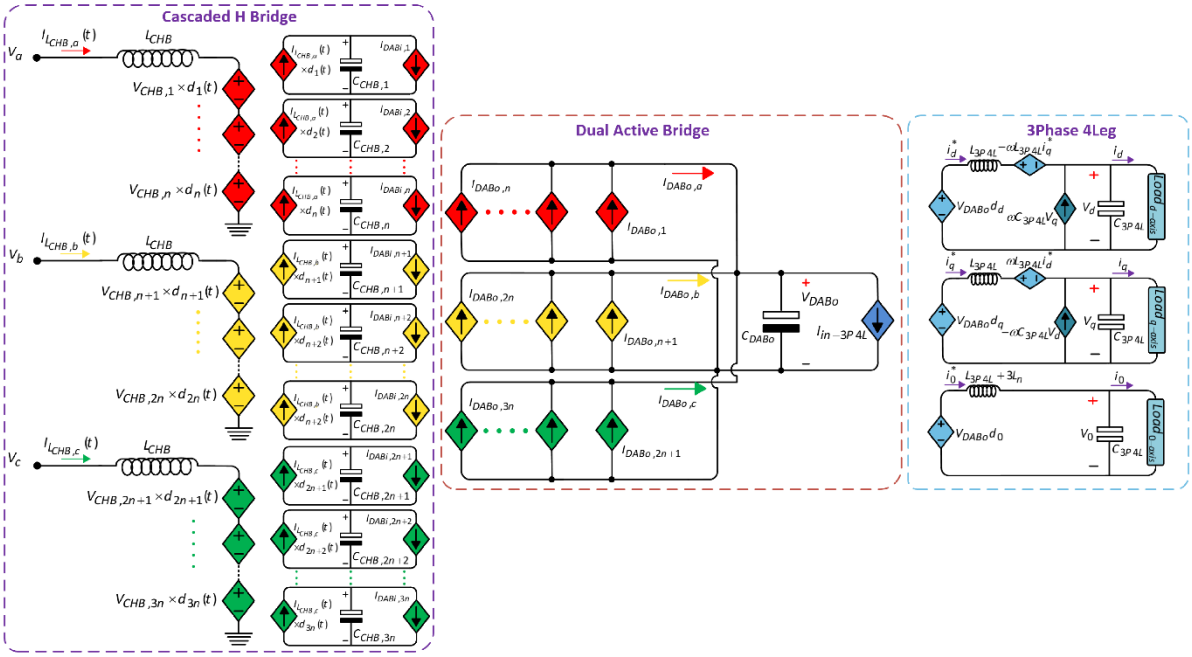

Figure 14

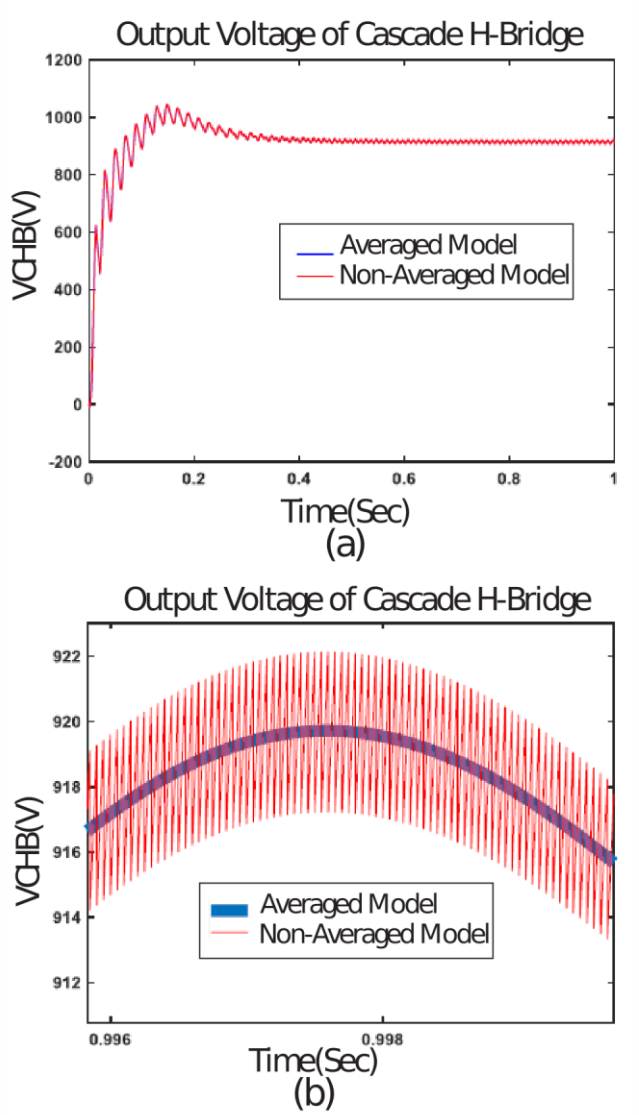
Output Voltage of Cascade H-Bridge
VCHB(V)
Time(Sec)
Averaged Model
Non-Averaged Model
(a)
Output Voltage of Cascade H-Bridge
VCHB(V)
Time(Sec)
Averaged Model
Non-Averaged Model
(b)

Figure 15

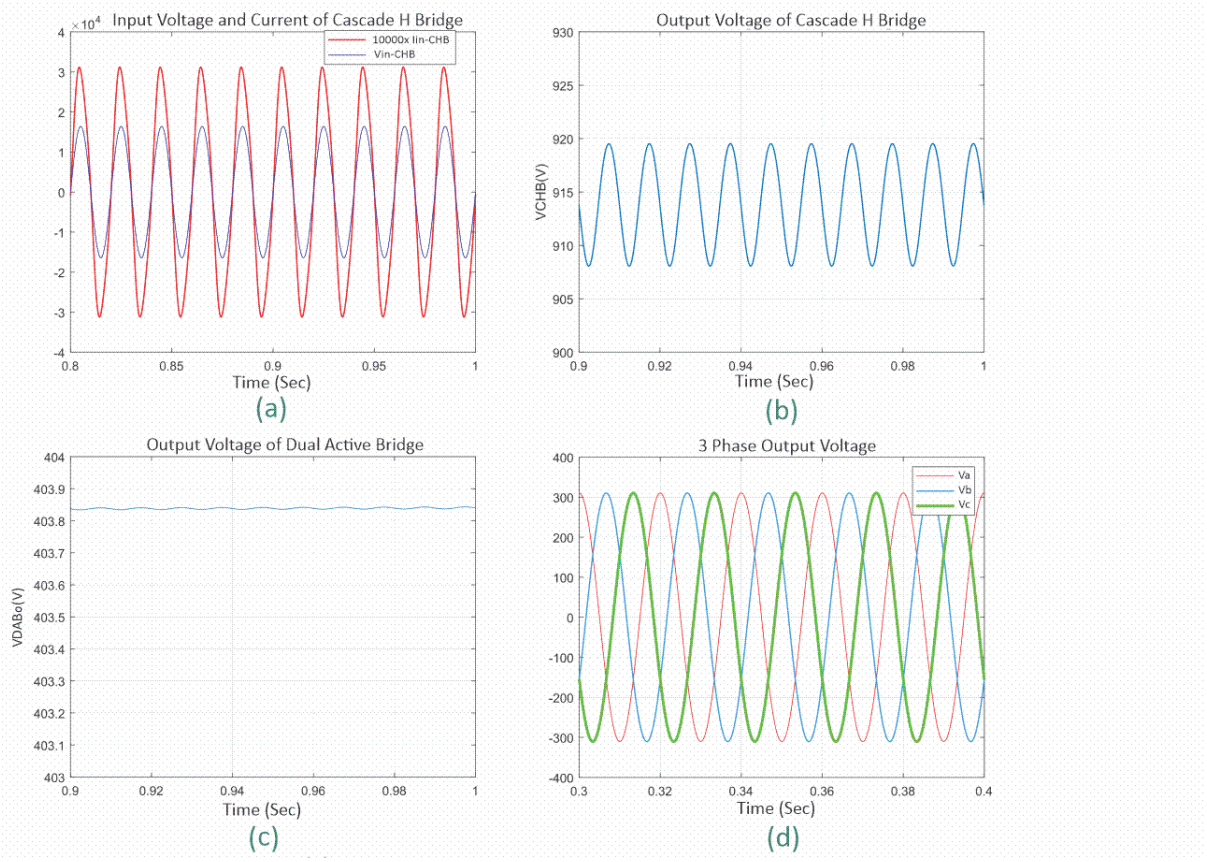

Figure 16

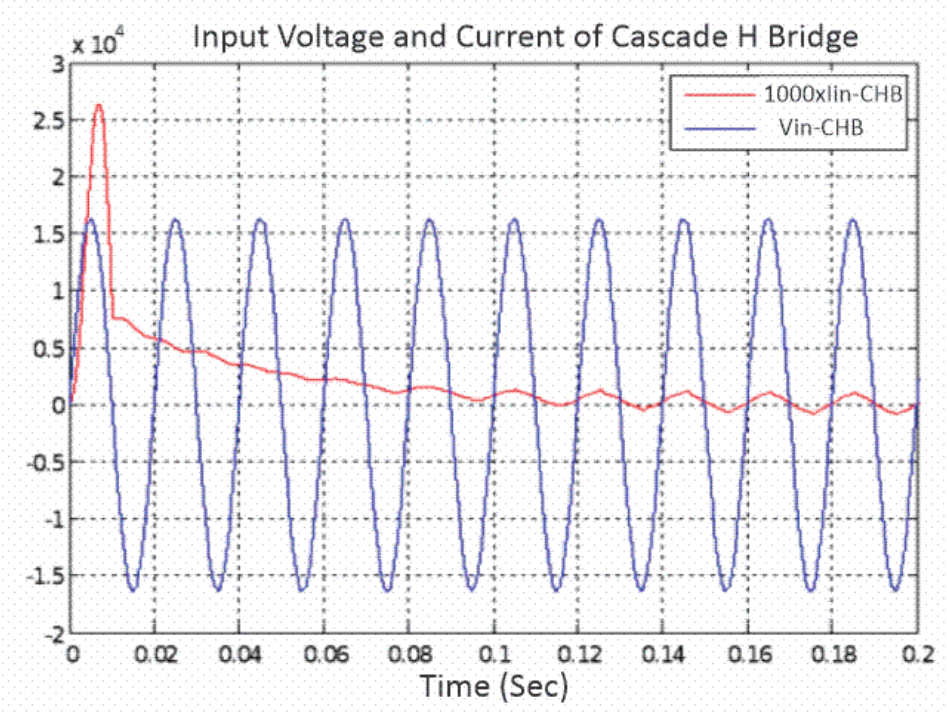

Figure 17

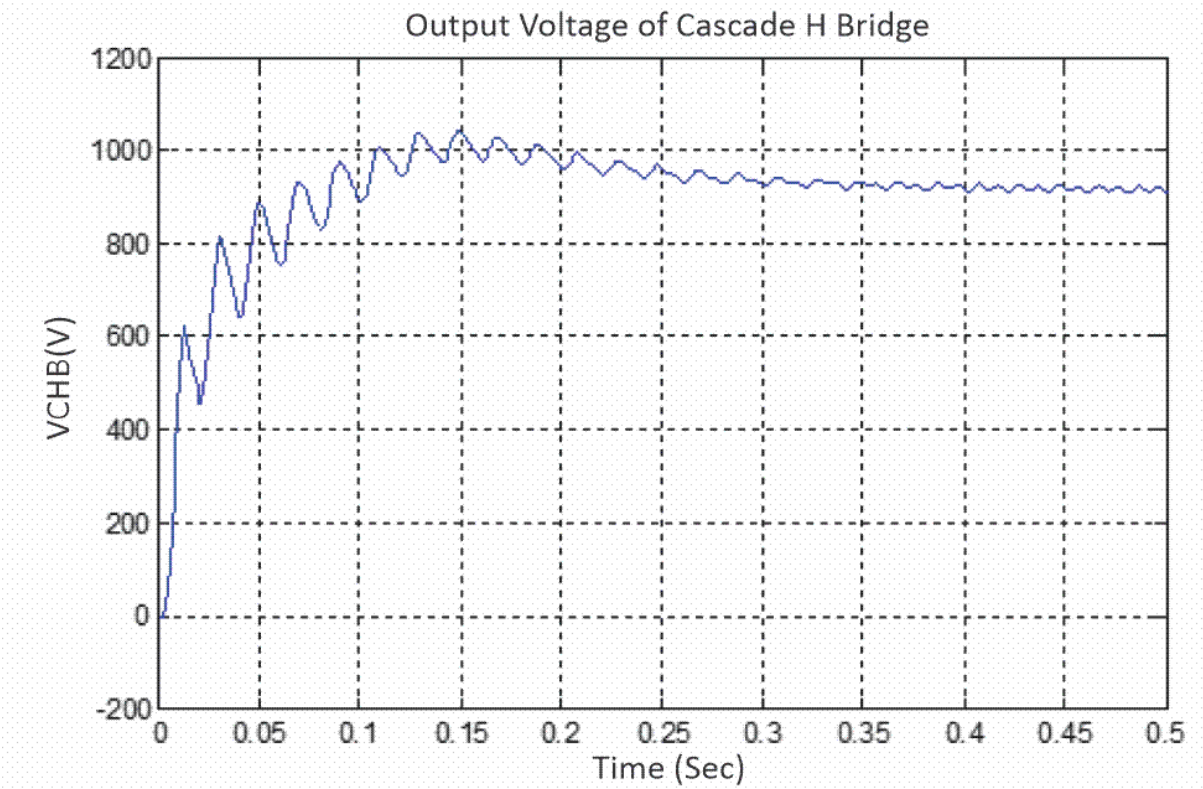
Output Voltage of Cascade H Bridge
VCHB(V)
Time (Sec)
1200
1000
800
600
400
200
0
-200
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5

Figure 18

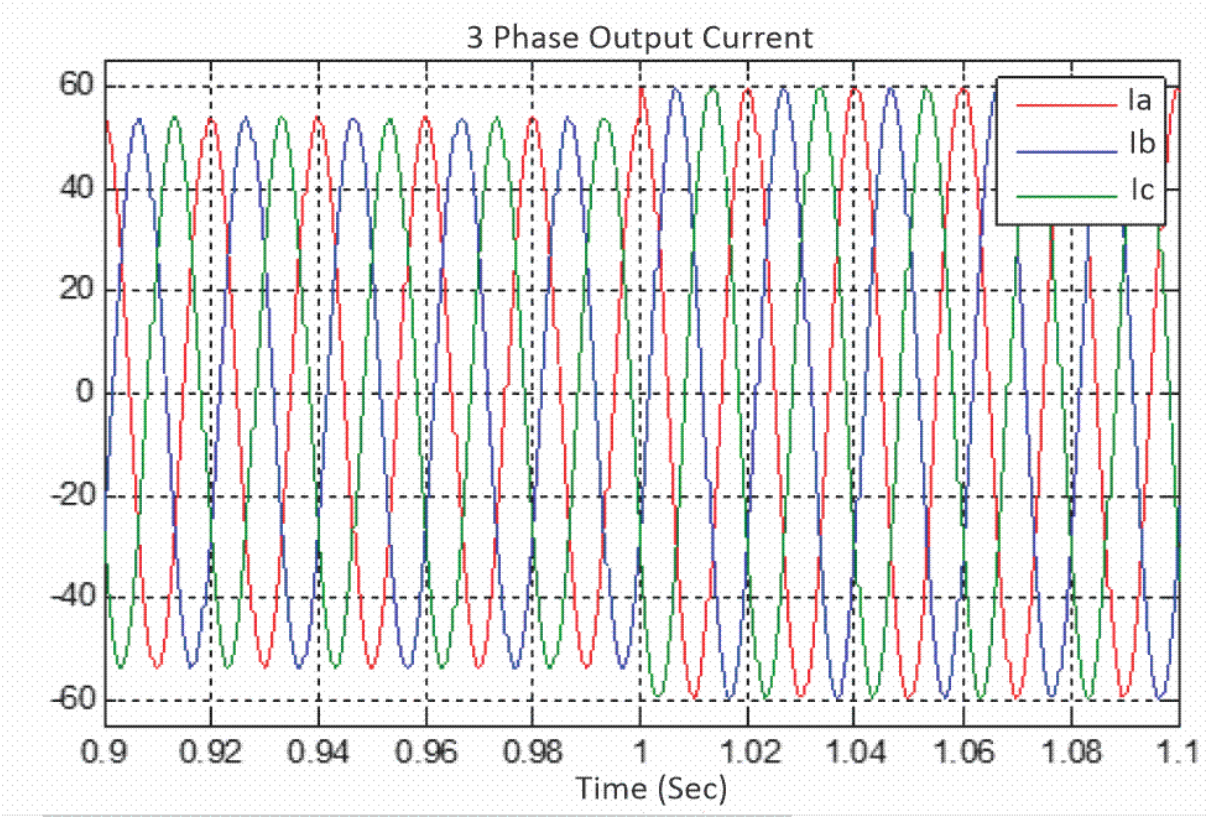

Figure 19

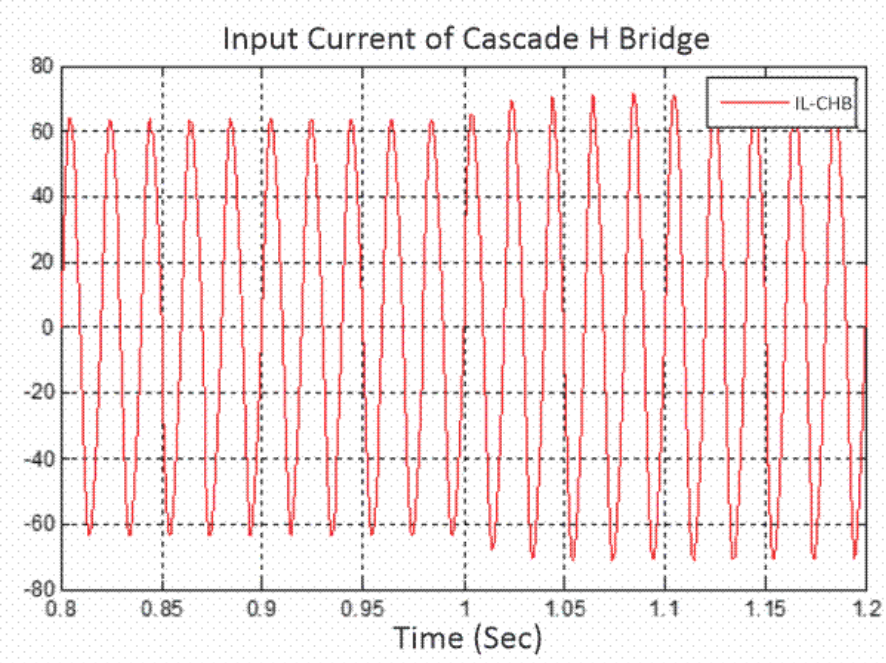

Figure 20

Table 1

Parameter	Value	Unit
$v_{ac,in}(t)$	sinusoidal maximum voltage =16330 (phase to ground)	V
$v_{ac,out}(t)$	sinusoidal maximum voltage =380 (phase to phase)	V
L_{CHB}	44	mH
C_{CHB}	118	μF
n_{Tr}	2.24	-
L_{DAB}	8.26	mH
C_{DABo}	383	μF
L_{3P4L}	33	μH
L_n	0.1	mH
C_{3P4L}	46	μF