Title: Performance Assessment of DC Circuit Breakers in Networks with Unpredictable Fault Current Peak Value

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Abstract

The development of medium voltage DC (MVDC) and high voltage DC (HVDC) networks emphasizes protecting network-connected elements, with the DC Circuit Breaker (DCCB). The use of DCCBs with a short interruption time is crucial to prevent damage to converters. Resonant DCCBs based on mechanical switches, semiconductor switches, and hybrid DCCBs (HDCCBs), have been proposed to efficiently interrupt fault current. The HDCCB, based on the current commutation drive circuit (CCDC), offers a simple structure that efficiently interrupts fault current and reduces pre-fault losses. This structure can only be successfully interrupted at a specific rate of fault current and a specific peak of fault current while changing the location of the fault disrupts the interruption performance of this HDCCB. This study aims to evaluate and analyze the various structures of DCCB particularly the HDCCB based on CCDC, which is considered superior to other DCCBs. The study highlights the limitations of using HDCCB based on CCDC to interrupt fault current peaks, with simulated verification by Finite Element (FE). A 44 kV network with fault current maxima ranging from 2 to 7 kA is used as a case study to highlight inadequacies and propose further research.

Keywords: DC network, DC circuit breaker (DCCB), Mechanical switches (MS) limitations, Hybrid DCCB (HDCCB), current commutation drive circuit (CCDC).

I. Introduction

The advancement of power electronic equipment has caused the growth of DC sources, DC consumers, and consequently DC transmission lines and protection in modern networks. The replacement of voltage source converters (VSC) instead of line commutated converters (LCCs) and the development of multi-terminal DC networks (MTDC) resulted in the integration and development of the high voltage DC network (HVDC). In addition, the use of multi-module converters (MMCs) in HVDC networks has led to the stable performance of this network [1], [2], [3], [4], [5], [6], [7], [8]. Research into diverse applications of medium voltage DC networks (MVDCs), such as traction and electric ships, has also increased significantly. In recent years, conversion AC systems have been converted to DC operation to improve power transmission capacity and accommodate additional distributed generation (DG) in distribution networks [9], [10], [11].

The transmission and distribution of DC electricity will provide numerous benefits, including reduced losses, better integration of renewable generation sources, and novel control and dispatching methods. However, DC fault protection is one of the factors influencing the evolution of the DC network. Interrupting the DC fault current is difficult since normal and fault currents do not cross zero in DC circuits, and the fault current increases rapidly [12]. AC breakers cannot be used alone due to the lack of a zero-crossing current, as these breakers can only successfully break at a zero current. Furthermore, selecting the right breaker for a DC network is a complicated issue because, in DC networks, the rate of increase in fault current is not only high but also uncertain. The first origin of the unpredictable fault current rise rate is the fault inductance, which depends on the fault location and the line reactance, which can be considered a serious challenge. Furthermore, when a fault occurs, the reflected wave causes a rise in the network's inductance voltage. This issue causes the fault current to increase at a variable rate. Therefore, the peak fault current is not a fixed value [13], [14], [15], [16].

The first MV-level DC breakers included mechanical switches (MS) and resonant components [17], [18], [19], [20], [21]. When a fault occurs, the MS forms an arc, and the resonant current created by passive parts flows across the mechanical-breaker, potentially causing interruptions at zero crossings. In this construction, zero crossing current may not occur at the start of the current resonance; even after the zero crossing current, the *di/dt* may exceed the MS's permitted range, resulting in a longer interruption time [22], [23]. The slow interruption speed of MS-based DCCBs

led to the development of solid-state based DCCBs (SSDCCBs). The SSDCCBs can be divided into two types of structures; in the first structure, the IGBT array is used in series and parallel as an element to interrupt the fault current [24]. In the second structure (known as Z-Source DCCB), Silicon Controlled Rectifier (SCR) is used as a fault current interrupter switch. In Z-Source DCCB, due to utilization of SCR, the current is reduced to zero with elements such as magnetic coupling, and then it is cut off by the SCR or transferred to a branch consisting of a capacitor, and the capacitor damps the fault current [25], [26], [27]. High power losses in the pre-fault state needed for the complex cooling system and limited tolerances for voltage and current stresses caused the development of hybrid DCCBs (HDCCBs) [28], [29], [30], [31]. The first structure developed by ABB included three branches. In the first branch, an ultra-fast disconnector (UFD) was connected in series with a load commutation switch (LCS). The main branch (MB) uses an array of IGBTs, whereas the last branch has a voltage limiter. Before the fault, the current flows via the LCS and the mechanical breaker; after the fault, the LCS transfers the current to the MB, which causes an arc-less operation of the UFD, and the IGBTs on this branch turn off the fault current. However, the power losses of LCS as a semiconductor switch in the nominal current persist and increase, complicating the structure's cooling system and reducing its reliability. Pre-fault LCS losses prompted the use of the current commutation drive circuit (CCDC) construction instead of LCS. This structure comprises two windings with magnetic coupling, one connected to the network side and the other to the pre-charged capacitor via a SCR. The difference between CCDC and LCS is in the commutation principle. In CCDC, the command to open the UFD is first given, and then the MS starts to arc. Then, after a while has passed, activating the SCR, the capacitor on the network side is discharged, and the commutation process is performed. The use of a low number of winding turns on the network side makes the power losses of this structure less in pre-fault compared to the structures based on semiconductor switches. On the other hand, less arc time and higher interruption speed make it perform more optimally than resonant structures.

The DCCB based on CCDC structure offers the benefits of minimizing losses in the pre-fault state and ensuring fast interruption speed, distinguishing it from other DCCB structures. However, the successful interruption of the fault current by the CCDC structure is complicated. Challenges caused by the increased rate of the fault current which affect the fault current peak, and the limitations of the mechanical breaker in breaking the fault current at zero crossing lead to possible malfunction of this type of DCCB. This article provides a comprehensive analysis of the

performance of various DCCB structures compared to the CCDC structure. The aim is to identify the advantages and disadvantages of the CCDC structure and propose solutions for its shortcomings and defects.

II. Fault mechanism in DC networks

As noted in the introduction, HVDC and MVDC networks have distinct structures. Figure 1-a and b depict two general topologies of DC network structures. The network inductance is one of the parameters that influence the rate at which the fault current increases in both network architectures. Network inductance can also differ according to the location of the fault [13].

On the other hand, a pole-to-ground fault is considered on the cable side. The fault generates a reverse traveling wave to the converter whose peak can be up to -V_{DC}. The peak value of this wave is reduced and calculated by the e^{-KD}, where K is the attenuation coefficient of the cable and D is the distance. This wave hits the DC breaker as a large impedance and is reflected so that the cable side voltage changes to negative. Therefore, the inductance between the converter and the fault location faces a voltage higher than the V_{DC}, which leads to a boost in the fault current increasing rate [14], [15], [16].

Therefore, the worst case of fault current increasing rate in the DC network is not a terminal fault but a fault occurring some way down the cable. This issue leads to mathematical calculations not assuming a specific value for the worst rate of increase of the fault current in the DC network.

Figure 2 depicts a simplified DC network that includes network inductance connected to the load via DCCB for analyzing the DCCB performance and a residual circuit breaker (RCB). As illustrated in Figure 2-a, the current flows through the DCCB and RCB in the pre-fault state; therefore, the DCCB should have the least power losses and effects during this time. When a fault occurs, two detection procedures are performed. The first employs several current samples to determine fault occurrence and the rate at which the fault current rises. As shown in Figure 2-d, the peak of the fault current varies owing to the different rates of fault current increasing. Thus, the DCCB must be capable of interrupting the peak of various currents.

The latter method, as illustrated in Figure 2-e, detects faults based on the peak of the fault current. Therefore, the current peak remains constant while the fault current rise rate varies. Thus, the DC circuit breaker must be able to interrupt

the rate of increase in current caused by various problems. As illustrated in Figure 2-c, the energy held in the network inductor is discharged at the post-fault state, and the RCB switches off the remaining current.

Therefore, the expectations of a DCCB are as follows:

1) Has the ability to interrupt the fault current as fast as possible.

2) In the pre-fault state, the DCCB causes the most negligible losses on the network.

3) Be able to interrupt the uncertain peaks of fault currents with different fault current increasing rates.

4) Arc-less interruption to minimize MS contact surface corrosion.

III. Different types of MV and HV DCCBs

Three generic structures have been proposed for DCCB:

1-Mechanical based CBs

2-Semiconductor-based DCCBs

3- Hybrid DCCBs

Zero crossing must occur in all structures that use mechanical breakers to cut off or isolate the fault current. Three categories of mechanical breakers in DCCBs are used to interrupt or isolate the fault current: gas circuit breaker (GCB), vacuum circuit breaker (VCB), and air circuit breaker (ACB). All three structures will have a successful interruption when the *di/dt* is lower than their tolerance range. The *di/dt* range that ACB can interrupt is much less than that of GCB and VCB. As it is clear from Figure 3, VCB and GCB have been tested under a nominal current state current with high frequency. Based on this test, two output results can be obtained [22], [23]:

1) The maximum *di/dt* that is able to be interrupted by VCB in a short time is below 400 *k*A/*m*s and only one interruption test has been done successfully. (The maximum current is 31 *k*A). While for more successful interruption occurrence, *di/dt* should be below 100*k*A/*m*s. On the other hand, no successful interruption occurs in GCB, and the permittable range for GCB is under 20*k*A/*m*s.

2) The more important point is that in any *di/dt*, which can be interrupted by a mechanical breaker, it completely depends on the type of contact, the cut-off time, and the gas pressure inside the breaker. For this reason, as shown in Figure 3, the

di/dt in which the successful interruption hasn't a certain value in the same case study.

A. Mechanical based CBs

The mechanical type is divided into arc chute CBs and resonance CBs.

a. Arc chute circuit breakers

As shown in Figure 4, arc chute CBs are made up of plates where the arc is transmitted from the main contact to the plates after the fault occurs, and the arc voltage is divided to interrupt the fault current. This topology is compatible with both alternating current and direct current networks. To enhance the operating voltage level of this breaker, the solution of increasing arc length was offered, which was accomplished by extending the distance between arc chutes, as shown in Figure 3-b. As the distance grows, the speed of breaker action reduces significantly. An external electromagnetic force was applied to enhance the arc length without increasing the breaker's operation time, as shown in Figure 3-c. SF6 gas was utilized instead of air to improve the breaker's breaking performance up to medium voltage levels.

The advantages and disadvantages of arc chute based CBs can be concluded:

1) Low resistance of contact of structure in the pre-fault state, and the power losses related to its performance are also reduced in this state.

2) It has the lowest voltage level among medium voltage breakers and its voltage development is complicated. On the other hand, it also operates during the arc which causes corrosion of the contacts.

3) It only has the ability to interrupt a specific fault current peak, and if the fault current peak increases, according to the fixed structure of the arc chutes and the specified arc voltage, the current interruption procedure will be disrupted.

4) The Operation time of the breaker is too long compared to the development of the network.

b. Resonance circuit breakers

The passive elements are used to create a zero-crossing current and employ an SF6 breaker to interrupt the current. After the fault occurrence and the MS opens, a portion of the current is transmitted to the resonant branch, and as the arc voltage

decreases with increased current, a resonant current is applied to the MS. The resonance current equation created by passive elements is as follows:

$$L_c \frac{d^2 i_{res}}{dt^2} + \frac{dU_{arc}}{di_{MS}} \frac{di_{res}}{dt} + \frac{1}{C_c} i_{res} = 0 \quad (1)$$

Where L_c and C_c are the resonant elements, and U_{arc}, i_{res} and i_{MS} are the arc voltage, resonant branch current and MS branch current, respectively. When zero crossing of the current occurs, the arc can be extinguished and the MS can be opened. The voltage across the switch then rises until an arrestor is triggered as mentioned in Figure 5-a. As it is clear from Figure 5-c, in the first few resonances, zero crossing may not occur, and after the occurrence of zero-crossing, the successful interruption happens when the mechanical *di/dt* breaker limit in zero crossing is also exceeded. Comply for this reason, the interruption time of this DCCB is completely variable and can last up to 12 *m*s.

Figure 5-c clearly shows that the resonant current increases over time. A fault current limiter (FCL) is added to address this issue before the breaker, as shown in Figure 5-d [18], [32]. The next step in creating faster resonance is to utilize a pre-charged capacitor, which has been limited by *di/dt* in zero crossing, so the interruption speed does not vary significantly. The next structure for improving the resonance based DCCBs, as illustrated in Figure 5-b, is to use a full-bridge voltage source converter (VSC) as an active oscillator with passive elements. One of the benefits of this design is the ability to alter the resonance rate, which approximately covers the mechanical *di/dt* breaker constraints. Still, the negatives include a lack of clarity in the cut-off time and cut-off under the arc. The resonant structure outperforms the arc chute structure regarding operating voltage level limit and ability to interrupt the peak of varied fault currents. On the other hand, the unpredictable interrupting time and, as a result, the variable current peak may be one of this DCCB's weak points, causing damage to other equipment.

B. Solid State DCCBs

As mentioned in the introduction, the conventional structure of SSDCCBs (Figure 6-a) uses a series and parallel arrays of IGBTs, once a fault occurs, all these switches are turned off and the overvoltage is controlled by the voltage limiter. The Z-source DCCB structure is considered another SSDCCB. As shown in Figure 6-b, an SCR array with magnetic coupling is used. Before the fault, the current passes through the branch of the semiconductor switches and as soon as the fault occurs,

the current in the SCR branch is zeroed by the magnetic coupling with the opposite current flow, and the SCR is turned off. In addition, the current is transferred to the capacitor branch and damped. In Figure 6-c, as another Z-source DCCB, two LCSs are used for fault current commutation. Before the fault, the current passes through all the semiconductor switches and as soon as the fault occurs, the LCS transfers the current to the capacitor branch, and the current is dumped there. At the same time, when the SCR current becomes zero, the current in this branch is also interrupted.

Very fast interrupting speed and specific cutting time are two positive features of these DCCBs. This is while the nominal current passes through the switches in the pre-fault state, and the presence of forward voltage along with the resistance of the on state of each switch causes high power losses in this state [28]. As shown in Figure 7, the thermal control of switches will be complex. Turning on and off the series and parallel array of switches, on the other hand, is extremely intricate, and any delay in turning off or on any of the switches causes the rest of the switches to burn out [33], [34], [35].

C. Hybrid DCCB

In order to benefit from low losses in the nominal current and the quick interruption process, the combination of mechanical breakers with semiconductor switches has been used to make HDCCB.

a. HDCCB based on LCS.

The first structure was developed by ABB company. As shown in Figure 8, an UFD and LCS are placed in series in the first branch. A series and parallel IGBT array is used in the MB, and a voltage limiter is used in the last branch to control overvoltage. In the pre-fault state, the current passes through LCS and UFD. As soon as the fault occurs, the switches of the main branch are turned on, and the LCS is turned off, which leads to the current commutation to the main branch. Once the commutation process has been finished, the command to open the UFD is given. After completing the UFD opening process, the switches of the main branch are turned off, and the limiter dampens the current.

Fast and arc-less interruption and the ability to quickly reclose are the advantages of this structure. However, the mechanical breaker constraint limits this DCCB's speed. The presence of LCS while nominal current passes results in power losses and complex thermal management. This is while the losses are significantly lower than in the SSDCCB structure.

b. Superconductor based HDCCB

One of the proposed structures is to employ superconducting components rather than LCS, as illustrated in Figure 9. The superconductor cooling system provides the lowest resistance at a nominal current. After the fault occurs, an increment in the cooling system's current and temperature causes the superconducting portion's resistance to increase, and the current switches to the main branch. Functionally, the resistance during the fault is lower than the off-state resistance of a semiconductor switch, and residual current flows through the mechanical switch, potentially resulting in mild arcing. However, the high cost of superconducting materials, the lack of development in long lengths, and the extremely complex cooling system rendered this construction uneconomical.

c. HDCCB based on CCDC

In another version of HDCCB, a magnetic coupling is used instead of LCS. Figure 10 shows that the CCDC comprises two windings: the first has fewer turns and is positioned on the network side, while the second is connected to a pre-charge capacitor via a SCR. When the nominal current flows through the UFD and the primary side of the CCDC, this configuration produces the lowest power losses compared to the preceding structures due to the reduced resistance of the primary winding, resulting in a lower temperature of the CCDC and eliminating the cooling system. When the fault occurs, the command to open the UFD and close the main branch switches is initially issued, which leads to the occurrence of an arc. The SCR is then active after a predetermined time, and the injection of the pre-charged capacitor current causes the primary side fault current to commutate. The main branch switches are turned off when the UFD is fully open, and the commutation is complete. This structure not only has fewer losses in the pre-fault condition than LCS-based HDCCB and SSDCCB, but it also has faster interruption and less interruption time depending on the capacitor capacity and the number of turns of the windings in comparison to resonance-based DCCBs. Furthermore, it is more affordable than the SSDCB construction by removing the cooling system. Owing to the numerous benefits of this structure, several network structures are examined by ANSYS software in the simulation section to better understand the pros and drawbacks of this topology.

IV. Performance analysis of CCDC using FE simulation

The long interruption duration of resonant mechanical DCCBs, combined with substantial pre-fault losses in SSDCCBs and LCS in HDCCBs, make HDCCBs

based on CCDC a desirable choice, as discussed in the literature review. So, several simulations were analyzed to highlight the limitations of interrupting HDCCB based on CCDC in the commutation of the peak of different fault currents. By addressing and overcoming these concerns, CCDC emerges as the superior choice over other DCCBs. The FE simulation is presented through ANSYS Maxwell software.

A. Specifications of simulations

Figure 11 depicts the proposed circuit in ANSYS Simplorer and the CCDC structure in Maxwell. The proposed network is a 44 kV network with a nominal current of 0.3 kA. When a fault occurs, the rate at which the fault current increases in this network is determined by different inductances, as indicated in Table I.

Using the same sampling period in each scenario to determine the fault, the peak fault current values are 2*k*A, 3.1*k*A, and 7.3*k*A, respectively. According to the [36] the CCDC model will be as follows:

$$\begin{pmatrix} L_1 & M & 0 \\ M & -L_2 & 0 \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} di_{CCDC}/dt \\ di_c/dt \\ dv_c/dt \end{pmatrix} = \begin{pmatrix} v_{MB} - v_{arc} \\ v_c \\ i_c/C_c \end{pmatrix} \quad (2)$$

where L_1 is the magnetizing inductor on the network side, L_2 is the magnetizing inductor on the capacitor side, and M is the mutual inductance, which are obtained from the FE solution. In addition, the amount of capacitor voltage (v_C) and its capacity (C_C) are considered equal to and 820V and 50μf, respectively. Both windings are wound on the air core, with 5 turns on the network and 20 turns on the control side. Both windings are wrapped around each other to reduce leakage flux.

B. Simulation results

In all test scenarios, the command to open the UFD is issued at time t=1.2 *m*s. The SCR is engaged in 1.21 *m*s after the UFD generates a 50 V arc voltage, which helps the current commutation process. As demonstrated in Figure 12, Figure 13, and Figure 14, the control current begins to rise and reaches its peak at 1.24 *m*s. In contrast, the capacitor's voltage hits zero at 1.25 *m*s. Figure 12 shows that the commutation procedure is successful with a fault current slope of 2.7 *k*A/*m*s and a peak fault current of 3 *k*A. In addition, zero crossing is performed with an appropriate *di/dt* (70 *k*A/*m*s) of UFD, and successful interruption is achieved.

Figure 13 shows that as the path inductance decreases, the fault current's rate of rise climbs to 6.66 *k*A/*m*s, resulting in the commutation of the current failure. The failure of current commutation results in no zero current being formed in the mechanical breaker, and the current cannot be interrupted by the UFD in the first branch. If UFD does not interrupt the current, the current in the UFD branch will begin to grow again.

In Figure 14, the path's inductance has increased, and the slope of the fault current increase has decreased to 1.66 *k*A/*m*s. The slope of the fault current at the initial zero crossing has reached 98 *k*A/*m*s, making it impossible to interrupt with a VCB, as described in section III. On the other hand, due to the incomplete discharge of the capacitor, the current in the UFD branch becomes negative, and this excess current passes through the branch of the main IGBTs and leads to damage to them. In the second zero crossing, where the capacitor is completely discharged, the rate of current change is 354 kA/ms, which cannot be interrupted by any of the topologies of mechanical breakers.

C. Enhanced CCDC and future improvement

As previously stated, one of the characteristics that DCCB should include is the ability to interrupt the fault current by changing the fault current rise rate and, as a result, the fault current peak.

As is obvious from the simulation results, an increase in the fault current rate in the CCDC-based HDDCCB caused no zero crossing current. As a result, the UFD could not have a current interruption, and the overall performance of the breaker would be disturbed. On the other hand, as the rate of increase of the fault current dropped, two zero-current crossings occurred, with *di/dt* values that exceeded the VCB tolerance. As a result, it can be stated that the CCDC structure is intended for only one fault current rise rate and a particular network configuration.

To improve CCDC performance, instead of using one capacitor, several capacitors are used in parallel based om Figure 15- (a). The capacity of the capacitors is determined based on the lowest rate of increase of the fault current and their number is determined in such a way as to successfully commutate the highest rate of increase of the fault current in the network that is used. Therefore, the number of fired SCRs (paralleled capacitors) depends on the increasing rate of the fault current so that the commutation of the fault current is done successfully as shown in Figure 15 (b) and (c).

For future works, an array of capacitors can be used in series and parallel, which are activate to the circuit in a sectional manner based on the peak of the fault current and the desired commutation rate. In addition, it is possible to adjust the voltage of the capacitors to adjust the commutation rate.

V. Comparison study of different DCCBs

Each DCCB has advantages and disadvantages, and some limits must be addressed to get optimal performance. According to Table II, resonant mechanical DCCBs have the slowest speed in interrupting the fault current, while SSDCCBs have the best speed. Regarding power losses and cooling system complexity, using semiconductor switches in HDCCB structures based on LCS and SSDDCCB in the pre-fault state results in the most significant power losses and the most complex cooling system. On the other hand, structures based on mechanical switches that do not use semiconductor switches in the pre-fault state, such as CCDC and resonance structures, have lower power losses. The presence of an arc in the structure of CCDC and mechanical resonance-based DCCB is inevitable due to the use of MS, but the duration of the arc occurrence in CCDC is short enough if the interruption has been done successfully. In structures where mechanical breakers are used, it is necessary to comply with the limits of the mechanical breaker to make a successful interruption. Hybrid DCCB with LCS is exempted from this limitation due to the current interruption before UFD opening. The ability to cut off variable peaks of the fault current or the rates of increase of the fault current makes the DCCB capable of being used in any network. Accordingly, the ability to interrupt more or less than the pre-designed fault current in the only structure that significantly leads to the deterioration of the interrupting performance by DCCB is HDCCB based on CCDC.

VI. Conclusion

The DCCB should exhibit minimal error to effectively serve as a protective component in the DC network. The accuracy of DCCB operation can be verified in low interruption time, low losses before the fault, and successful interruption of different peaks of the fault currents. The presence of semiconductor switches in the path of nominal current before the fault occurrence in structures such as LCS and SSDCCB causes losses and consequently complexity of the cooling structure. However, the resonant structures have a significantly longer breaking time when used in modern networks because they should achieve the appropriate rate of fault current change at zero-crossings of the MS current. Due to its minimal losses and appropriate interruption time, the CCDC structure can be seen as a beneficial option

when compared to other DCCBs. Nevertheless, the limitations of this design lie in its ability to interrupt just one current peak and its functioning during the arc. However, these drawbacks can be addressed by implementing the suggested recommendations of this paper.

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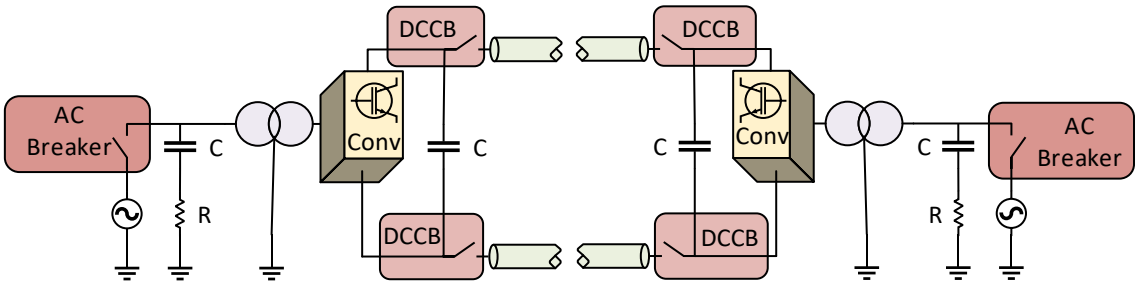
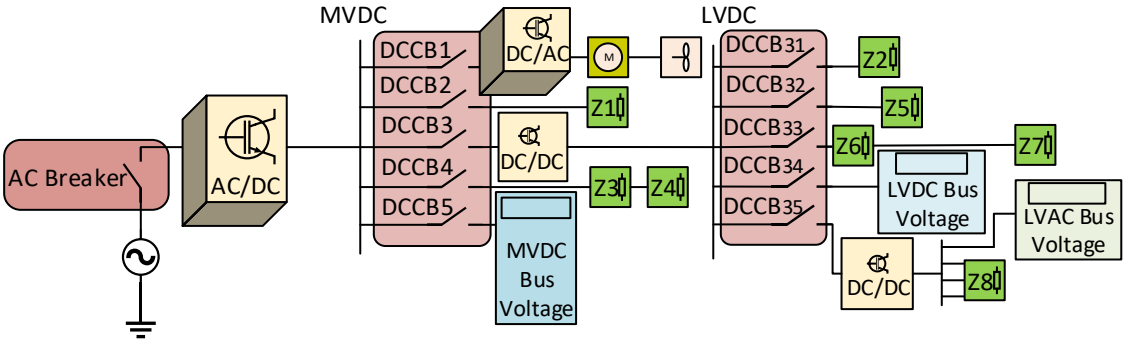


(a)



(b)

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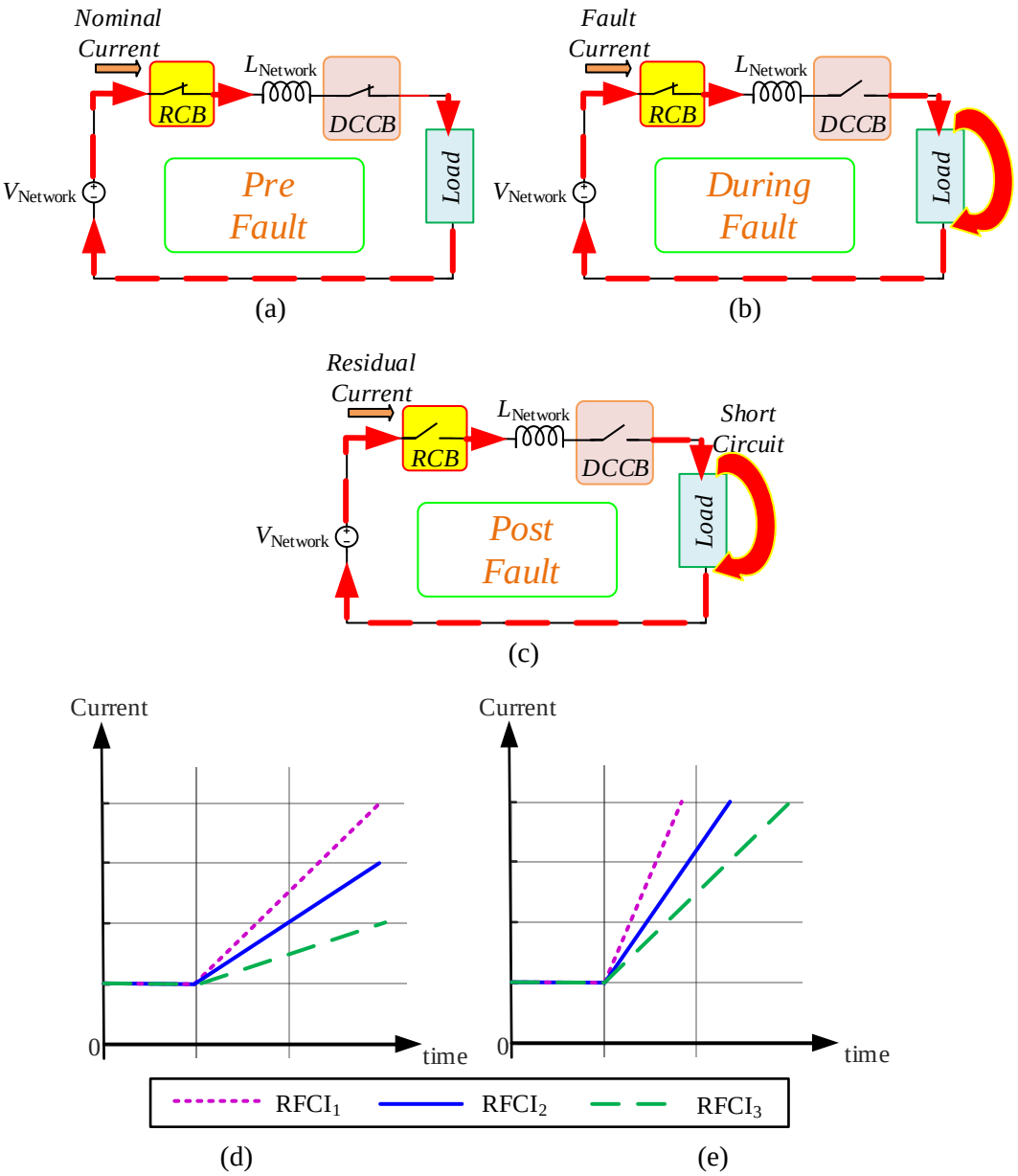

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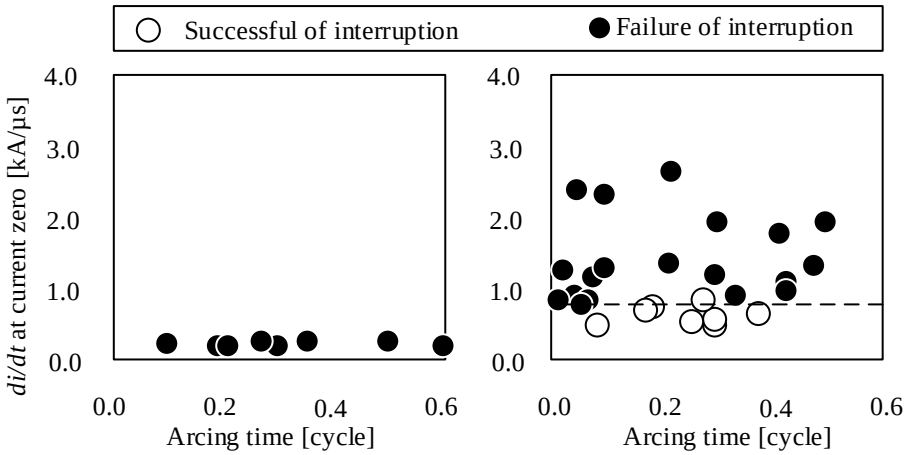

(a) (b)

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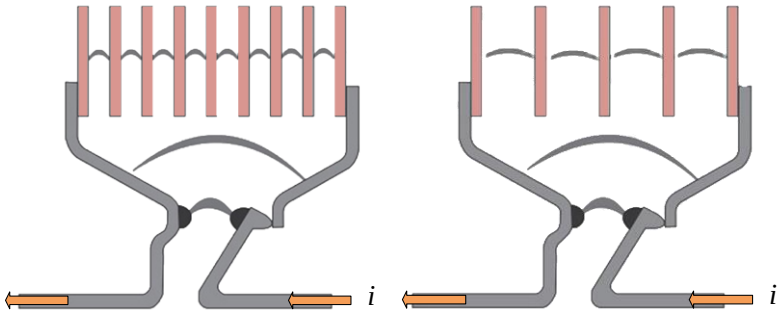
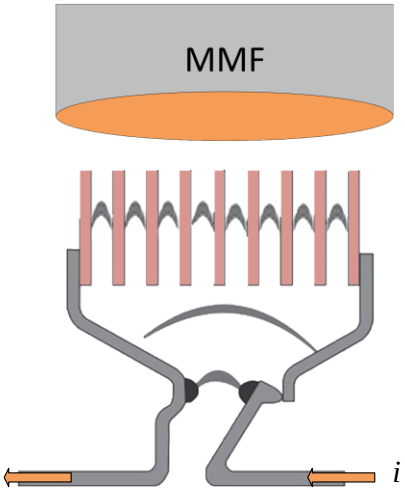


(a) (b)



(c)

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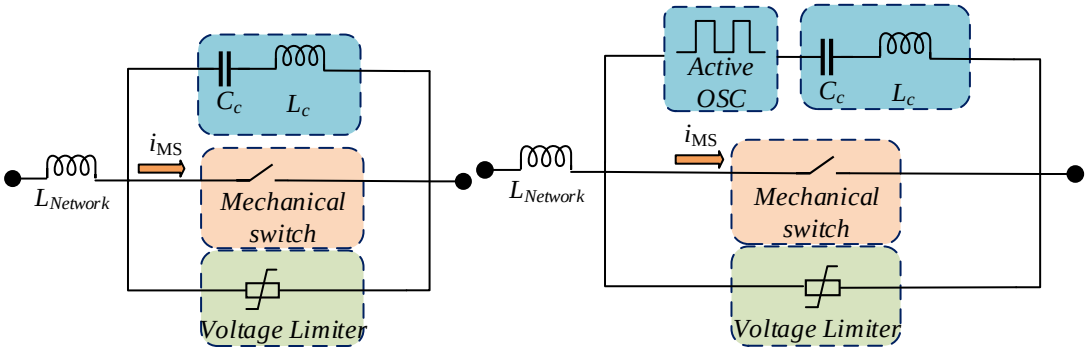
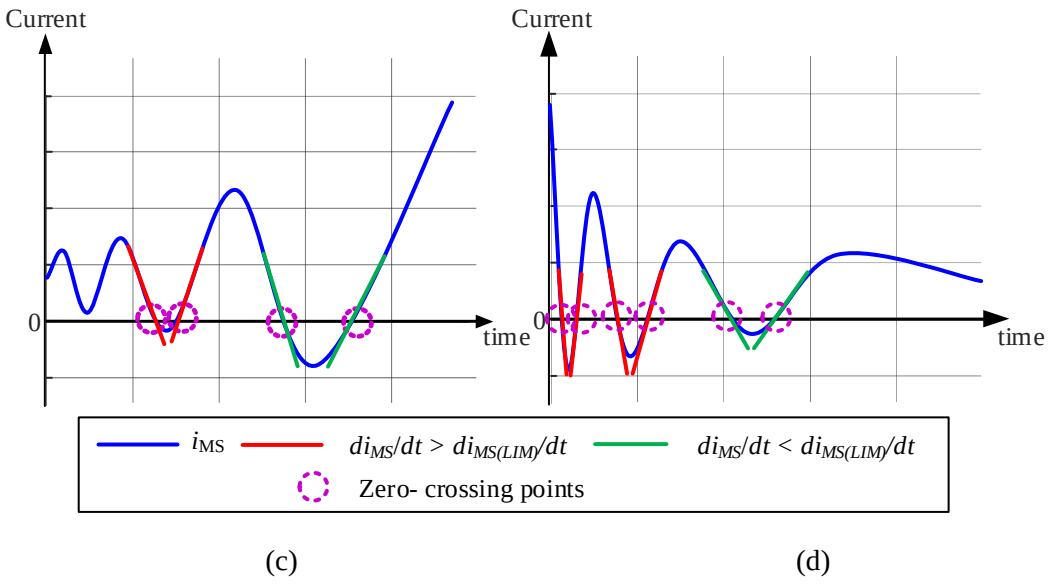


(a) (b)



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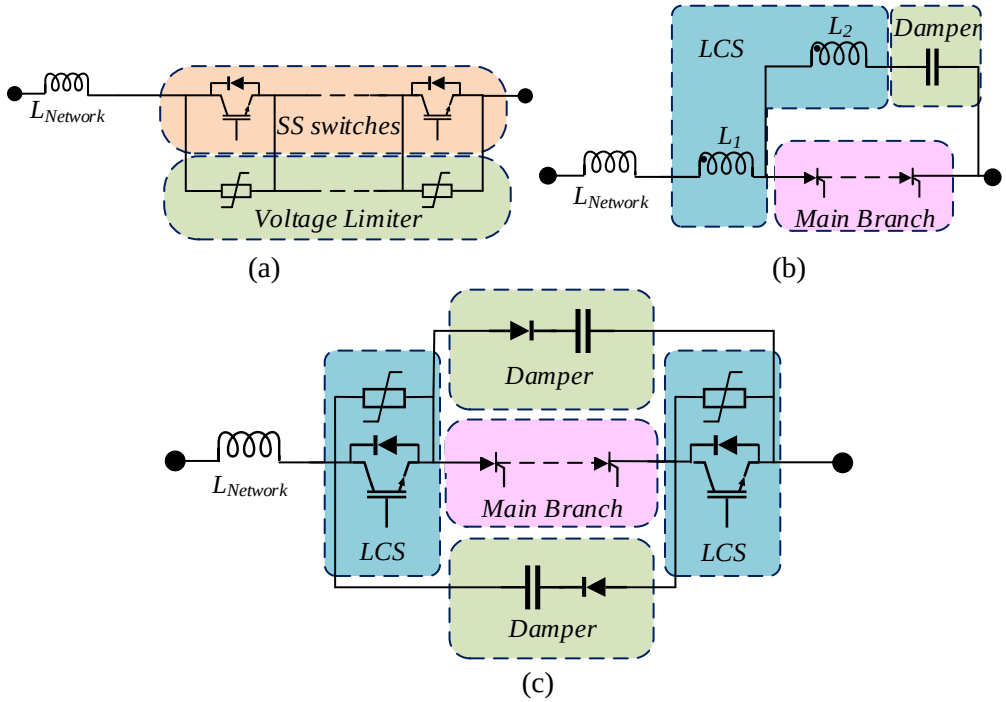

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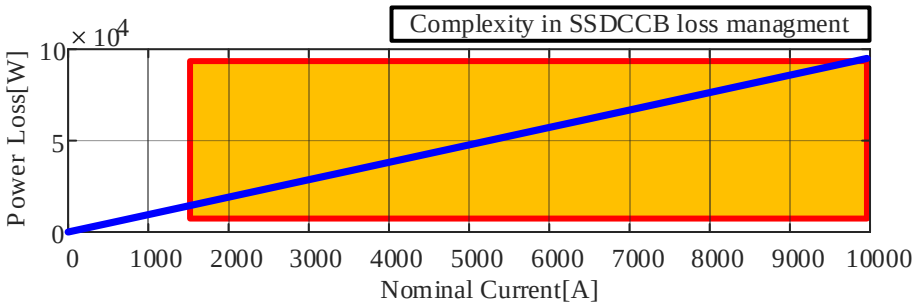


Figure 7: SSDCCB structure power loss and complexity of thermal management.

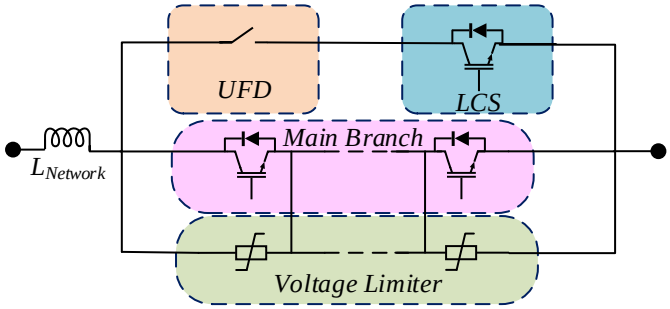


Figure 8: HDCCB using LCS developed by ABB.

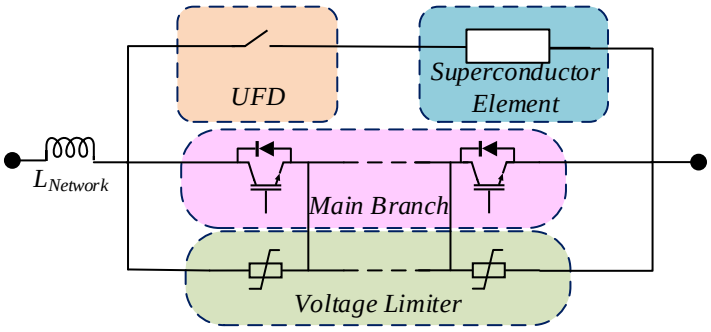


Figure 9: Super conducting based HDCCB.

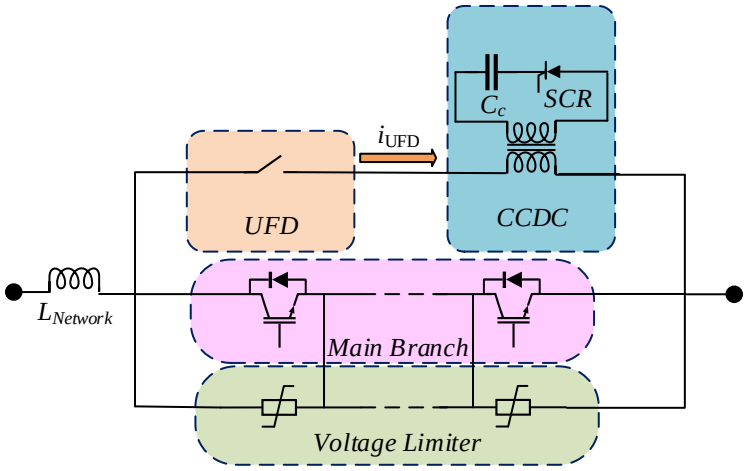
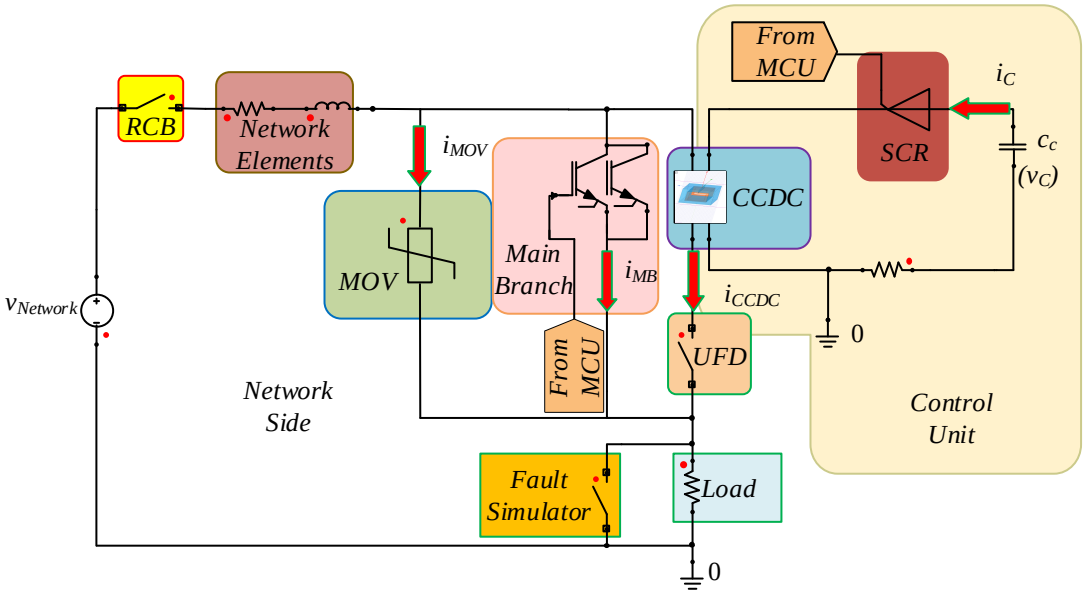
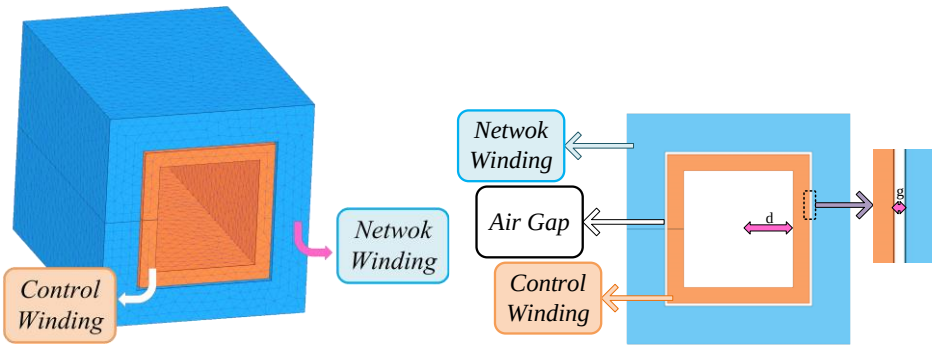


Figure 10: HDCCB using CCDC.

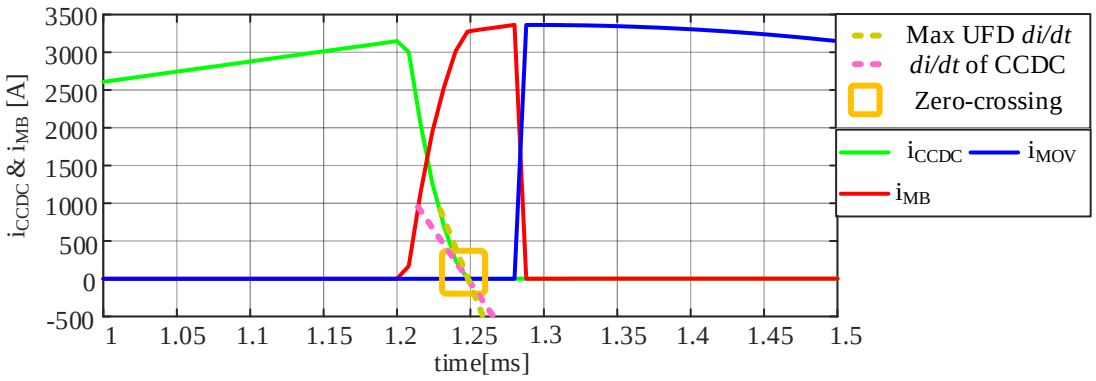


(a)

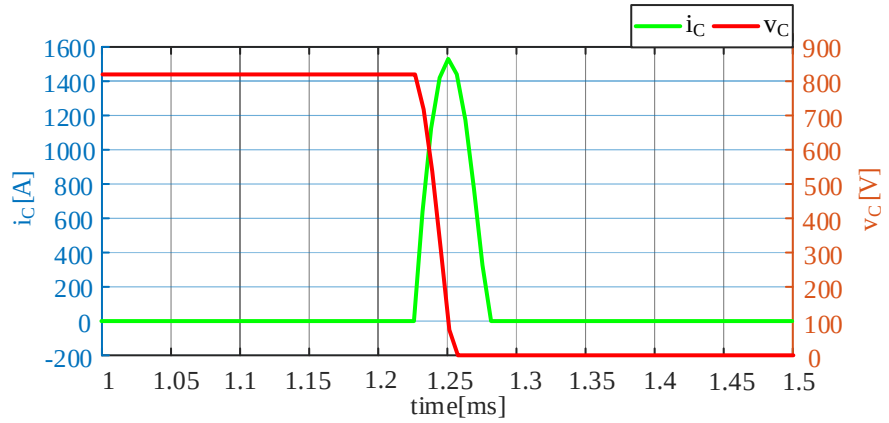


(b) (c)

Figure 11: (a) Ansys simplorer simulation circuit, (b) Ansys Maxwell model mesh sizing (c) Ansys Maxwell model side-view and dimentiones

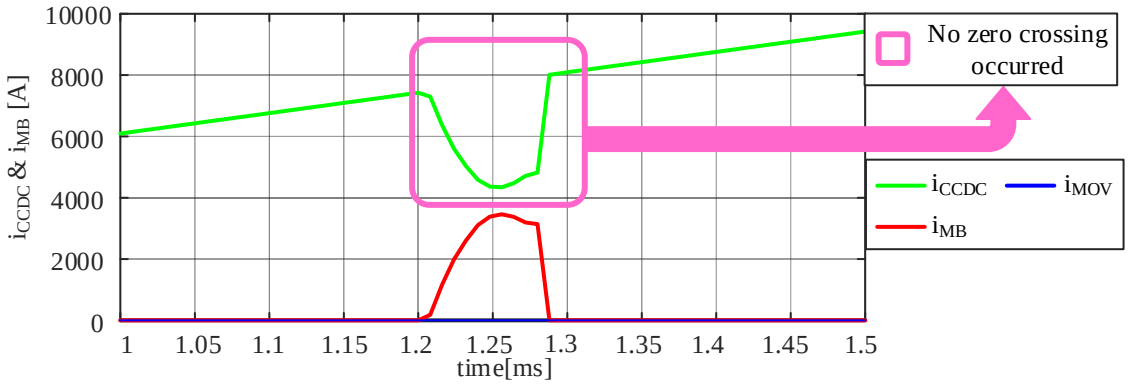


(a)

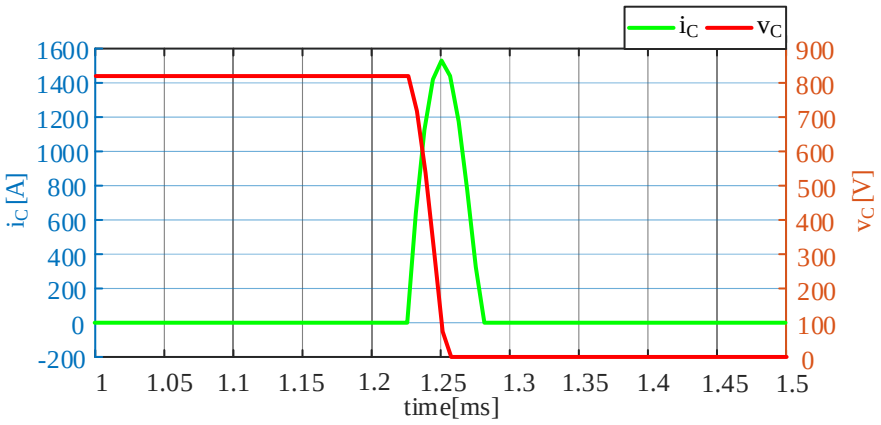


(b)

Figure 12: CCDC current, MB and MOV currents (a), the current and the voltage of control unit(b) while the increasing rate of fault current is 2.77 *k*A/*m*s.

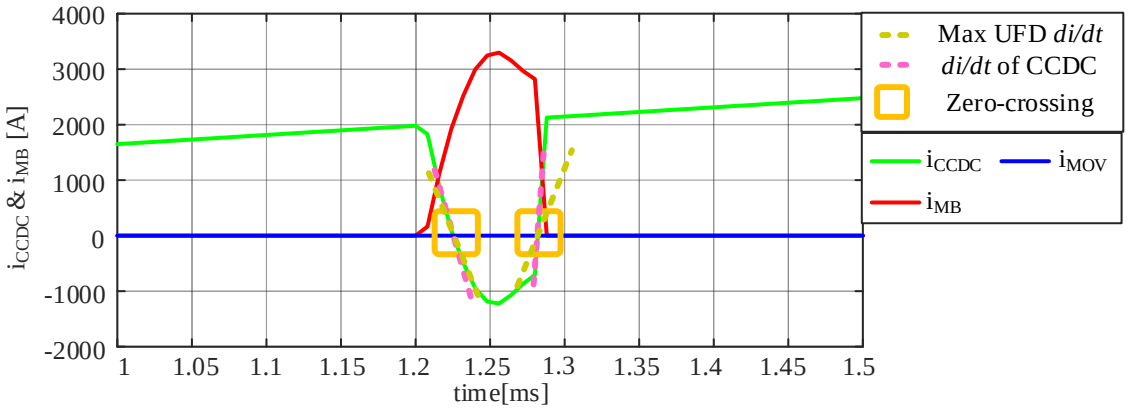


(a)

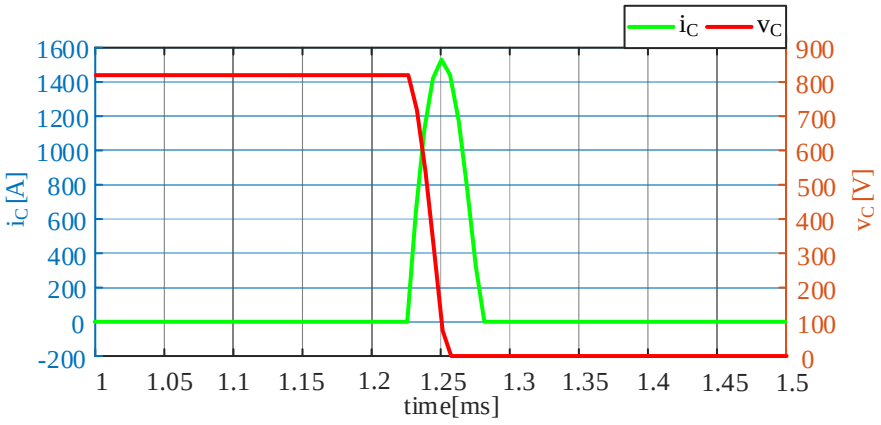


(b)

Figure 13: CCDC current, MB and MOV currents (a), the current and the voltage of control unit(b) while the increasing rate of fault current is 6.66 *k*A/*m*s.

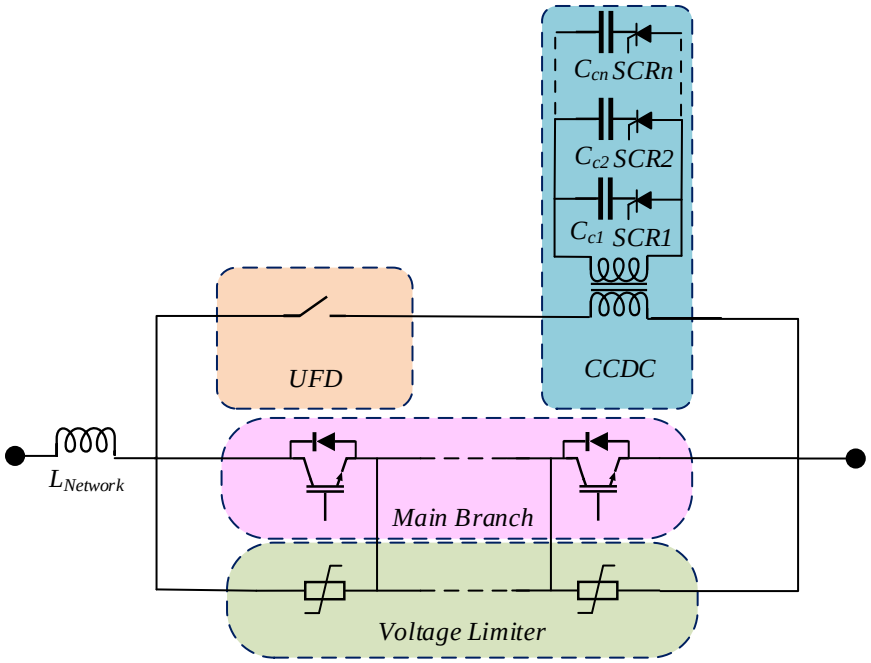


(a)

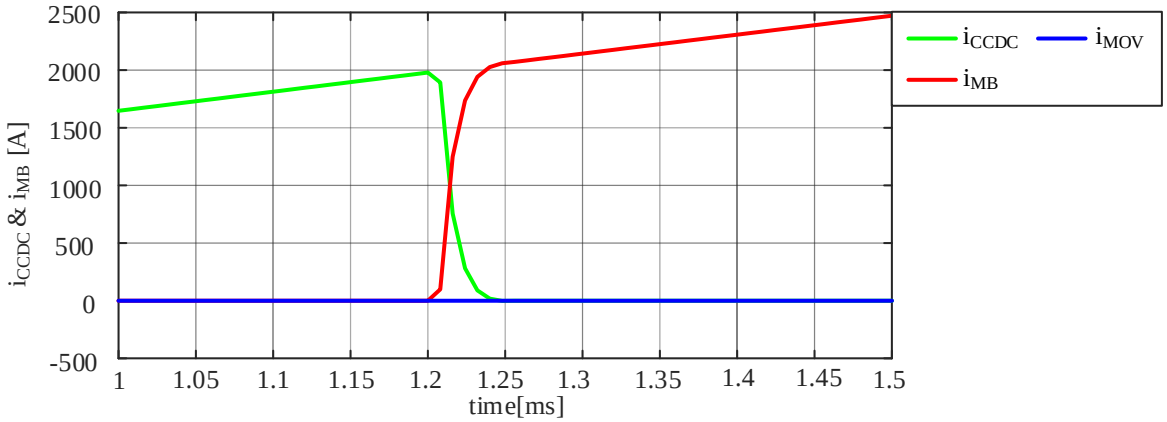


(b)

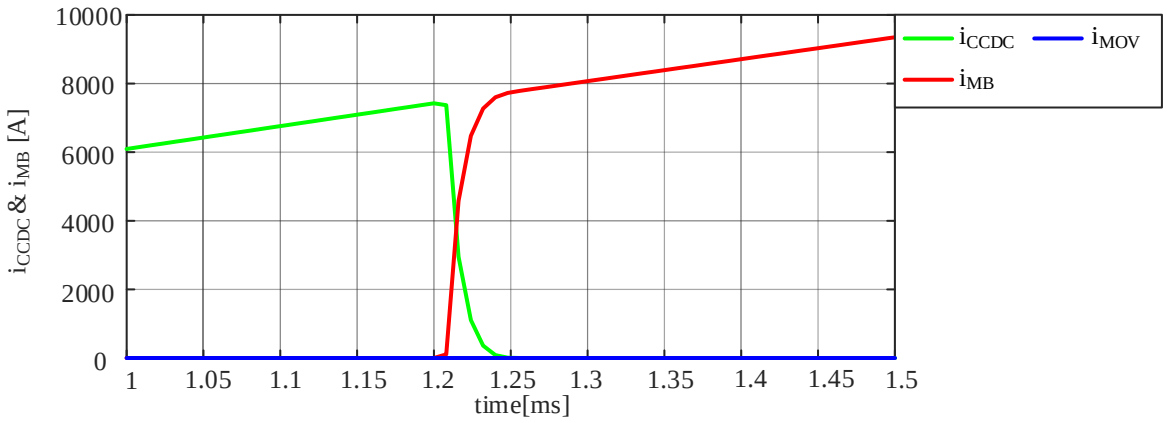
Figure 14: CCDC current, MB and MOV currents (a), the current and the voltage of control unit(b) while the increasing rate of fault current is 1.66 kA/ms.


C_{cn} SCRn
C_{c2} SCR2
C_{c1} SCR1
CCDC
UFD
$L_{Network}$
Main Branch
Voltage Limiter

(a)


2500
2000
1500
1000
500
0
-500
1
1.05
1.1
1.15
1.2
1.25
1.3
1.35
1.4
1.45
1.5
time[ms]
i_{CCDC} & i_{MB} [A]
i_{CCDC}
i_{MOV}
i_{MB}

(b)



(c)

Figure 15: Enhanced CCDC structure (a) to commutate fault current while the increasing rate of fault current are 1.66 *k*A/*m*s (b) and 6.66 *k*A/*m*s (c)

Table I: The case study specifications used for FE analysis [36].

Parameters	Rate of fault currnet increasing =1.66	Rate of fault currnet increasing =2.77	Rate of fault currnet increasing =6.66
L_{Network}	26.5 mH	15.9 mH	6.6 mH
Nominal current	300 A		
Network voltage	44 kV		
Maximum i_{CCDC}	2000A (At start of commutation)	3100A	7300A (At start of commutation)
Maximum i_{MB}	3500A	3400A	3800A
Network coil turns	5		
Control coil turns	20		
d (*c*m)	16		
g (*c*m)	2		
Control Capacitor	50μf and 820 V		
Mesh sizing of FE model	Less than 5 mm		
Region size of FE model	Over 100%		

Table II: The comparison of different structures.

Structure	DCCB based on MS[17], [18], [19], [20], [21]	SSDCCB[24], [25], [26], [27]	HDCCB based on LCS[28]	HDCCB based on CCDC[29], [30]
Interruption time (*m*s)	7<*t*<12	t<3	3<t<4	3<t<5
Power loss in pre-fault	Low	Up to 30% nominal power	Up to 10% nominal power	Low
Arc-less	Operates with arc	Arc-less operation	Arc-less operation	Operates with arc
Ability to interrupt different rate of rise of fault current (peak of fault current)	Available (After multiple zero-crossings)	Available (Until the failure of semiconductor switches)	Available	Unavailable
Cooling system	Simple	Complex	Complex	Moderate
Comply with MS restrictions	Needed to be comply	Don’t have MS	Automatically comply by LCS	Needed to be comply

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