A Fractional-Order Meminductor Emulator with Applications in Chaotic Oscillator

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Abstract: This paper introduces a fractional-order meminductor emulator (FOMI) with both grounded and floating configurations, showcasing its applications in a chaotic oscillator. It employs one voltage differencing inverted buffered amplifier, a current follower, a fractional-capacitor, and a conventional capacitor. The transient analysis, pinched hysteresis loops, and non-volatile characteristics obtained for the suggested FOMI serve as clear indicators of the circuit's effective operation. The variations in pinched hysteresis loops with changes in the fractional-order (α) and frequency also support the theoretical concepts. The circuit's robust performance has been assessed by analyzing simulation results under varying conditions of temperature and supply voltage. The analysis also involves examining the impact of varying capacitor values on pinched hysteresis loops. Monte Carlo and corner analyses support the robust behaviour of the circuit. The suggested FOMI's potential use has been demonstrated using the chaotic oscillator circuit.

1. Introduction

The exploration of novel circuit components and architectures is a continuous pursuit in the field of electronic design, leading to advancements with applications across diverse disciplines. While traditional approaches focus on integer-order differentiation and integration, the potential of non-integer, or fractional-order, calculus has gained significant interest due to its ability to model real-world phenomena more accurately. This branch of mathematics, known as fractional calculus, offers greater flexibility by introducing the concept of fractional-order derivatives and integrals. Its impact has transcended boundaries, finding applications in various scientific and engineering fields, including material science, biology, and control theory [1].

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To take the advantages offered by fractional calculus, in circuit theory, fractional-order capacitors (FOCs) have been realized. These elements, denoted as C_α where α lies between 0 and 1, are also known as constant phase elements (CPEs). Their impedance characteristic, $1/s^\alpha C_\alpha$, introduces a constant phase shift of $-\alpha\pi/2$. However, due to the absence of readily available physical components exhibiting fractional-order behaviour, various techniques based on RC networks have been developed to approximate FOCs through continuous fraction expansion [2, 3]. Notably, Foster and Cauer networks utilize resistors and capacitors to achieve this approximation, with a trade-off between network complexity and accuracy. While higher-order networks provide better approximations, they also require more components. The foster form of fifth order is often realized with the help of six resistors and five capacitors.

The potential of fractional-order elements extends beyond capacitors, finding application in the recently discovered memristor. Unlike traditional capacitors and inductors that store energy, memristors possess the unique ability to store information, making them highly attractive for low-power neuromorphic computing applications. Their capability to retain and process information within a compact footprint further enhances their appeal. While conventional circuit components lack the captivating features of memristors, these were first envisioned by Prof. Leon Chua in 1971 [4] and eventually physically realized using Titanium dioxide (TiO2) by HP labs after a 37-year gap [5]. Today, they are readily available as commercial components. However, memristors' counterparts, memcapacitors and meminductors, are not yet widely available, prompting researchers and engineers to develop emulator circuits that replicate their expected characteristics. While numerous integer-order memcapacitor and meminductor emulator designs exist, research on their fractional-order counterparts remains scarce.

The motivation for this paper stems from this noticeable gap in research concerning fractional-order meminductors. In addition to the fact that fractional-order meminductors remain underexplored as compared to their integer-order counterpart, it has been analyzed that the existing fractional-order meminductor designs are often intricate, limiting their frequency responses to the kHz range. *This paper addresses this critical gap by introducing a simplified circuit for a FOMI with a superior frequency response.* Unlike existing fractional-order meminductors, the proposed design directs for a more straightforward architecture, ensuring broader applicability across broad frequency ranges. Beyond overcoming the

limitations of existing designs, the untapped potential of fractional order meminductors has been explored compared to their integer-order counterparts. Specifically, in chaotic circuits, fractional-order meminductors hold immense promise for generating complex dynamics and offering greater flexibility in controlling chaotic behavior. To achieve these objectives, a new design of meminductor emulator has been realized that leverages two well-established active building blocks: a voltage differencing inverted buffered amplifier (VDIBA) and a current follower (CF). Additionally, the design incorporates both a fractional-order capacitor and a conventional capacitor. The resulting circuit demonstrates robust performance, as verified through simulations conducted under varying temperature and supply voltage conditions. Finally, to showcase the versatility of the proposed fractional-order meminductor emulator (FOMI), its potential application in chaotic oscillator has been demonstrated.

A comparison summary of the suggested FOMI with existing ones are presented in Table 1. The observations of Table 1 are provided below:

1. For fractional meminductor emulators described in the literature [6-13], the greatest frequency for PHLs is restricted up to kHz only. In comparison, the suggested FOMI operates till 7MHz.
2. The suggested circuit is free from the requirement of memristors. This is in contrast to the known meminductor emulators [6], [7], and [12] that require memristors for their proper functioning.
3. The meminductor emulators [6], [11], and [13]) involve multipliers, active building blocks, along with a lot of passive components, nonetheless, the proposed FOMI has a fairly simple architecture and only requires a few components.

The content of the paper is arranged into seven sections which start from the first section of the introduction. The short review is given in Section 2 for the ease of readers. Section 3 presents the traits of active building blocks (ABBs) and their CMOS realizations. Section 4 discusses the operational concept and mathematical formulations of the proposed FOMI. Section 5 presents the simulation results. Applications of the proposed floating meminductor emulator namely chaotic oscillator is given in Section 6. Section 7 contains the paper's conclusion.

2. Short review of FOMI

Fractional meminductors extend the concept of traditional inductors and capacitors by incorporating fractional calculus principles. The application of fractional calculus principles

enables the analysis of time-domain behaviour and fractional-order dynamics, thereby enhancing modelling capabilities for these devices and offering potential solutions across a range of applications. In fractional calculus, the fractional derivative of a function is expressed in terms of the differentiation of non-integer order. Similarly, the fractional integral is an integration of non-integer order. FOMI is a device that exhibits memory effects in its current-flux relationship, similar to a traditional inductor, but with the inclusion of fractional-order derivatives. The FOMI's fractional nature enables it to capture more intricate and non-linear system behaviours. The FOMI can be tuned to have particular memory characteristics and frequency responses, allowing for more flexibility in system design and analysis.

The fractional derivative of a function $f(t)$ with respect to time t of order α, denoted by D_t^α, is defined using the Caputo or Riemann-Liouville fractional derivative operators. The Caputo fractional derivative operator is commonly used and is defined as follows:

$$D_t^\alpha f(t) = \frac{1}{\Gamma(n-\alpha)} \int_0^t \frac{f^{(n)}(\tau)}{(t-\tau)^{\alpha+1-n}} d\tau \tag{1}$$

where, $\Gamma(.)$ is gamma function and $n\text{-}1 \leq \alpha \leq n$ is the fractional order.

In the case of fractional meminductors, the fractional derivative term is incorporated into the constitutive relation between the current (I) and flux (φ) of the meminductor. The fractional-order derivative of current (I) with respect to time (t) is related to the fractional-order derivative of voltage (V) by a constant fractional-order meminductance (L^α) [14]:

$$I(t) = L^{-\alpha} \cdot D^{\alpha-1} V(t) \tag{2a}$$

here, $D^{\alpha-1}$ represents fractional derivative. Considering the fact that flux is time integral of voltage, Equation (2a) can be re-written as:

$$I(t) = L^{-\alpha} \cdot D^\alpha \varphi(t) \tag{2b}$$

The fractional order α, which controls the memory characteristics, frequency response, and dynamic behaviour of the device, affects the distinct characteristics and behaviour of fractional-order meminductors. The desired characteristics of meminductors can be attained by choosing suitable values for α.

3. Overview of ABBs

VDIBA and CF have been used in the designing of the proposed FOMI.

3.1 VDIBA

The VDIBA is a four-terminal amplifier, as illustrated in Fig. 1 (a). The positive and negative high-impedance input voltage terminals are denoted as V+ and V-, respectively. The output voltage terminal W- has a low impedance, while the intermediate terminal 'Z' exhibits high impedance. In terms of implementation, its input stage comprises an OTA with a differential input and a single output. This OTA converts the differential signal into a corresponding current at the 'Z' terminal. The voltage at the W- terminal of the output stage unity-gain inverting voltage buffer is the inverse of the voltage observed at the 'Z' terminal. An additional biasing terminal V_B can be used to control the transconductance parameter (G_m). Applications requiring resistor-less and electronically regulated circuits encourage the use of VDIBA because its G_m may be electronically controlled by a biasing voltage.

The equations defining the port characteristics of VDIBA are given as:

$$I_{V+} = I_{V-} = 0 \tag{3}$$

$$I_Z = G_m \left(V_{V+} - V_{V-} \right) \tag{4}$$

$$V_{W-} = -\beta V_Z \tag{5}$$

$$G_m = \frac{K}{2\sqrt{2}} \left(V_B - V_{SS} - 2V_{th} \right) \tag{6}$$

where K is a technological parameter and its value is given by $\mu_n \cdot C_{ox} \cdot W/L$, with μ_n representing the mobility of charge carriers, C_{ox} is per unit area capacitance due to the oxide layer, W is the width and L is the channel length of the symmetric MOSFETs constituting differential pair of OTA. V_{SS} is the negative supply voltage used for biasing of VDIBA and V_{th} is the threshold voltage of the MOSFETs that govern the gain of the amplifier. β denotes the gain of 'W-' terminal in the non-ideal case and is ideally unity. The CMOS circuit of VDIBA depicting all its port terminals is shown in Fig. 1 (b).

3.2 CF Block

The current at the output terminal follows the input current in a traditional CF, which has a low input impedance and a very high output impedance. The number of output terminals and their current polarity can be adjusted by using different combinations of current mirrors. The block diagram and CMOS circuit of a four-terminal CF are shown in Figs. 2 (a) and (b), respectively.

Here 'X' is a low-impedance input current port, Z_{1+} and Z_{2+} are two high-impedance output ports with positive current polarity, and Z- is a high-impedance output port with negative current polarity. The port equations describing the current at various ports of CF are given as:

$$V_X = 0 \tag{7}$$

$$I_{Z1+} = I_{Z2+} = \gamma \cdot I_X \tag{8}$$

$$I_{Z-} = -\gamma \cdot I_X \tag{9}$$

here, γ is the current gain of non-ideal CF and has a value equal to unity in case of the ideal output.

4. Proposed FOMI

Electronic components called fractional-order meminductors have fractional-order dynamics in terms of memory effects and nonlinearity. Fractional-order dynamics can offer greater flexibility and control for simulating memory effects in the context of meminductor emulators. The fractional meminductor emulator can simulate a variety of meminductive behaviours, including varied degrees of memory and nonlinearity, by varying the order of the fractional calculus operator. A few designs [6-13] are available for floating-order meminductors. It is well-known that fractional-order meminductor provides many advantages over integer-order meminductors such as better control over pinched hysteresis loops, complex chaos generation in chaotic oscillators for secure communication, and additional variable (α) available for controlling many circuit parameters, etc. Therefore, in this paper, a FOMI has been proposed. This meminductor is designed using VDIBA and CF as active blocks. Along with active blocks, the proposed emulator employs a fractional capacitor and a conventional capacitor. The fractional capacitor (C_α) is connected to VDIBA's 'Z' terminal to produce the fractional behaviour. The VDIBA is used in view of charging C_α and its internal buffer helps in copying the voltage generated at the 'Z' terminal to the 'W-' terminal. The proportional voltage produces a current I_X for the CF that is utilized to charge the capacitor C_2. The capacitor C_2 is used to remember the state of the circuit. The voltage across C_2 is further utilized to control the fractional meminductance of the proposed FOMI.

4.1 Proposed grounded FOMI

The complete circuit of the suggested grounded FOMI designed using VDIBA and CF has been presented in Fig. 3(a). The depiction of the Foster-I realization employed for the

implementation of C_α is illustrated in Fig. 3(b). The order of the RC network shows a significant compromise between the accuracy of the achieved fractional capacitor and the intricacy of the design. In the presented implementation, a 5th order RC network has been selected for the realization of the fractional capacitor. This choice has been governed by the fact that a 5th order Foster-I RC network offers a precise emulation of fractional capacitors across a broad frequency spectrum.

In the proposed meminductor of Fig. 3(a), the incremental configuration is obtained by connecting the V- terminal to the input and the V+ terminal to the ground (ⓐ → ⓓ and ⓑ → ⓒ). In order to obtain decremental configuration, the input is connected to V+ while V-terminal is grounded (ⓐ → ⓒ and ⓑ → ⓓ). The fractional capacitor C_α is charged by the voltage reflected at the 'Z' terminal. The 'X' terminal of the CF draws current from 'W-' and is reflected to 'Z_{1+}', 'Z_{2+}', and 'Z-' terminals. The capacitor C_2 is charged by the current drawn from 'W-' terminal. The voltage developed across C_2 biases the VDIBA and controls the transconductance G_m as per Equation (6). The feedback mechanism created by the charge stored at C_2 provides the basis for memory in this meminductor.

To verify the working of the circuit, a detailed mathematical analysis of the incremental meminductor is carried out as follows:

Using Equation (4) and analyzing from Fig. 3(a) that $V_{V-} = V_{in}$ and $V_{V+} = 0$, the expression obtained is:

$$I_Z = G_m\left(-V_{in}\right) \tag{10}$$

Using Equation (5), the voltage across C_α can be written in s-domain as:

$$V_Z(s) = \frac{1}{s^\alpha C_\alpha} \cdot I_Z = -\frac{G_m V_{in}}{s^\alpha C_\alpha} \tag{11}$$

where α is the fractional order of C_α.

Since, the flux at the input is represented as: $\phi_{in}(s) = \dfrac{V_{in}}{s}$, Equation (11) gets modified as:

$$V_Z(s) = \frac{-G_m}{s^{\alpha-1} C_\alpha} \cdot \varphi_{in}(s) \tag{12}$$

Direct analysis of Fig. 3(a) yields the current drawn by CF as:

$$I_X = \frac{V_{W-}}{R_1} \tag{13}$$

where R_1 is the parasitic resistance seen between 'W-' and 'X' terminals and is given as:

$$R_1 = R_{W-} + R_X I_X \tag{14}$$

here, R_{W-} and R_X denote the parasitic resistances at 'W-' and 'X' terminals, respectively.

The voltage across the capacitor C_2 $(V_{C2}(s))$ is given by:

$$V_{C2}(s) = V_B(s) = \frac{1}{s \cdot C_2} \cdot I_{Z2+} \tag{15}$$

Using Equation (8) and Equation (13), Equation (15) can be rewritten as:

$$V_B(s) = \frac{\gamma}{s \cdot C_2} \cdot \frac{1}{R_1} \cdot V_{W-} \tag{16}$$

Substituting V_{W-} from port Equation (5) and V_Z from Equation (12), Equation (16) can be expressed as:

$$V_B(s) = \frac{\gamma \cdot \beta \cdot G_m}{s^\alpha R_1 \cdot C_\alpha \cdot C_2} \cdot \varphi_{in}(s) \tag{17}$$

Since, $\frac{\phi_{in}}{s} = \rho(s)$, where $\rho(s)$ is the time domain integral of flux, Equation (17) can be redefined as:

$$V_B(s) = \frac{\gamma \cdot \beta \cdot G_m}{s^{\alpha-1} R_1 \cdot C_\alpha \cdot C_2} \cdot \rho(s) \tag{18}$$

The transconductance parameter (G_m) of VDIBA is dependent on biasing voltage V_B, as seen in Equation (6). Substituting value of V_B from Equation (18) in Equation (6) yields:

$$G_m(s) = \frac{K}{2\sqrt{2}} \left(\frac{\gamma \cdot \beta \cdot G_m}{s^{\alpha-1} R_1 \cdot C_\alpha \cdot C_2} \cdot \rho(s) - V_{SS} - 2V_{th} \right) \tag{19}$$

From Fig. 3(a), $I_{in} = -I_{Z+}$. Further combining Equations (5), (9), (12) and (13), we get:

$$I_{in}(s) = \frac{\gamma \cdot \beta \cdot G_m \cdot \varphi_{in}(s)}{s^{\alpha-1} R_1 \cdot C_\alpha} \tag{20}$$

Substituting the value of G_m from Equation (19) in Equation (20), yields:

$$I_{in}(s) = \frac{\gamma \cdot \beta}{s^{\alpha-1} R_1 \cdot C_\alpha} \frac{K}{2\sqrt{2}} \left(\frac{\gamma \cdot \beta \cdot G_m}{s^{\alpha-1} R_1 \cdot C_\alpha \cdot C_2} \cdot \rho(s) - V_{SS} - 2V_{th} \right) \cdot \varphi_{in}(s) \tag{21}$$

The relation between current and induced flux in meminductor in terms of meminductance (L_M) is given as:

$$I(s) = L_M^{-1} \cdot \varphi(s) \tag{22}$$

Considering Equations (21) and (22), the inverse meminductance of the proposed meminductor is expressed as:

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$$L_M^{-1} = \frac{\gamma \cdot \beta}{s^{\alpha-1} R_1 \cdot C_\alpha} \frac{K}{2\sqrt{2}} \left(\underbrace{V_{SS} + 2V_{th}}_{\text{fixed part}} - \underbrace{\frac{\gamma \cdot \beta \cdot G_m}{s^{\alpha-1} R_1 \cdot C_\alpha \cdot C_2} \cdot \rho(s)}_{\text{variable part}} \right) \qquad (23)$$

where α is fractional order, β is the voltage gain of VDIBA and γ is the current gain of CF. Equation (23) shows that the meminductance of the proposed meminductor can be controlled by fixed parameters (supply voltage and threshold voltage) and variable parameters (input flux). The fractional power (α) helps in precise control of the meminductance. The circuit shown in Fig. 3 (a) can be used in decremental mode by connecting ⓐ → ⓒ and ⓑ → ⓓ. A similar mathematical analysis as carried out for incremental configuration, yields meminductance for decremental configuration as:

$$L_M^{-1} = \frac{\gamma \cdot \beta}{s^{\alpha-1} R_1 \cdot C_\alpha} \frac{K}{2\sqrt{2}} \left(\underbrace{V_{SS} + 2V_{th}}_{\text{fixed part}} + \underbrace{\frac{\gamma \cdot \beta \cdot G_m}{s^{\alpha-1} R_1 \cdot C_\alpha \cdot C_2} \cdot \rho(s)}_{\text{variable part}} \right) \qquad (24)$$

From Equation (24) it can be observed that both fixed and variable components are negative, leading to decremental behaviour of the proposed fractional meminductor.

4.2 Proposed floating FOMI

The suggested floating type FOMI is shown in Fig. 4. When the circuit of Fig. 4 is subjected to the same mathematical analysis that was done for the grounded type, the relationship obtained between flux and current for incremental configuration is provided below:

$$L_M^{-1} = \frac{\gamma \cdot \beta}{s^{\alpha-1} R_1 \cdot C_\alpha} \frac{K}{2\sqrt{2}} \left(\underbrace{V_{SS} + 2V_{th}}_{\text{fixed part}} + \underbrace{\frac{\gamma \cdot \beta \cdot G_m}{s^{\alpha-1} R_1 \cdot C_\alpha \cdot C_2} \cdot \rho(s)}_{\text{variable part}} \right) \qquad (25)$$

By flipping the switch as indicated in the figure, the proposed emulator shows decremental behaviour and its meminductance can be expressed as:

$$L_M^{-1} = -\frac{\gamma \cdot \beta}{s^{\alpha-1} R_1 \cdot C_\alpha} \frac{K}{2\sqrt{2}} \left(\underbrace{V_{SS} + 2V_{th}}_{\text{fixed part}} + \underbrace{\frac{\gamma \cdot \beta \cdot G_m}{s^{\alpha-1} R_1 \cdot C_\alpha \cdot C_2} \cdot \rho(s)}_{\text{variable part}} \right) \qquad (26)$$

In the proposed FOMI, Equations (23) to (26) show that the fractional s-domain factor of $s^{\alpha-1}$ offers greater flexibility in modelling complex systems. This aids in capturing a broader range of system behaviours that integer-order models are unable to faithfully capture. Additionally, it offers greater accuracy and increased adaptability in simulating real-world

systems, particularly those displaying non-linear and non-integer behaviours. However, fabricating such emulators with precise fractional-order characteristics is a complex task, leading to increase in manufacturing costs. Additionally, fractional-order circuits are generally more sensitive to variations in component values compared to their integer-order counterparts. Even minor discrepancies in resistance, capacitance, or other parameters can significantly affect the behaviour of the emulator, posing challenges in practical implementations. Furthermore, commercially available components specifically designed for fractional-order circuits are limited compared to those readily available for integer-order circuits. Furthermore, existing circuit design methodologies, simulation tools, and standard components are primarily tailored for integer-order circuits making the analysis of these circuits a challenging task.

5. Simulation results

Simulations using the LTspice tool have been performed to test the operation of the proposed fractional-order meminductor circuit. The blocks VDIBA, and CF have been simulated with supply rails of ±0.9V utilizing TSMC's 180nm technology parameters. Table 2 displays the size of the MOSFETs utilized in the active blocks. The capacitance value C_2 is set to 10 pF in order to achieve pinched hysteresis lobes. A fifth-order Foster-I form is used to implement C_α linked to the 'Z' terminal of VDIBA, as displayed in Fig. 3(b). The values of R and C for the Foster-I form have been calculated using MATLAB [15]. These values for $C_\alpha = 10pF$, for different values of α have been presented in Table 3. Unless otherwise stated, all the simulated results have been plotted with $α = 0.5$ for the sake of simplicity.

5.1 Simulation results of proposed floating FOMI in incremental configuration

The curves representing transient analysis of the proposed floating FOMI for $α = 0.5$, plotted with a 100kHz sinusoidal signal have been displayed in Fig. 5. This analysis reveals intricate details of the proposed floating FOMI's temporal behaviour showcasing the unique relationship between voltage, flux, and current waveforms. In this figure it can be observed that the voltage waveform leads the flux and current waveforms. This is a characteristic that is observed in inductive circuits. The non-sinusoidal nature of the current waveform is attributed to the dynamic fluctuations in the inductance value over time, providing a comprehensive understanding of the circuit's transient response. To check the non-volatile behaviour of the proposed emulator, a step signal with 15μs period and 1μs ON time is

applied at the input terminal and the observed response is shown in Fig. 6. The figure illustrates a key aspect of the emulator's behavior. Specifically, during the ON time of the step signal, the emulator's meminductance value increases. Meminductance is a property similar to inductance but with memory effects, implying that the device "remembers" its previous states. What is particularly noteworthy is that when the pulse train is turned OFF, the emulator retains its meminductance value from the previous ON state. This persistence of the meminductive property during the OFF state demonstrates the non-volatile behaviour of the proposed emulator. This ensures that the emulator has the ability to "remember" and maintain its meminductive state even after the input signal is no longer actively applied. This characteristic is a crucial element of non-volatile memory, where information or states persist even in the absence of power or input stimuli.

To understand the behaviour of the circuit across different frequency ranges, sinusoidal signals with varying frequencies are applied. The corresponding hysteresis loops obtained are presented in Figs. 7(a) and 7(b). Fig. 7(a) displays the PHL curves obtained for frequencies ranging from 1kHz to 7kHz. In this figure, the curves are plotted with frequency varying in steps of 2kHz. Fig. 7(b) demonstrates the curves for frequency varying from 1MHz to 7MHz in steps of 2MHz. The capacitance of C_2 has been suitably modified to produce PHL curves with zero-crossing for the given range of frequencies. An additional crucial aspect of a meminductive device is the PHL lobes' area decreasing with frequency. This characteristic can be effectively visualized in the PHL curves shown in Fig. 7.

Additionally, to explore the maximum operating frequency of the proposed FOMI, the circuit underwent testing with high-frequency sinusoidal signals. Fig. 8 displays the results analyzed for an input signal of 10MHz frequency for different values of the fractional order parameter ($\alpha = 0.2$, 0.5, and 0.8). As evident from the figure, PHL curves for all tested α values exhibit the dumbbell hysteresis shape, confirming the FOMI's functional operation even at a high frequency of 10 MHz. However, these curves are observed with slight shift in pinched point.

5.2 Simulation results of proposed floating FOMI in decremental configuration

The proposed floating FOMI presented in Fig. 4 is simulated in decremental mode. The circuit behaved satisfactorily, as shown by the results of the non-volatility test and transient analysis. The PHL curves observed for a sinusoidal signal with frequency varying from 100kHz to 7MHz are depicted in Fig. 9. All these curves have been plotted for $\alpha = 0.5$. From Fig. 9, it can be visualized that the size of the lobes reduces as frequency increases, this

confirms the satisfactory behaviour of the proposed emulator in the complete range of frequencies for the decremental mode of configuration.

To analyze the effect of the variations in α on PHL curves, the circuit has been simulated for $α$ varying from 0.2 to 0.8 under the stimulation of a sinusoidal voltage signal. The curves obtained are displayed in Fig. 10. The slight modifications in the shape of loop demonstrate the control of the fractional order in meminductance of the designed emulator.

5.3 Simulation results of the proposed grounded FOMI

In the presented grounded FOMI circuit illustrated in Fig. 3, a sinusoidal signal with a phase difference of 90^0 has been applied at the input. This sinusoidal input serves as a dynamic stimulus to assess the performance of the grounded FOMI across a range of frequencies. The frequency of the applied signal has been systematically varied, spanning from 100kHz to 7MHz. For the evaluation of the meminductive behaviour under these varying frequencies, the R and C values are configured according to the Foster-I form with a specific fractional order, in this case, $α = 0.5$. This choice of α is significant, as it represents a balanced fractional order that influences the circuit's meminductive characteristics.

The resulting responses of the grounded FOMI are captured in curves presented in both Fig. 11 and Fig. 12. Fig. 11 illustrates the behaviour in the incremental mode, where the meminductive response is observed during the increasing phase of the applied signal. On the other hand, Fig. 12 displays the response in the decremental mode, focusing on the meminductor's behaviour during the decreasing phase of the signal. These curves validate the proper functioning of the proposed grounded meminductor across the entire frequency range for both incremental and decremental configurations. The fact that the curves exhibit consistent and reliable behaviour throughout this frequency spectrum affirms the robustness and effectiveness of the grounded FOMI circuit.

5.4 Analysis of the proposed meminductor subjected to environmental conditions

In reality, a device will experience a variety of non-ideal environmental and manufacturing conditions, which will affect its behaviour. It is necessary to analyze a device's characteristics, when subjected to practical conditions, to determine its tolerance in a real-world environment. In this section, the impact of the variations of various parameters on the behaviour of the proposed FOMI has been investigated.

5.4.1 Temperature variation analysis

The performance characteristics of the proposed meminductor have been thoroughly investigated by examining its behaviour across a temperature range spanning from -50°C to +50°C. The analysis involves the generation of PHL curves for the floating FOMI under both incremental and decremental configurations. The outcomes of this investigation are represented in Fig. 13(a) for incremental mode and Fig. 13(b) for decremental mode.

In these figures, the meminductor's behaviour is assessed for $\alpha = 0.5$, a choice that represents a balanced configuration for the meminductor. The PHL curves plotted in these figures depict the slight deviations in the meminductive response under varying temperatures.

The observed slight deviations in the PHL curves do not compromise the overall operation of the proposed meminductor. Instead, they confirm the meminductor's ability to maintain functionality and stability across a defined temperature span. This resilience is indicative of the suggested meminductor's capability to withstand temperature variations without substantial impact on its performance, making it a reliable and robust component for applications that may be subjected to temperature fluctuations within the specified -50°C to +50°C range.

5.4.2 Supply voltage variations

The impact of supply voltage variations on the performance of the proposed FOMI has been systematically examined by subjecting the circuit to an approximate 10% fluctuation in the supply voltage. The resulting PHL curves, obtained by simulating the suggested meminductor with a sinusoidal signal of 100 kHz frequency and $\alpha = 0.5$, are presented in Fig. 14. The depicted waveforms in Fig. 14 illustrate the PHL curves in the φ vs. i plane, showcasing the meminductive response to variations in supply voltage. Specifically, the curves are generated for supply voltage fluctuations ranging from 0.81V to 0.99V for V_{DD} and from -0.81V to -0.99V for V_{SS}.

Despite the variations in supply voltage within the specified range, the suggested meminductor demonstrates satisfactory performance. The observed PHL curves reveal only slight modifications in lobe shape, indicating that the meminductive behavior remains stable even under supply voltage variations of 10%.

5.4.3 Variations due to capacitance tolerance:

During the fabrication process, achieving exact component values is often an impossible task. In reality, component values are inherently prone to certain tolerances or variations, which can potentially lead to circuit failure or suboptimal performance. Recognizing this inherent variability, an examination of the suggested meminductor's behaviour in the φ vs. i plane has been conducted by varying capacitor values. This investigation aims to understand how fluctuations in capacitance values influence the meminductive response.

Fig. 15 visually presents the PHL curves for the floating FOMI for both incremental and decremental configurations. These curves are generated for different values of capacitance, where C_2 is set at 5pF, 10pF, and 20pF. This variation in capacitance values provides insight into how the meminductive behaviour adapts to different component tolerances.

5.4.4 Monte-Carlo Analysis:

In the practical development of a MOSFET-based circuit, factors such as the aspect ratio and threshold voltage of the MOSFET can undergo variations due to fabrication imperfections. To assess the impact of these variations on the properties of the proposed meminductor, Monte Carlo (MC) analysis has been employed. The Gaussian distribution function has been used to perform the MC analysis with 5% variations in the MOSFET's aspect ratio and threshold voltage. Figs. 16 (a) and 16 (b) show the MC plots of PHL curves for a 100 kHz sinusoidal signal, considering threshold modifications for incremental and decremental meminductors, respectively. Each curve in these figures represents the outcome of the MC analysis for a specific run, with a total of 100 runs being conducted. These MC plots serve to demonstrate the robustness of the proposed circuit's meminductive behaviour across a range of mismatch scenarios.

The observed PHL curves in the MC plots affirm the circuit's ability to maintain meminductive functionality over the entire range of mismatch induced by variations in MOSFET specifications. Despite the inherent variations in the aspect ratio and threshold voltage, the form of the PHL curves remains consistent, with only minor modifications. This resilience is crucial for real-world applications where fabrication-induced variations are inevitable, ensuring that the proposed meminductor reliably preserves its intended behaviour despite variations in MOSFET properties.

5.5 Quantification of error in fractional-order capacitance using Foster-I form

As mentioned in Section 1, commercially available fractional capacitors are not readily accessible. Hence various continuous fraction expansions utilizing RC networks have been proposed in the literature to approximate their values. The s-domain equation that characterizes the impedance of a CPE is expressed as follows [15]:

$$Z(s) = \frac{1}{C_\alpha s^\alpha} \qquad (27)$$

here, C_α represents normalized capacitance expressed in Farad/sec$^{(1-\alpha)}$ (F/sec$^{(1-\alpha)}$). The value of this capacitor which depends both on frequency and order, is represented as:

$$C_\alpha = C\omega_0^{1-\alpha} \qquad (28)$$

where, C is the capacitance value for which the fractional capacitor is designed. The phase (θ) of the impedance $Z(s)$ of CPE is expressed as:

$$\theta = -\alpha\pi/2 \qquad (29)$$

In this paper, a fifth-order Foster-I network has been employed to realize the fractional capacitor (C_α) required in the proposed design. There exists a trade-off between the network order and the exact value of fractional impedance. The 5th order network was chosen in this work, as it enables the attainment of a highly accurate value of fractional capacitor impedance across several decades centered around the central frequency.

In this work, a capacitance $C=10$pF centred at $f_0 = 100$ kHz ($/Z/ = 159.15$kΩ) has been chosen for the realization of the fractional capacitor through 5th order Foster-I form. The impedance of the fractional capacitor, implemented using the network illustrated in Fig. 3(b) with the component values specified in Table 3, have been examined. The resulting impedances for various values of alpha are plotted in Fig. 17(a). In this figure, the impedance corresponding for $\alpha = 0.2, 0.4, 0.6$ and 0.8 have been plotted for a frequency range of 10^3 Hz to 10^7 Hz (4 decades). The waveforms depicting % error as compared to the impedance obtained through Equation (27) have been plotted in Fig. 17(b). These waveforms show that near centre frequency, the 5th order Foster-I form accurately realizes the fractional capacitance. The error in impedance magnitude is almost negligible in the frequency range of 20kHz to 500kHz and increases beyond this range.

The waveforms showing phase response of fractional capacitance realized through Foster-I RC network and the corresponding error related to different values of α have been plotted in Fig. 18(a) and 18(b) respectively. These plots have also been drawn for a frequency range of 4 decades (10^3 Hz to 10^7 Hz). Fig. 18(b) depicts that error in phase response is almost negligible for 2 decades of frequency variation (from 10kHz to 1MHz).

Figs. 17 and 18 confirm the validity of the 5th order Foster-I RC network for implementing the desired fractional capacitor.

6 Applications of the suggested FOMI as a chaotic oscillator

This section introduces a chaotic oscillator implemented using the proposed FOMI. The incorporation of FOMI in chaotic oscillator design introduces additional degrees of freedom, resulting in more intricate and diverse dynamical behavior. The fractional order, denoted by 'α', offers precise control over the system's dynamics, facilitating customization of the oscillator's behavior to meet specific requirements [14, 16]. Despite the advantages of fractional-order chaotic oscillators, including richer dynamics and enhanced controllability, their implementation entails increased complexity and challenges.

In the suggested implementation of Chua's oscillator, the fractional order model is exclusively applied to the meminductor flux characteristic, while the remaining states are maintained as integer order. Fig. 19 illustrates the basic configuration of Chua's oscillator, where the traditional nonlinear element (M_L) is replaced with the proposed VDIBA and CF based meminductor. The oscillator includes one inductor (L), two capacitors (C_1 & C_2), a resistor (R_1), an OPAMP-based negative impedance converter ($-R_2$), and one meminductor (M_L).

The four state variables of this oscillator are: current through the inductor (I_L), the capacitor node voltages (V_X & V_Y), and flux (φ_{MI}) and integral of flux (ρ_{MI}) of meminductor. This meminductor-based oscillator's state space dynamics can be expressed with the help of 1st order differential equations as shown below:

$$\left.\begin{aligned}
C_A \frac{dV_X}{dt} &= \frac{V_X}{R_B} - I_L \\[4pt]
C_B \frac{dV_Y}{dt} &= I_L - I_{ML} \\[4pt]
L \frac{dI_L}{dt} &= V_X - V_Y - I_L \cdot R_B \\[4pt]
\frac{d\varphi_{MI}}{dt} &= V_Y \\[4pt]
\frac{d\rho_{MI}}{dt} &= \varphi_{MI}
\end{aligned}\right\} \tag{30}$$

In above analysis, C_A, C_B, L, R_A and R_B represent the values of the respective elements (capacitance, inductance, or resistance) in the chaotic oscillator. To model the current through the meminductor, the equation $I_{LM} = (A + B\rho_{MI})\varphi_{MI}$, as derived in Equation (21), can be employed. In this equation, α is considered to be equal to unity for the sake of simplicity ($\alpha = 1$ for an ideal capacitor). Under this assumption, the parameters A and B are characterized by Equation (31).

$$A = \frac{\gamma \cdot \beta}{R_1 \cdot C_\alpha} \frac{K}{2\sqrt{2}}\left(V_{SS} + 2V_{th}\right)$$
$$B = \frac{\gamma^2 \cdot \beta^2}{R_1^2 \cdot C_2 \cdot C_\alpha^2} \cdot \frac{K \cdot G_m}{2\sqrt{2}}$$

(31)

A set of equilibrium points can be derived by setting all derivatives of Equation (30) equal to zero. This set of equilibrium points considering, $\dot{V}_X, \dot{V}_Y, \dot{I}_L, \dot{\varphi}_{MI}, \dot{\rho}_{MI} = 0$, is defined as:

$$E = \left\{ \left(V_X, V_Y, I_L, \varphi_{MI}, \rho_{MI}\right) \mid V_X = V_Y = I_L = \varphi_{MI} = 0, \rho_{MI} = m \right\}$$

(32)

where, m is a constant real number. At equilibrium point given by Equation (32), the Jacobian matrix (J) is defined as:

$$J = \begin{bmatrix} \frac{1}{C_A R_B} & 0 & -\frac{1}{C_A} & 0 & 0 \\ 0 & 0 & \frac{1}{C_B} & -\frac{1}{C_B}(A+Bm) & 0 \\ \frac{1}{L} & -1 & \frac{-R_A}{L} & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

(33)

The dynamics of the Chua's oscillator (Fig. 19) can be analyzed by finding the characteristic equation associated with the Jacobian matrix expressed Equation (33). This equation which gives the eigenvalues of the matrix is defined as:

$$Det\left(J - \lambda I\right) = 0$$

(34)

here, λ represents the eigenvalues and are crucial for determining the stability of the Chua's oscillator at the equilibrium point specified by Equation (32). Using MATLAB, the eigenvalues of the system are calculated as:

$$\lambda^5 + a_1\lambda^4 + a_2\lambda^3 + a_3\lambda^2 + a_4\lambda = 0$$

(35)

here, coefficients a_1, a_2, a_3, and a_4 are defined by Equation (36).

$$a_1 = \frac{R_A}{L} - \frac{1}{C_A R_B}$$
$$a_2 = \frac{1}{C_B}(1 + A + Bm) + \frac{1}{C_A L}\left(1 - \frac{R_A}{R_B}\right)$$
$$a_3 = \frac{1}{C_B}\left\{(A+Bm)\left(\frac{R_A}{L} - \frac{1}{C_A R_B}\right) - \frac{1}{C_A R_B}\right\}$$
$$a_4 = \frac{1}{C_A C_B L}(A+Bm)\left(1 - \frac{R_A}{R_B}\right)$$

(36)

Using the characteristic equation given by Equation (34), the eigen values can be obtained for the chaotic circuit of Fig. 19. From Equation (35), it can be easily realized that Jacobian matrix 'J' has a zero value and four nonzero values. Since, the coefficients a_1, a_2, a_3, and a_4 are all nonzero, if the real parts of all eigenvalues of Equation (35) (except $\lambda = 0$) are negative, the system is stable. As per Routh–Hurwitz criterion the system is stable only when, $\Delta_1 = a_1$, $\Delta_2 = (a_1 a_2 - a_3)/a_1$, $\Delta_3 = a_3-(a_1^2 a_4)/(a_1 a_2 - a_3)$, and $\Delta_4 = a_4$, all are positive. Otherwise, the system is unstable, and chaotic response can be generated. Fractional-order systems exhibit significantly more complex behavior than their integer-order counterparts due to the challenging nature of fractional-order calculus. The previous analysis was conducted assuming an ideal capacitor with $\alpha = 1$. Interestingly, when considering a fractional capacitor ($0 < \alpha < 1$), the chaotic behavior remains at least as stable as the integer-order system [17]. However, maintaining chaos in the fractional system depicted in Fig. 19 requires the same number of eigenvalues to remain within the unstable region. The essential condition to achieve unstable eigenvalues is outlined below:

$$\alpha > \frac{2}{\pi} \tan^{-1}\left(\frac{|\text{Im}(\lambda)|}{\text{Re}(\lambda)} \right) \tag{37}$$

The behavior of the chaotic oscillator, as illustrated in Fig. 19 and implemented with the recommended fractional-order meminductor with $\alpha = 0.5$, has been explored through LTspice simulations. The negative resistance ($-R_2$) is achieved by the OPAMP-based negative impedance converter when $R_a = R_b = 2\text{k}$. The rest of the elements are set to have the following values: L=120mH, C_1=65nF, C_2=10nF, and R_1=200. Fig. 20 shows the 2-D projection plots that are observed for the different state variables. These plots validate the chaotic dynamics exhibited by the system when utilizing fractional values of α.

7   Conclusion

In this paper, the feasibility of designing grounded/floating FOMI based on a few active blocks has been investigated. VDIBA and CF blocks have been selected for their straightforward construction, differential capabilities, and inherent tuning options. Verification tests, including meminductor fingerprints, PHL with zero-crossing, and non-volatility tests, have all been employed to ensure the intended functionality of the proposed circuit. The circuit's ability to operate in both incremental and decremental modes was demonstrated using a simple switch connected to the input terminals. LTspice simulation results indicate the circuit's effectiveness up to 7MHz. Temperature variations (-50°C to

+50°C), capacitance changes (5pF to 20pF), and supply voltage fluctuations (10%) were considered in PHL curves, affirming the circuit's practicality in real-world scenarios. Additionally, the proposed fractional-order meminductor's realization was validated through a Monte Carlo study. The paper illustrates the successful implementation of a chaotic oscillator using the suggested fractional-order floating meminductor emulator.

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Fig. 13 PHL curves of proposed floating FOMI (a) incremental (b) decremental configuration for temperature fluctuations from -50^{0}C to 50^{0}C

Fig. 14 PHL curves of the proposed FOMI for (a) floating incremental (b) floating decremental observed with $\pm$10% deviations in supply voltage

Fig. 15. PHL curves of the proposed floating FOMI observed for deviations in C_2 for (a) incremental (b) decremental configuration

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Fig. 17 Waveform corresponding to α = 0.2, 0.4, 0.6 and 0.8 for (a) Magnitude of impedance realized using 5th order Foster-I form (b) % error in the magnitude of fractional capacitor impedance

Fig. 18 Waveform corresponding to α = 0.2, 0.4, 0.6 and 0.8 for (a) Phase response of impedance realized using 5th order Foster-I form (b) % error in the phase response of fractional capacitor impedance

Fig. 19. A fourth-order Chua's chaotic oscillator

Fig. 20 Projection plots of chaotic oscillator observed between space variables (a) V_X & I_L (b) V_X & I_{ML} (c) V_Y & V_X (d) V_Y & I_L

List of Table Captions:

Table 1 Comparison of the suggested FOMI with existing meminductor emulators
Table 2: Aspect Ratios of MOSFETs
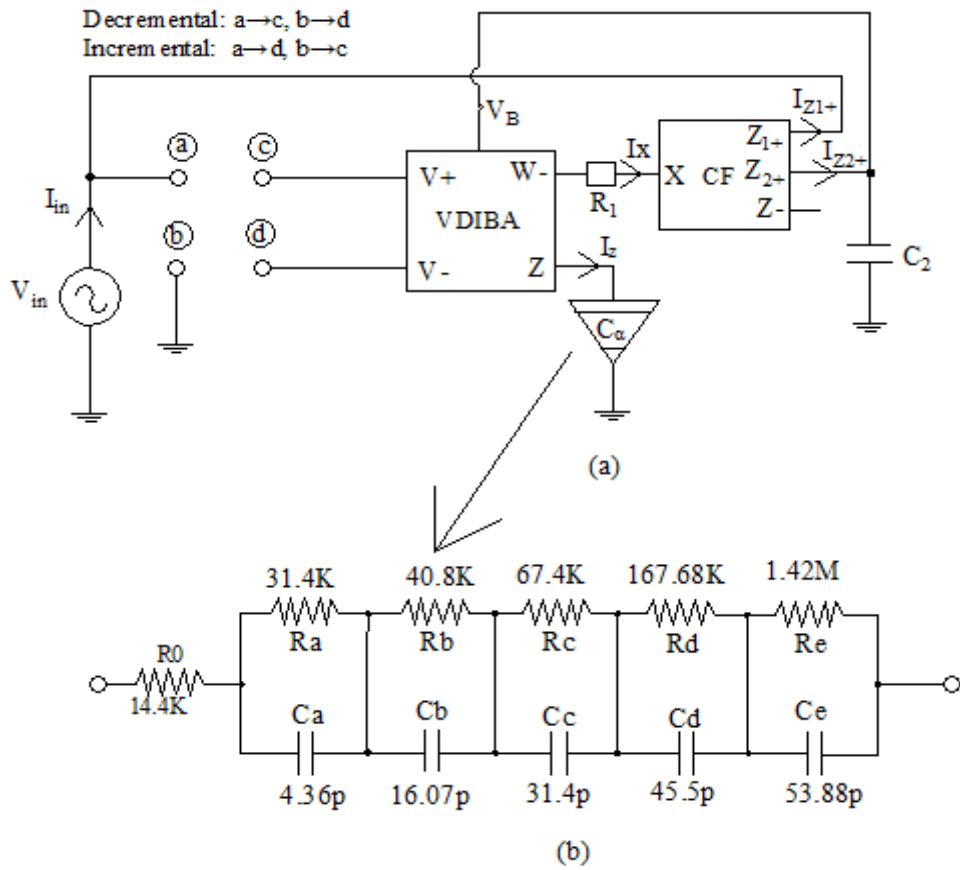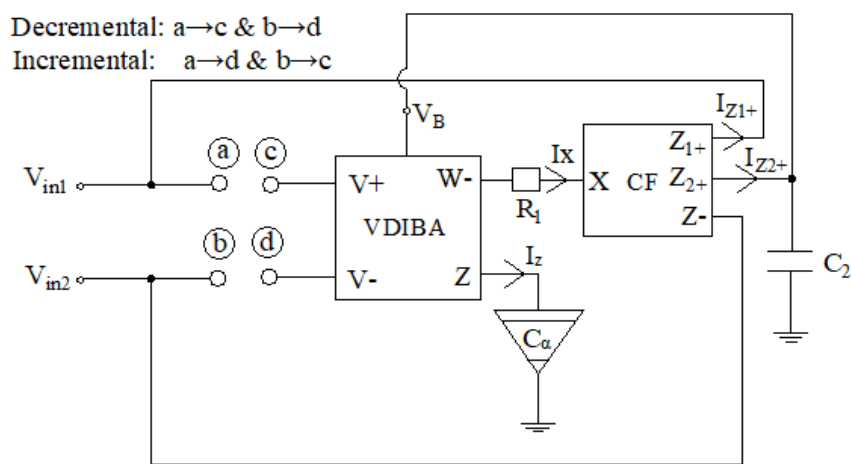Table 3: R and C values for Foster-I form for various values of α

Figures:

| | (a) | | (b) |
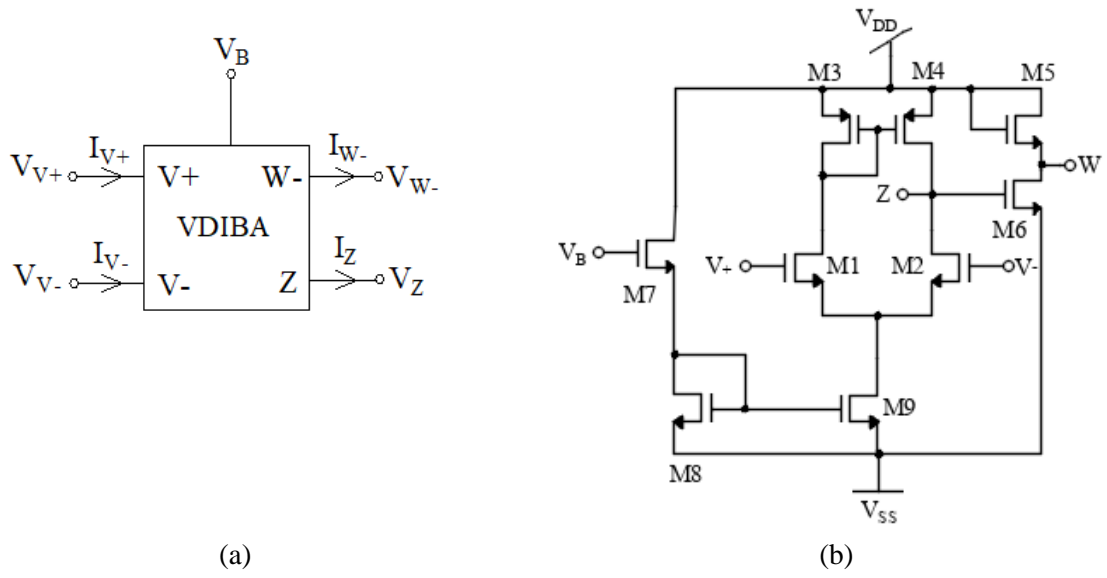
Figure 2. VDIBA (a) Symbol (b) Circuit diagram

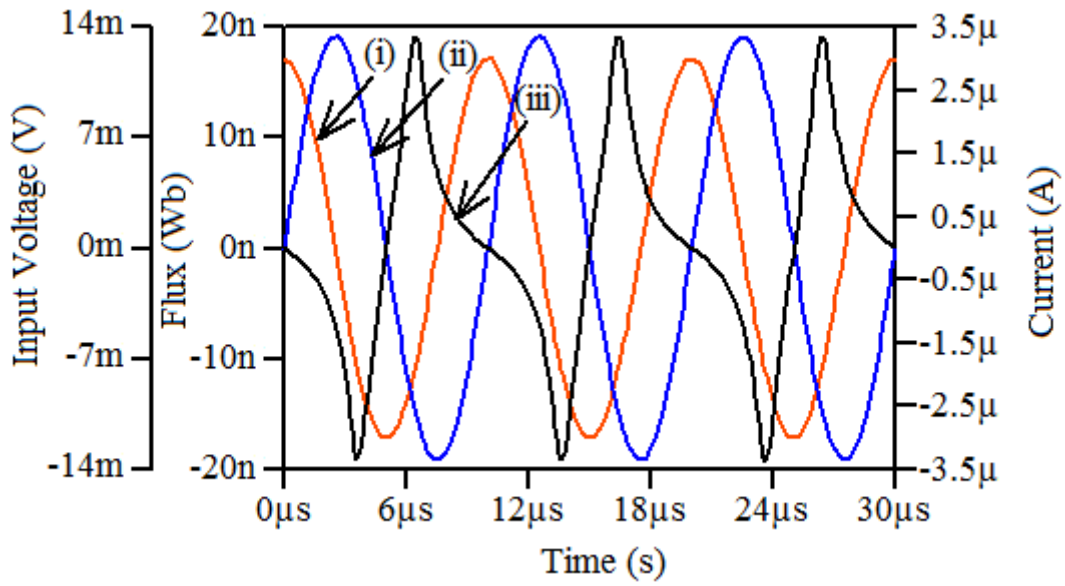| | (a) | | (b) |
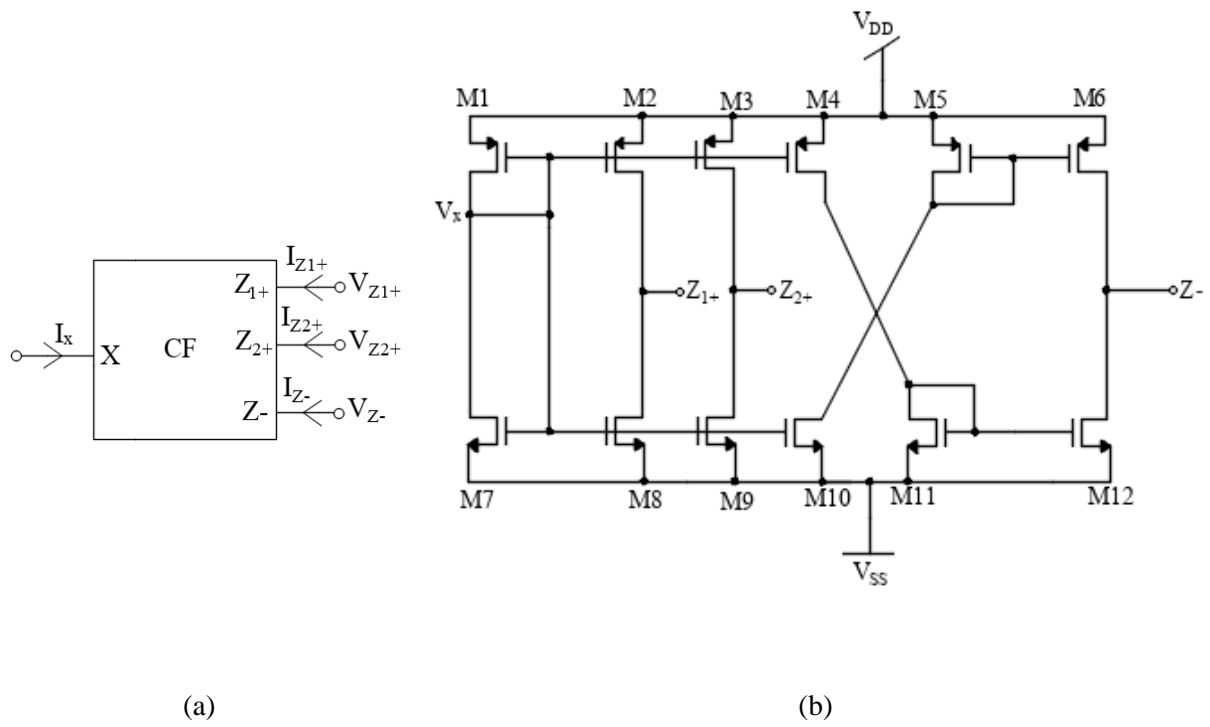
Figure 2. CF (a) Symbol (b) Circuit diagram

Figure 3. Proposed Grounded FOMI (a) Circuit diagram (b) Foster-I realization of fractional capacitor for $\alpha = 0.5$
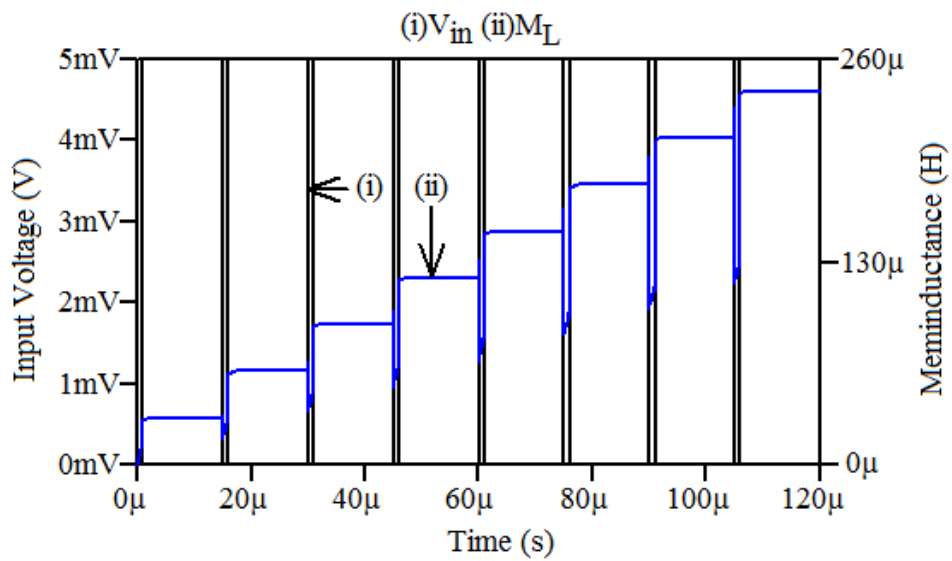

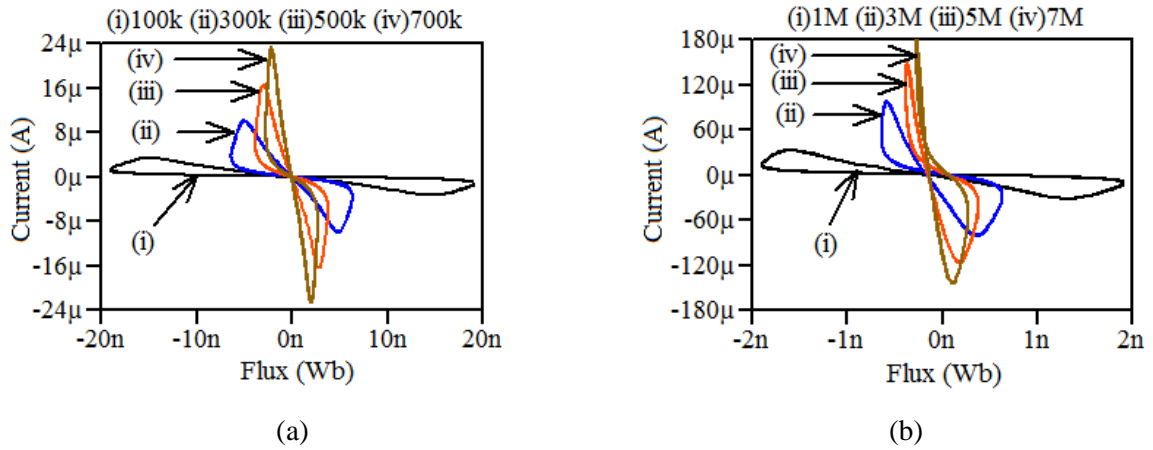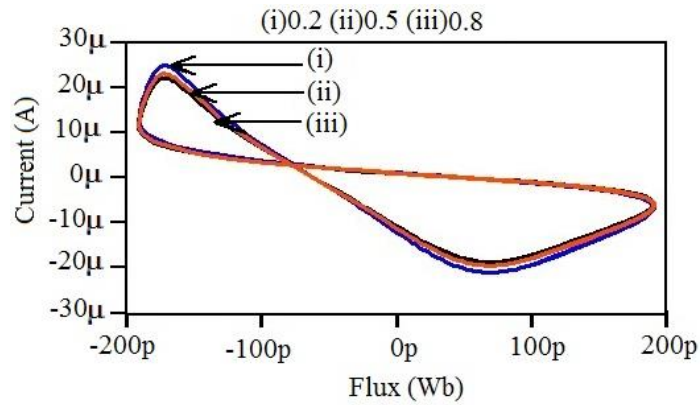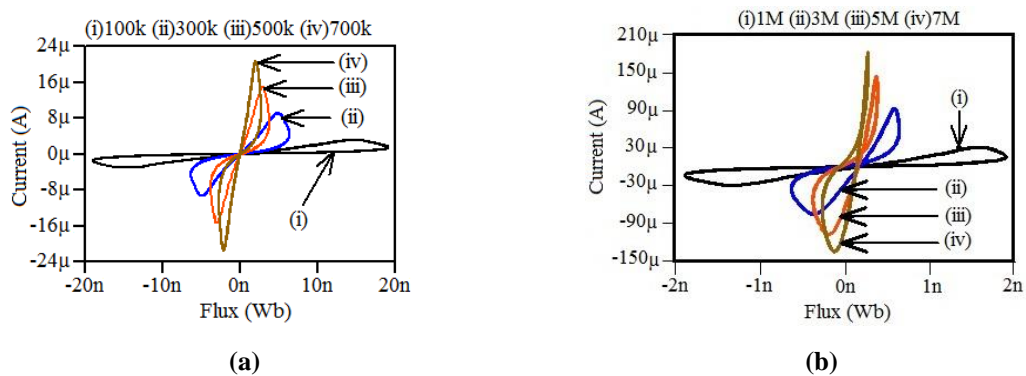**Figure 4.** Proposed Floating Decremental/Incremental FOMI

Figure 5. Transient analysis for the floating FOMI incremental configuration for a sinusoidal frequency of 100kHz for α = 0.5

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Figure 6. Non-volatile behavior of the proposed floating FOMI for α = 0.5
for color reproduction on the Web

Figure 7. PHL curves observed for the floating incremental FOMI for α = 0.5 for a frequency range of (a) 1kHz to 7kHz (b) 1MHz to7MHz

for color reproduction on the Web

Figure 8. PHL curves observed for 10MHz sinusoidal signal for α = 0.2, 0.5 and 0.8
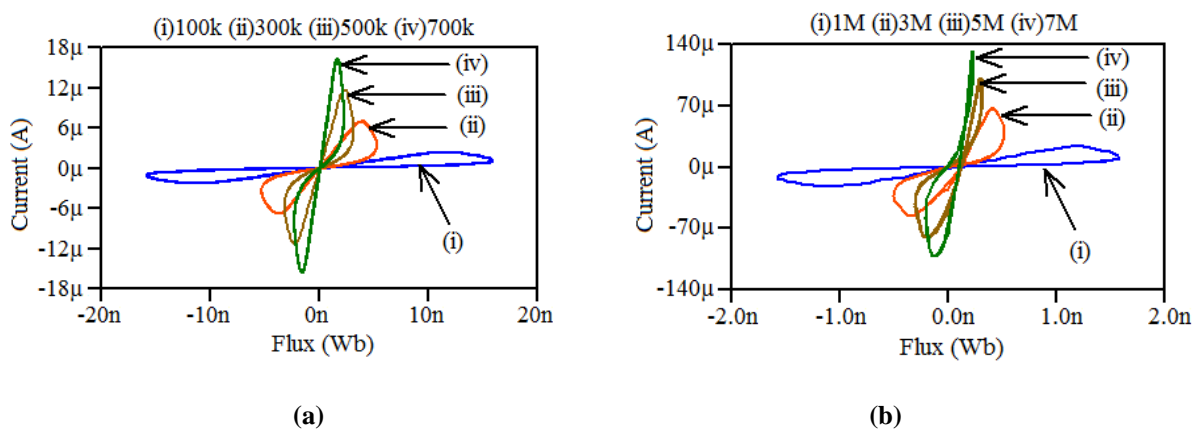
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Figure 9. PHL curves observed for the proposed floating decremental FOMI with α = 0.5 for a frequency range of (a) 100kHz to 700kHz (b) 1MHz to 7MHz
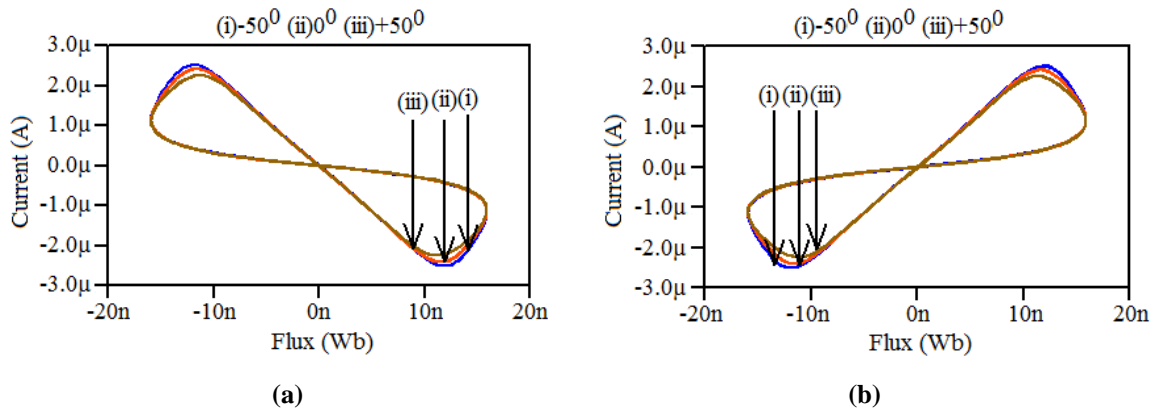
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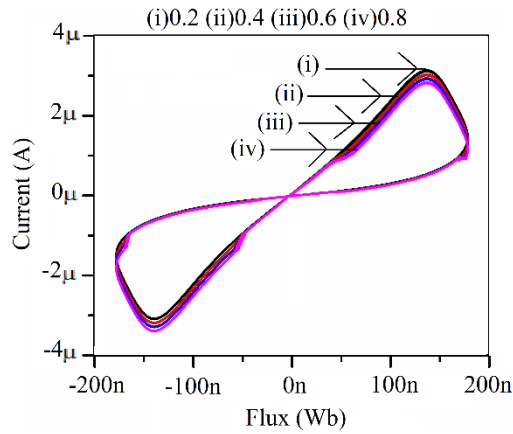
Figure 10. PHL curves observed for decremental floating FOMI for $\alpha = 0.2$ to 0.8

for color reproduction on the Web

(a)   **(b)**
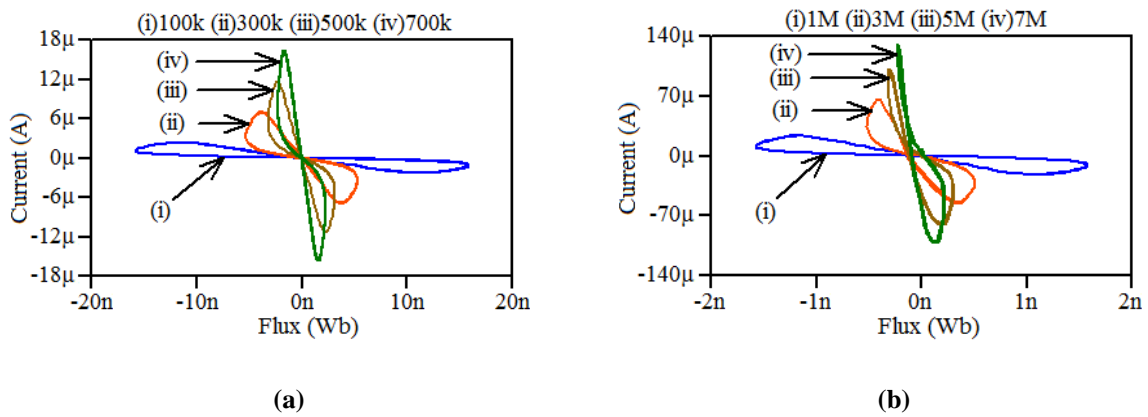
Figure 11. PHL curves observed for the incremental FOMI with $\alpha = 0.5$ for a frequency range of (a) 100kHz to 700kHz (b) 1MHz to7MHz

for color reproduction on the Web

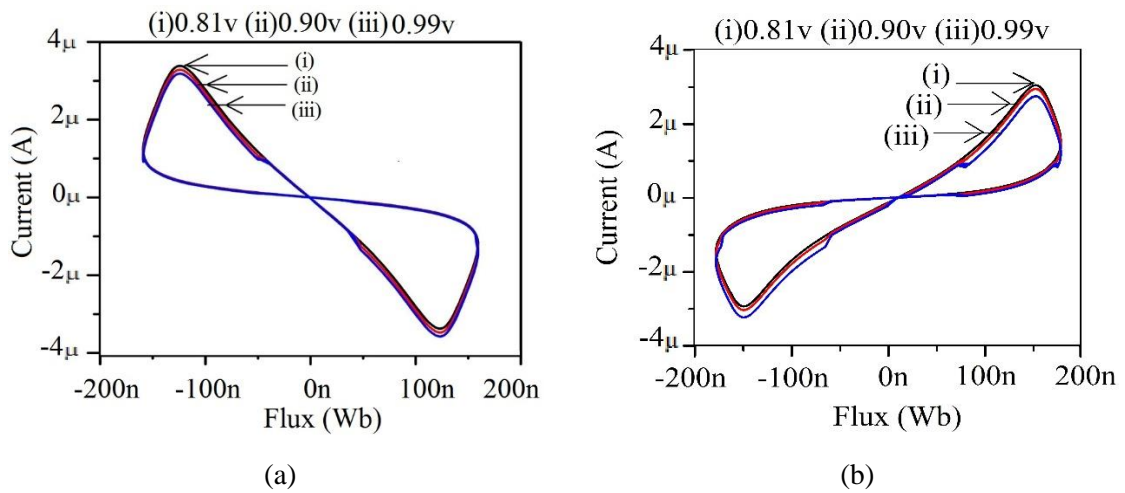**(a)**   **(b)**

Figure 12. PHL curves observed for the grounded decremental FOMI with $\alpha = 0.5$ for a frequency range of (a) 100kHz to 700kHz (b) 1MHz to7MHz
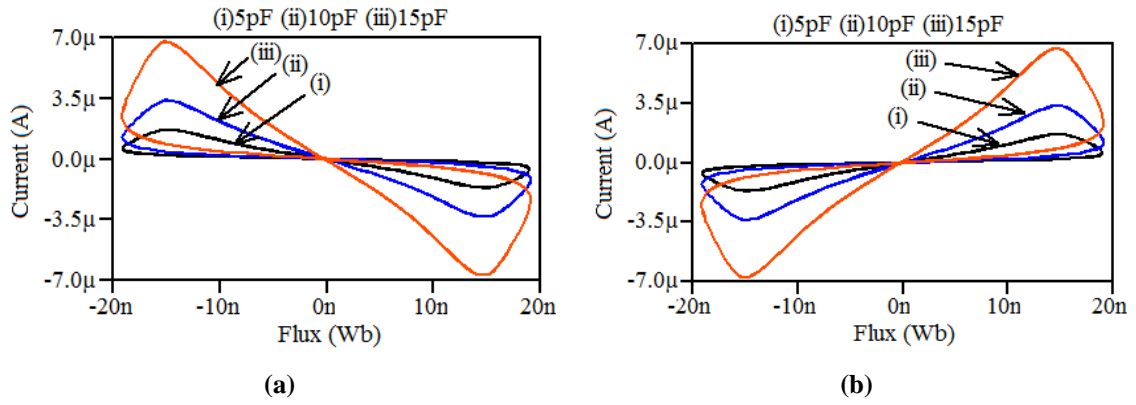
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Figure 13. PHL curves of proposed floating FOMI (a) incremental (b) decremental configuration for temperature fluctuations from -50^0C to 50^0C
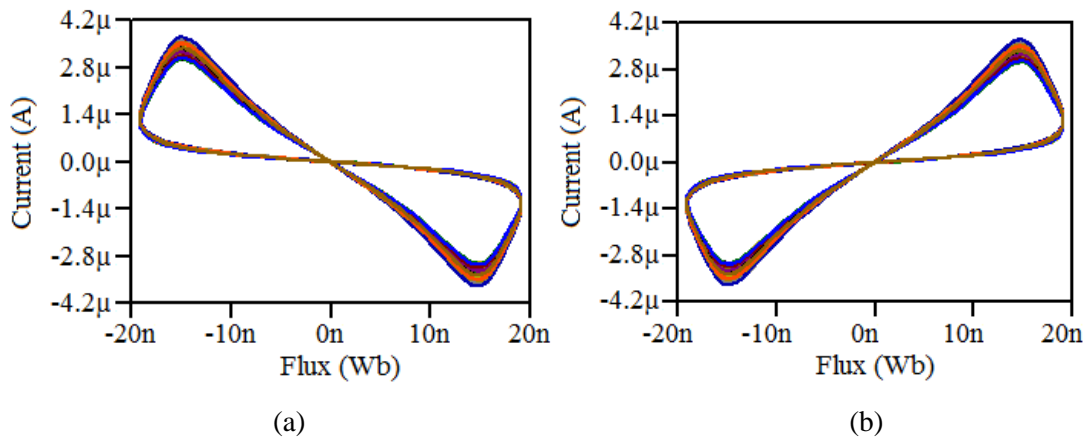
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Figure 14. PHL curves of the proposed FOMI for (a) floating incremental (b) floating decremental observed with $\pm10\%$ deviations in supply voltage

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Figure 15. PHL curves of the proposed floating FOMI observed for deviations in C_2 for (a)
incremental (b) decremental configuration

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Figure 16. PHL curves observed with MC analysis for the proposed floating FOMI for 5% variations
in aspect ratio and threshold voltage for (a) incremental (b) decremental.
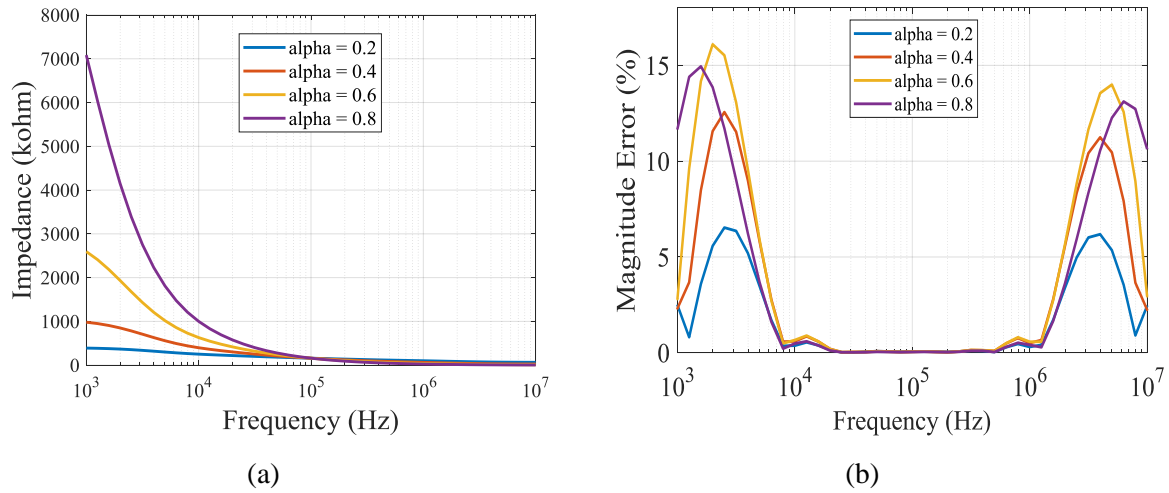
for color reproduction on the Web

(a)   (b)

Figure 17. Waveform corresponding to α = 0.2, 0.4, 0.6 and 0.8 for (a) Magnitude of impedance realized using 5th order Foster-I form (b) % error in the magnitude of fractional capacitor impedance
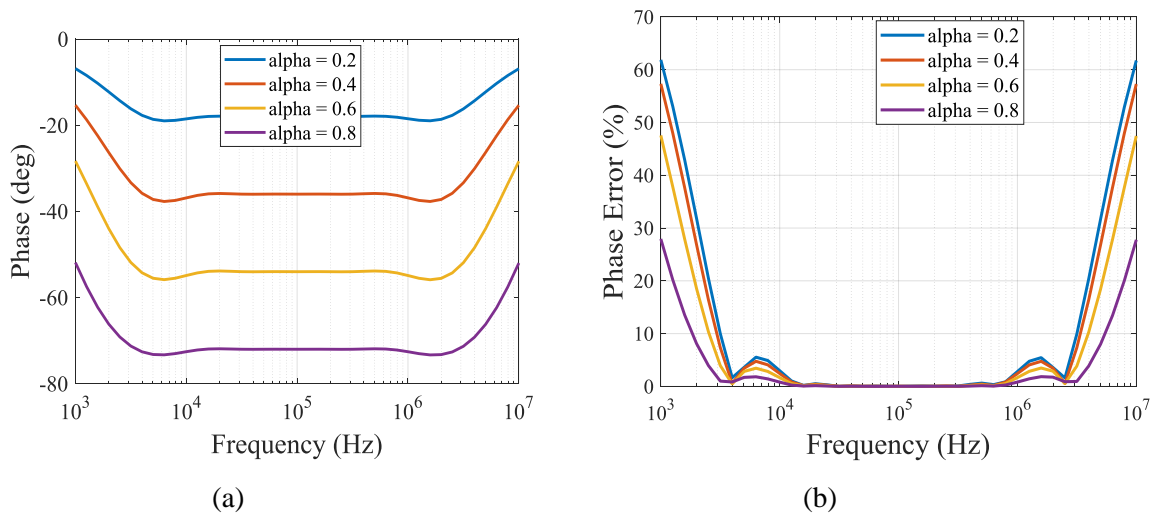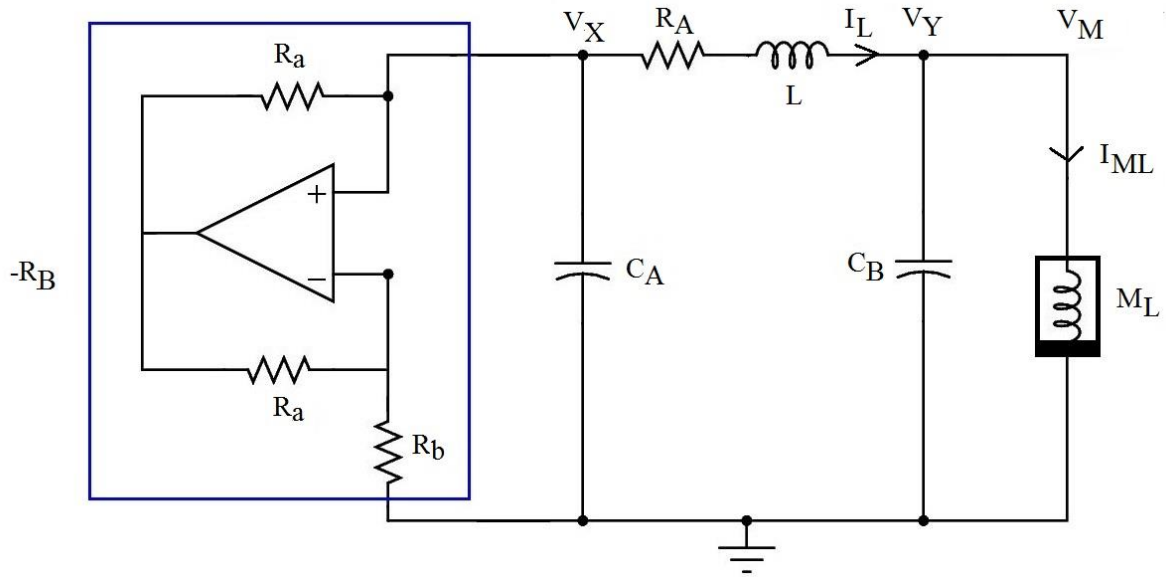
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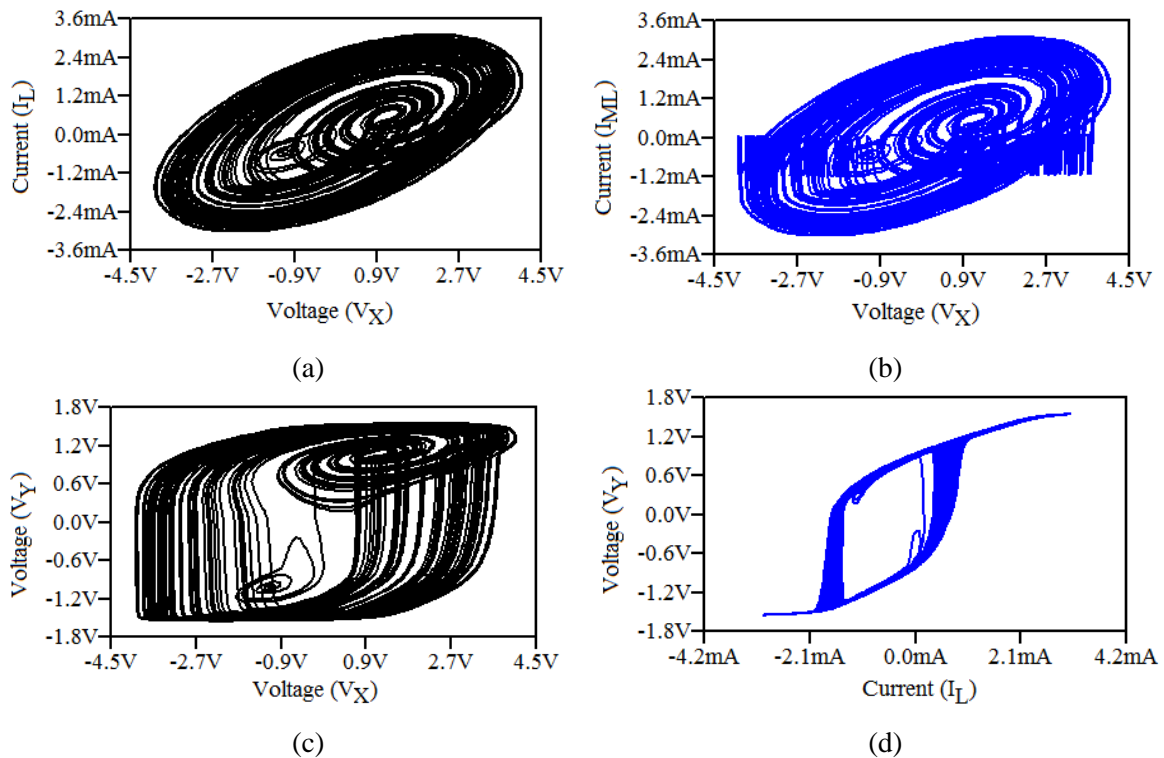(a)   (b)

Figure 18. Waveform corresponding to α = 0.2, 0.4, 0.6 and 0.8 for (a) Phase response of impedance realized using 5th order Foster-I form (b) % error in the phase response of fractional capacitor impedance

for color reproduction on the Web

Figure 19. A fourth-order Chua's chaotic oscillator

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(a)

(b)

(c)

(d)

Figure 20. Projection plots of chaotic oscillator observed between space variables (a) V_X & I_L (b) V_X & I_{ML} (c) V_Y & V_X (d) V_Y & I_L

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Tables:

Table 1 Comparison of the suggested FOMI with existing meminductor emulators

Ref No	No. of ABB	No. of R	No.of C	No.of L	Multi plier Less	Memristor less	Operat ing Freq.	Electronic Tunability	*F/G
[6]	5-CCII	4	0	0	No	Yes	10kHz	No	F+G
[7]	2 CCII+ 1 TA, 1 BOCCII	0	0	0	Yes	No	2kHz	No	F
[8]	1 DVCC+ 1 BOCCII,	1	0	0	Yes	No	2kHz	No	F
[9]	3-CCII	3	1	0	Yes	Yes	10Hz	No	F
[10]	2 OTA+ 1 CDBA	0	1	0	Yes	Yes	3MHz	No	F
[11]	4-AD844+ 1-AD633	2	0	1	No	Yes	5kHz	No	F
[12]	4-OPAMP	5	1	1	Yes	No	---	No	G
[13]	3-CCII	2	0	0	No	Yes	500Hz	NO	G
Our work	**1-VDIBA+ 1-CF**	**0**	**1**	**0**	**Yes**	**Yes**	**7MHz**	**No**	**G+F**

CCII: Second generation current conveyor, TA: Transconductance amplifier, BOCCII: Balanced Output CCII, DVCC: Differential Voltage Current Conveyor, OTA: Operational transconductance amplifier, CDBA: Current differencing buffered amplifier, OPAMP: Operational amplifier

G: Grounded; F: Floating

Table 2: Aspect Ratios of MOSFETs

VDIBA			CF		
MOS Transistors	W (μm)	L (μm)	MOS Transistors	W (μm)	L (μm)
M1-M9	54	0.18	M10-M15	14.04	1.08
			M16-M21	56.16	1.08

Table 3: R and C values for Foster-I form for various values of α

Alpha (α)	R₀(Ω)	Rₐ(Ω)	R_b(Ω)	R_c(Ω)	R_d(Ω)	R_e(Ω)	Cₐ(F)	C_b(F)	C_c(F)	C_d(F)	C_e(F)
0.2	63.43k	40.89k	31.35k	34.73k	54.72k	174.23k	2.44p	17.37p	51.34p	111.55p	247.96p
0.3	3.95k	4.22k	3.89k	4.93k	8.98k	38.05k	2.65p	14.90p	38.27p	72.87p	134.32p
0.4	24.23k	38.1k	41.92k	60.61k	128.60k	751.68k	3.26p	14.74p	33p	54.9p	82.23p
0.5	14.4k	31.4k	40.8k	67.4k	167.68k	1.42M	4.36p	16.07p	31.4p	45.50p	53.88p
0.6	8.29k	23.92k	36.54k	68.83k	201.83k	2.71M	6.30p	19.11p	32.64p	40.99p	36.85p
0.7	4.45k	1.65k	2.95k	6.36k	22.11k	535.25k	9.94p	25.06p	37.45p	40.54p	25.95p
0.8	2.11k	10k	20.72k	50.98k	213.87k	11.66M	17.97p	37.97p	49.64p	46.03p	18.64p

Biographies

Shireesh Kumar Rai received the B. Tech. degree in electronics and communication engineering from the Noida Institute of Engineering and Technology, Gr. Noida in 2008, the M.Tech. degree in VLSI Design from the YMCA University of Science and Technology, Faridabad, in 2012, and the Ph.D. degree from the Netaji Subhas Institute of Technology (University of Delhi), New Delhi, in 2017. From 2008 to 2010, he was a Lecturer at the Galgotias College of Engineering and Technology, Gr. NOIDA. From 2012 to 2013, he was a Sr. Lecturer at Echelon Institute of Technology, Faridabad. In 2013, he joined as a Teaching Cum Research Fellow with the Netaji Subhas Institute of Technology (University of Delhi). Since 2017, he has been an Assistant Professor with the Thapar Institute of Engineering and Technology, Patiala. He has authored/co-authored 43 research papers in SCI journals, 5 research papers in Scopus journals, and 6 research papers in international conferences. His research areas include mem-elements emulator circuits, chaotic circuits for cryptographic applications, analog integrated circuits for signal processing, and bandgap reference circuits.is currently working as Associate Professor, ECE Department, Netaji Subhas University of

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