A Fault-Tolerant DC-DC Buck Converter with Zero Interruption Time for Autonomous Vehicles

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Abstract A high-end autonomous vehicle is expected to have at least a hundred different electronic subsystems. Each one of them takes power from the battery through Power Management Unit (PMU). Having an efficient PMU is crucial and is expected to supply the required level of uninterrupted power. PMU consists of several buck converters which translate a higher voltage level to required lower voltage levels. A PMU is more reliable if it consists efficient and well-structured voltage converters. In this paper, a fault-tolerant buck converter is designed which outputs 3.3 volts. A simple yet effective technique is proposed to design a fault-tolerant buck DC-DC converter by bypassing the faulty converter leg. The proposed system utilizes a signal processing-based method for fault detection. The secondary converter is activated only upon the confirmed prognosis of a faulty primary converter. Ripple content in the output Aluminum Electrolytic Capacitor (AEC) voltage is monitored and used as a primary health indicator for the converter. An experimental setup is built and tested in the laboratory. Experimental results indicate a smooth transition from the primary converter to the secondary demonstrating an uninterrupted power supply along with the simplicity and effectiveness of the proposed solution.

Keywords Aluminum Electrolytic Capacitor, Power Management Unit, Prognosis, Ripple voltage, Voltage Regulator.

1 Introduction

The current era is going through the most complicated mobility regeneration. Cities have evolved from cattle carriages to automobiles, railways, metros, and airways, then to different levels of driverless autonomous vehicles [1]. Autonomous vehicles are gaining a lot of importance in the transition of urban mobility. Autonomous vehicles, also termed self-driving vehicles are expected to possess the transportation capabilities of conventional human-driven vehicles with minimal or without human intervention. From the study conducted by Chiyoung Park in [1], ensuring a safe environment digitally and physically for all users was found to be the highest priority element of autonomous vehicles [1]. Technology plays an utmost important role in achieving the same. In the successful development of an autonomous vehicle, there are challenges in every aspect like the physical build, mechanical designs, subsystem placements, and electronics hardware and software development. Autonomous vehicles must sense and read surrounding conditions, analyse them, and self-navigate accordingly. These will require many customized electronics sub systems to enable their functionality. Major systems are Advanced Driver Assistance (ADA) system [2], Parking assistance [3], Blind spot monitoring [2], LIDAR, Night vision, Cruise control, Intelligent driving control computers, Emergency responder, etc [2]. These systems are crucial for the efficient operation of autonomous vehicles. All these systems will demand different power supply ratings to function. The required power levels for each subsystem are provided by the Power Management Unit (PMU) in the vehicle which is attached to its main battery. Figure 1 depicts the block diagram of an autonomous vehicle focusing on electronic systems. The electronics of the control unit are at the centre of the control unit architecture [2]. Primary challenges in the design of electronics of the control unit are safety, reliability, and miniaturization. The PMU must supply relevant voltage to subsystems so that each subsystem functions reliably. Thus, having fault-tolerant DC-DC converters is one of the primary requirements in the safety-critical operations of autonomous vehicles. This paper intends to discuss fault-tolerant DC-DC converters in buck configuration for autonomous vehicles.

Power semiconductor switches and Aluminum Electrolytic Capacitors (AEC) are the two major components of buck converters [4]. Regretfully, 21% and 30% of breakdown or malfunctioning of power electronic converters are recorded due to a fault in the semiconductor switch and AEC respectively [5]. These components in the power supply may fail due to over current, over-voltage, temperature increase, overloading, short circuit, track breaking, ageing, etc. Also, in some cases, the cause of failure is unknown [4]. So, prognostically identifying the failure of power converters and providing fault-tolerant systems in critical applications is crucial.

A fault-tolerant DC-DC converter functions reliably despite the occurrence of fault [6]. Fault -tolerance in a DC-DC converter is achieved in several stages like fault detection, fault diagnosis, and feasible fault-tolerance implementation. Fault detection and diagnosis give an effective indication of the fault and status of fault. However, the type of fault-tolerant strategy adopted is responsible for continuous power supply with admissible quality post fault detection. Approaches used for fault detection and diagnosis are majorly classified as data-driven, model-based, and knowledge-based methods [6]. Data-driven methods are also termed signal processing methods. In this, either the time domain or frequency domain signature of identified signal parameters like DC bus current or capacitor voltage is processed to diagnose the fault [6-9]. In model based and knowledge-based techniques, the system behavior is modelled in prior and consistency between expected and measured values are analytically examined [6].

Fault-tolerant strategies are classified majorly as those which use additional hardware or those which are free of additional hardware [6-8]. Strategies based on additional hardware use bypassing of a faulty module, inclusion of additional discrete components, or inclusion of redundant legs. Strategies without additional hardware utilize phase shift adjustment or bypassing of faulty modules [6-8]. Hybrid methods of fault detection, diagnosis, and tolerance implementation are also demonstrated [7].

In this paper, a fault-tolerant buck converter for autonomous vehicle critical applications is proposed. Time domain signal processing is used for fault detection and diagnosis [5,9]. The inclusion of redundant legs with the help of additional discrete components followed by bypassing of the faulty module is used to achieve fault -tolerance [6-8].

The remainder of this paper is as follows. In section II a short survey of the available literature is carried out. Section III explains the methodology of the proposed solution. Section IV validates the proposed solution with experimental results followed by a discussion. Finally, in Section V overall work is concluded.

2. Literature Survey

The initial solution to obtain a fault-tolerant power supply is by adding redundant systems. An N+1 power converter is deployed in which N systems are required to run the system effectively [10-12]. Necessary and redundant systems are connected in parallel and diode ORing is used [12]. In [13] FET ORing technique is proposed which reduces the voltage drop across the diode. Reference [14] proposes a fault-tolerant boost converter by using two power semiconductor switches instead of one. In this, both switches share operating frequency equally and a control scheme is developed which adjusts the switching frequency to one switch if the fault is detected in the other. However, this solution leads to interruption in the output and works only for Boost converters. Reference [15,16] deals with fault detection and tolerance by monitoring inductor current variation. An event counter is used to latch and activate the redundant switch. But this works only for open circuit faults during the ON state of the semiconductor switch.

In reference [17], a new cost-effective fault-tolerant scheme without redundant switch is proposed for photovoltaic (PV) systems with Maximum Power Point Tracking (MPPT). In this Differential Power Processing (DPP) converter submodules coordinates are adjusted upon fault detection and boost converters PWM is controlled to have a fault-tolerant operation. This solution is complex and works only for open circuit faults. A simple fault clearance solution is proposed in reference [18]. Here, with the help of one diode and fuses faulty switch is cleared, so that the redundant switch can take over. In this solution, the short circuit is cleared instantly with the help of a switch and the open circuit fault is eliminated using a diode and a fuse. The proposed solution is supported by simulation and experimental results only on a boost converter. In this case fault tolerance is implemented with static redundancy. In reference [19] a new fault-tolerant scheme

is proposed with an additional redundant switch. The fault is detected by measuring the voltage across the drain-source terminal (Vds) of the MOSFET switch. The reconfiguration of converter post fault is enabled using an affine-parametrization-based control design implemented on a microcontroller. The method proposed is evaluated using the Markov model and through experiments. The proposed solution involves 10ms of interruption in the output of buck converter.

References [20,21] proposes a fault-tolerant strategy using a voltage doubler. In these, series resonant DC-DC converters are considered and upon one switch fault in the full bridge, the converter functions in the half-bridge mode. To compensate for the decreased voltage, a voltage doubler is used. Though this solution is simple it leads to efficiency compromises in constant uninterrupted output delivery. Reference [22] proposed a model-based method to detect sensor faults in buck controllers. Here, fault detection and fault-tolerant control are based on an affine switched system. The residual signals are identified for buck converter using switched system modeling. Fault detection is achieved by comparing the residual signal with a predefined threshold. System reconfiguration is also modeled and demonstrated through simulations for open circuit faults, gain and noise variations. However, proposed solution is complex in modeling. In [23], a fault-tolerant Dual Input Single Output (DISO) DC-DC converter is proposed. Inductor currents and input voltage are monitored to diagnose the fault. The proposed method demonstrates fault -tolerance towards power switch SC fault and input OC faults. Multiple redundant legs are employed and all legs are alternatively utilized under normal operation. Upon fault detection, healthy leg's duty cycles are reconfigured to continue the operation effectively. Here, multiple active redundant legs lead to power losses and system overheads. Reference [24] evaluated the effectiveness of employing zero-voltage-transition (ZVT) soft switching circuits for fault tolerance implementation. Proposed method in implemented on boost topology and an efficiency of 94% is recorded in faulty conditions. In reference [25] a fault tolerance DC-DC converter using FPGA for photovoltaic applications is presented. The proposed scheme is implemented on a boost converter by adding redundant switch, dedicated current sensors and replacing faulty semiconductor switch by monitoring inductor current shapes.

Reference [26] conducted a survey in which parallel, hybrid, and cascade architectures of buck converters were designed for various input and output voltages, and their efficiencies for LiDAR applications of autonomous vehicles were compared. Reference [26] utilized LM series buck converters from Texas Instruments in their design. Reference [26] discussed a design with 15Volts input, 3.3V output, and 1Ampere load current for which the converter efficiencies were recorded at 92%,97%, and 91% for parallel, hybrid, and cascade architectures respectively.

3. Methodology

A DC-DC power converter in buck topology majorly has an inductor, a capacitor, a free-wheeling diode, and a semiconductor switch. Based on the control of the duty cycle of the semiconductor switch, the output voltage is maintained. Standard semiconductor ICs are available to design Buck converters. The components in the Buck converter get degraded leading to non-favorable operation. According to the literature, about 30% of power converter failures are due to AEC failures. From literature, capacitors are considered degraded when their capacitance reduces by 20% or ESR (Equivalent Series Resistance) increases to 2.8 times the initial value [27]. Reference [5] demonstrates that, as the ESR of the capacitor increases, the ripple in the constant DC output voltage also increases.

In the proposed method, two Buck converters are used with the Diode OR ing technique [12]. Figure 2 depicts the block diagram of the proposed method. First Buck converter i.e primary regulator is initially ON and is giving a 3.3V constant DC output voltage. The AC ripple across the output capacitor is continuously monitored. The peak voltage of the AC ripple is extracted and compared with a predefined threshold [5] for prognostic identification of Buck Converter1 failure. When the AC ripple increases and reaches the threshold, the comparator switches the output. The comparator output is delayed using an RC network to avoid false triggering. After the prognosis of Buck Converter1 failure, Turn-ON of Buck Converter2 and Turn-OFF of Buck Converter1 is initiated. Turn-ON signal is latched to Buck Converter2 and Turn-OFF signal is latched to Buck Converter1 respectively.

An additional delay is introduced to the Turn-OFF signal before latching to Buck Converter1 which assures Turn- ON

of Buck Converter2 first and Turn-OFF Buck Converter1 later. This aids in providing an uninterrupted power supply to the load without keeping the redundant Buck converter always ON. By activating the redundant Buck converter only on a need basis, the overall power dissipation is reduced. This also increases the lifetime of the system and increases the reliability of PMU in an autonomous vehicle. A fault indication signal is provided for servicing purposes. Each block's basic functionality is described in the following section. Buck Converter1 is considered as the primary regulator and Buck Converter2 is considered to be a redundant regulator. Here, to each regulator, the feedback voltage 'Vfb' is given. Feedback 'Vfb', adjusts the duty cycle of the semiconductor switch to maintain the specific output voltage. 'Vfb' is extracted from the respective converter's output. A peak detector is designed using opamp which extracts the peak value of the ripple in the DC output. This peak ripple value is compared against the predefined threshold. A threshold is set to a voltage that is equivalent to expected rise in the ripple when capacitor ESR increases to 2.8 times original value. If the ripple peak exceeds the threshold, the comparator switches the output. RC circuit-based delaying elements are designed. A latching circuit is designed using a transistors to latch the enable signal (nVEN) to Buck Converter2. This latch maintains the enable signal even after Buck Converter1 turns OFF and peak ripple output reduces. Turn-OFF of Buck Converter1 is delayed slightly using an RC network so that, Buck Converter2 turns ON before turning OFF of Buck Converter1. A transistor-based latching circuit is used to latch the disable signal (VDIS) to Buck Converter1.

4. Experimental Results and Discussion

To experimentally evaluate the proposed fault-tolerance technique simulations and experimantal validations are carried out. TINA by Texas Instruments is used to design and simulate the proposed solution before conducting the experimental study. A voltage regulator in buck topology is designed using LM5085 buck controller [28]. This powerful voltage controller features a PFET gate driver and high voltage bias regulator that work across a wide 4.5-V to 75-V input range. The continuous ON-time regulation strategy eliminates the need for loop correction, simplifies circuit construction, and yields a very quick load transient response. Due to the inverse relationship between input voltage and on-time, operating frequency essentially stays constant even when the line and load are changing. The PFET architecture allows for a 100% duty cycle due to its low dropout voltage. Figure 3 depicts the schematic of the voltage regulator designed. Here, LM5085 Buck voltage Controller IC is used. A Constant DC input voltage of 12 V with ±3 volts tolerance is assumed. A 33uF AEC is used. The AEC considered has 250m ohms Equivalent Series Resistance (ESR).
The schematic of the proposed fault tolerant scheme is depicted in figure 4.

The performance of the proposed fault tolerance scheme when the system performs in steady state, while transitioning to degraded state and when recovers from faulty conditions is eveluated. An external resistor is added to increase the ESR of the capacitor. This emulates the degradation of the capacitor and thereby increases the ripple in DC output voltage indicating the ageing of the capacitor. Figure 5 depicts the simulation results of proposed solution. The transient section is zoomed in and presented for better understanding. Here, there is no interruption time observed when the system switches from Buck Converter1 to Buck Converter2. We can observe in figure 5 as the ripple in Buck converter1 output increses due to degradation, enable signal to Buck converter2 is activated first and with predefined delay disable signal to Buck converter2 gets activated. The signal to indicate the fault in Buck Converter1 gets activated. From the simulation, it is observed that, when Buck Converter2 turns ON, switching MOSFET of Buck Converter2 adjusts its turn ON periods to attain the required output voltage gradually. The output voltage ripple reduces to normal after the turn-on of Buck Converter2.

Table 1a depicts the major component specifications assumed for the design of the proposed fault-tolerant buck converter. Table 1b lists the major components used in the design and experimental setup of the proposed system.

Figure 6 exhibits the prototype of the proposed fault tolerant buck converter solution. Figure 7 displays the experimental setup used to validate the solution proposed. Here, a DC power supply is used to input 12 volts of DC into the circuit. A digital oscilloscope is used to capture the signals. An external resistor is appended to increase the ESR of the AEC. Figure 8 depicts the outputs of proposed systems for probable conditions. Figure 8a displays output when the system turns ON and is

functioning without any degradation. We can see from figure 8a that upon turning ON, both Buck Converter1 and Buck Converter2 turn ON. After initialization Buck Converter2 turns OFF and Buck Converter1 continues to perform steadily and gives constant output voltage. Figure 8b displays the experimental result of the proposed system when a fault occurs during steady state operating conditions. The figure also displays the zoomed version of the output depicting the transition from Buck Converter1 to Buck Converter2. From the output waveform, we can observe the increase in AC ripple in the 3.3V DC output as the capacitor ESR is increased. This increased ripple is monitored and as it increases beyond the defined threshold, we can observe a shift in the output signal of Buck Converter2. Figure 8b also depicts the signal indicating the degradation of Buck Converter1 and gradual turn OFF of Buck Converter1. Here, initially, the system is tested for original capacitor parameters. Later, the capacitor ESR is updated by increasing the ESR emulating the degradation. Then the output changed as expected to the degraded version and fault detection and fault-tolerance by activating Buck Converter2 is achieved. From Figure 8b, we can observe that there is no interruption while switching from Buck Converter1 to Buck Converter2.

Figure 8c displays output waveforms during the initial setup when Buck Converter1 is already degraded or faulty. In figure 8c we can observe that upon turn-ON both Buck Converter1 and Buck Converter2 are activated. However, as Buck Converter2 begins to turn OFF the output ripple is monitored and immediately Buck Converter2 turns ON and Buck Converter1 turns OFF. We also observe that there is no interruption in the output voltage in any discussed conditions.

In this proposed solution care is taken to avoid false triggering unlike in available fault-tolerant techniques using signal processing-based fault detection. Table 2 lists a comparative analysis of the proposed system with available literature. From Table 2, we can observe that most available systems have either a redundant system always active or there is interruption time while switching from primary to a redundant system. The proposed system overcomes both of these issues. The proposed solution also has low design complexity with minimal additional components.

To summarize, the proposed solution provides a fault-tolerant buck power converter with zero interruption time. The proposed solution of fault-tolerance is conveniently expandable to MOSFET or Diode degradation-induced failures. It is also applicable to other voltage converter topologies like Boost, and Buck-Boost converters.

5. Conclusion

In this paper, a novel fault-tolerant buck converter system for autonomous vehicle power management units is discussed. The proposed system gives constant uninterrupted DC power by prognostically identifying primary buck converter failure and thereby activating secondary buck converter using signal processing technique. Here, false alarms are avoided by careful design. Also, a redundant secondary system is activated only after identifying primary converter failure. This reduces power wastage in the system and enhances the overall lifetime of the system. The system is simple in design, cost-effective, uses less number additional components, and is highly efficient. These qualities make the system suitable for critical applications of autonomous vehicles. The proposed system is tested with simulations and experimentally. The results demonstrate the proclaimed properties of the system. The proposed system of fault detection and tolerance implementation is tested on a buck converter. However, this is scalable to other topologies of power converters like boost, and buck-boost efficiently. The fault detection and fault-tolerance implementation method introduced could be explored and adapted for the failure of buck converters due to MOSFET or Diode degradation.

Declarations:

Availability of data and Materials: Not applicable

Competing interests: The authors declare that they have no known competing financial interests or personal relationships

that could have appeared to influence the work reported in this paper.

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Figure captions:

Fig. 1 Block Diagram of Autonomous Vehicle with Major Electronic Systems

Fig. 2 Block Diagram of Proposed Solution.

Fig. 3 Schematic of the Voltage Regulator Designed.

Fig. 4 Schematic Representation of Proposed Fault- Tolerant Scheme

Fig. 5 Simulation Result of the Proposed Method. Here, Vreg1 and Vreg2 are the output voltages from Buck Converter1 and Buck Converter2 respectively. Vfault is the fault indicating signal. nVEN and VDIS are enable signal given to Buck Converter2 and disable signal given to Buck Converter1 respectively.

Fig. 6 Prototype of Proposed Solution

Fig. 7 Experimental Set-up of Proposed System

Fig. 8a Output of the Proposed System During Turn -ON and Upon Healthy Operation

Fig. 8b Experimental Results of Proposed Fault-Tolerant Buck Converter Upon Fault Occurrence During Operation

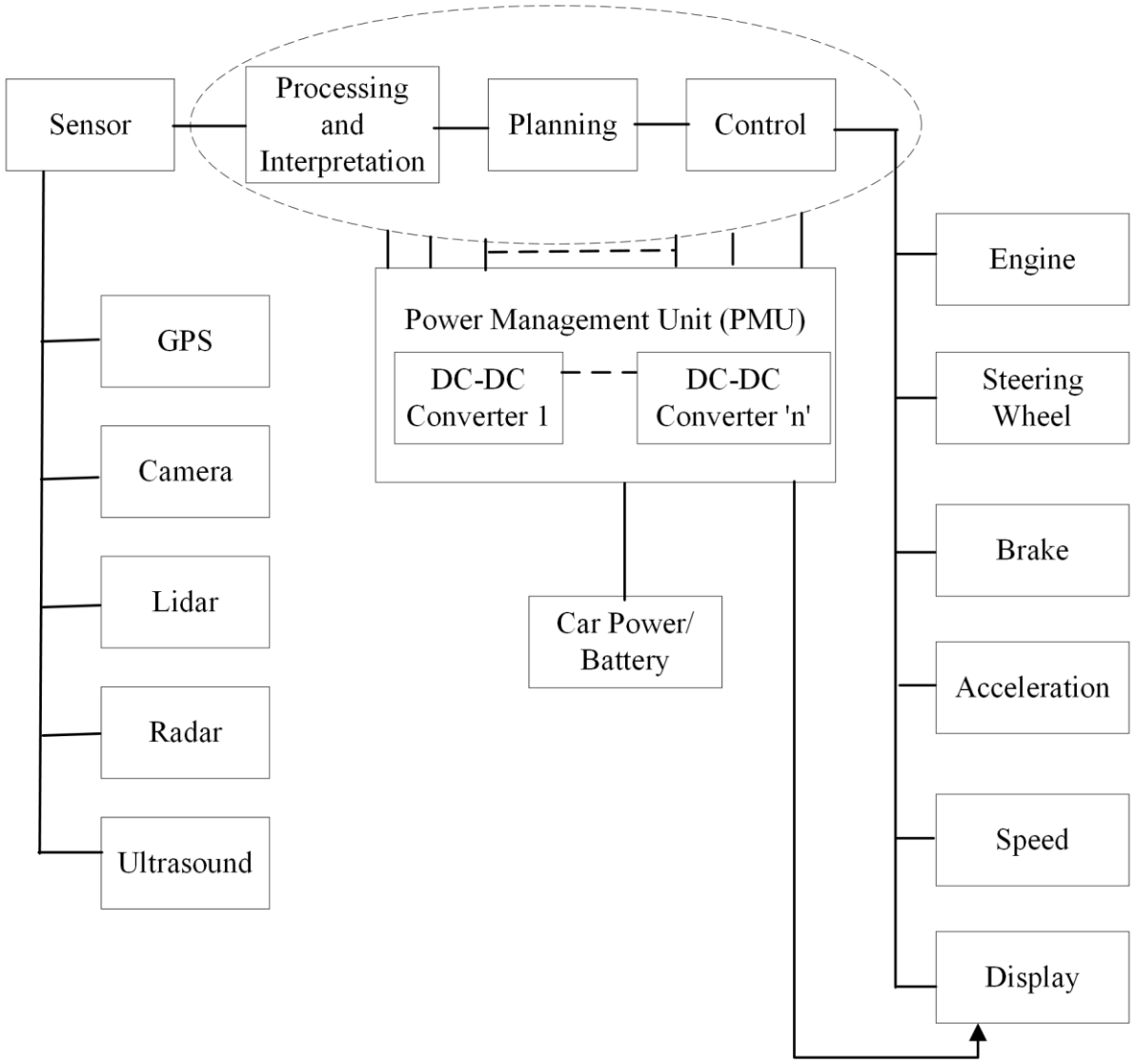
Fig. 8c Output of the Proposed System Upon Turn-ON while Regulator1 is Degraded

Table Captions:

Table 1a Specifications of the Proposed System

Table 1b Components used in the Proposed System

Table 2 Comparative Analysis of Proposed system with Existing Systems



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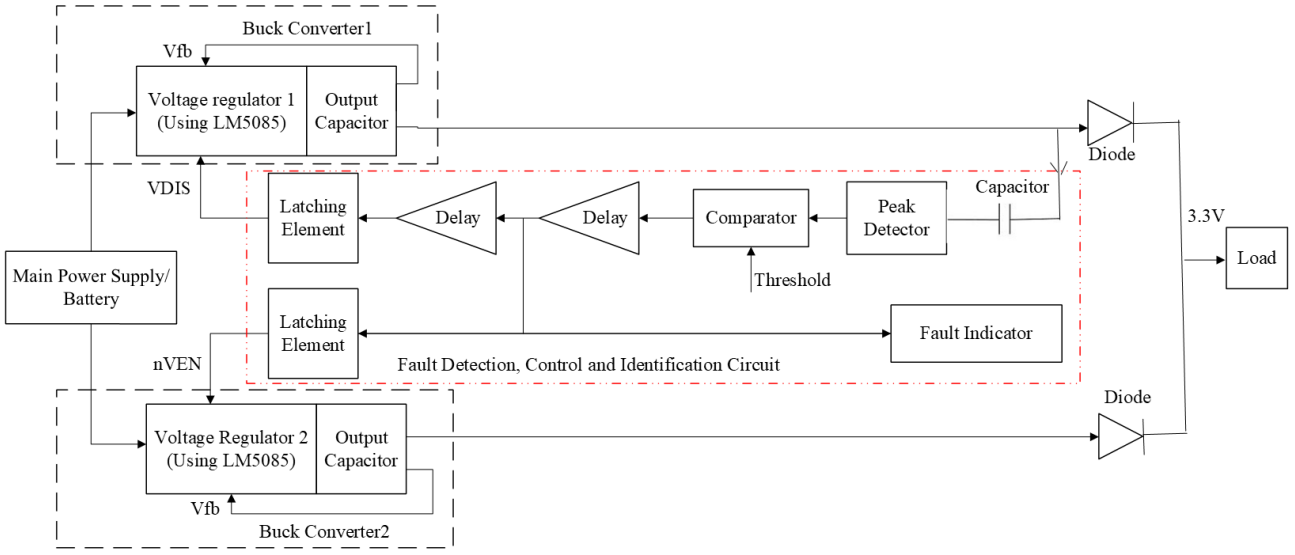

Fig. 2 Block Diagram of Proposed Solution.

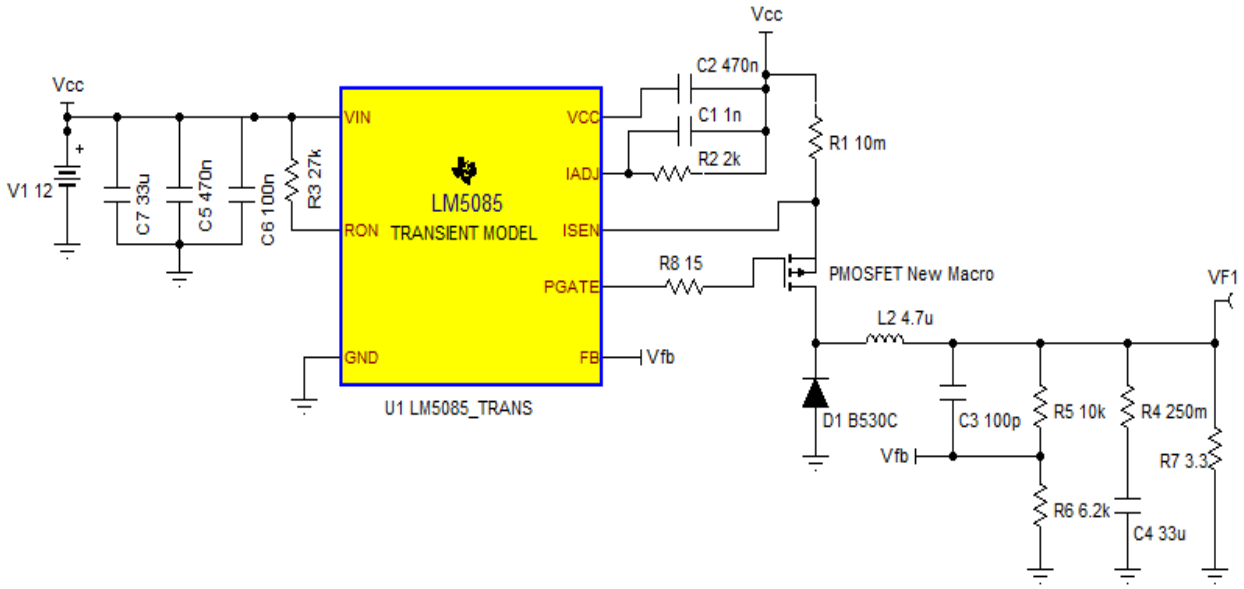

Fig. 3 Schematic of the Voltage Regulator Designed.

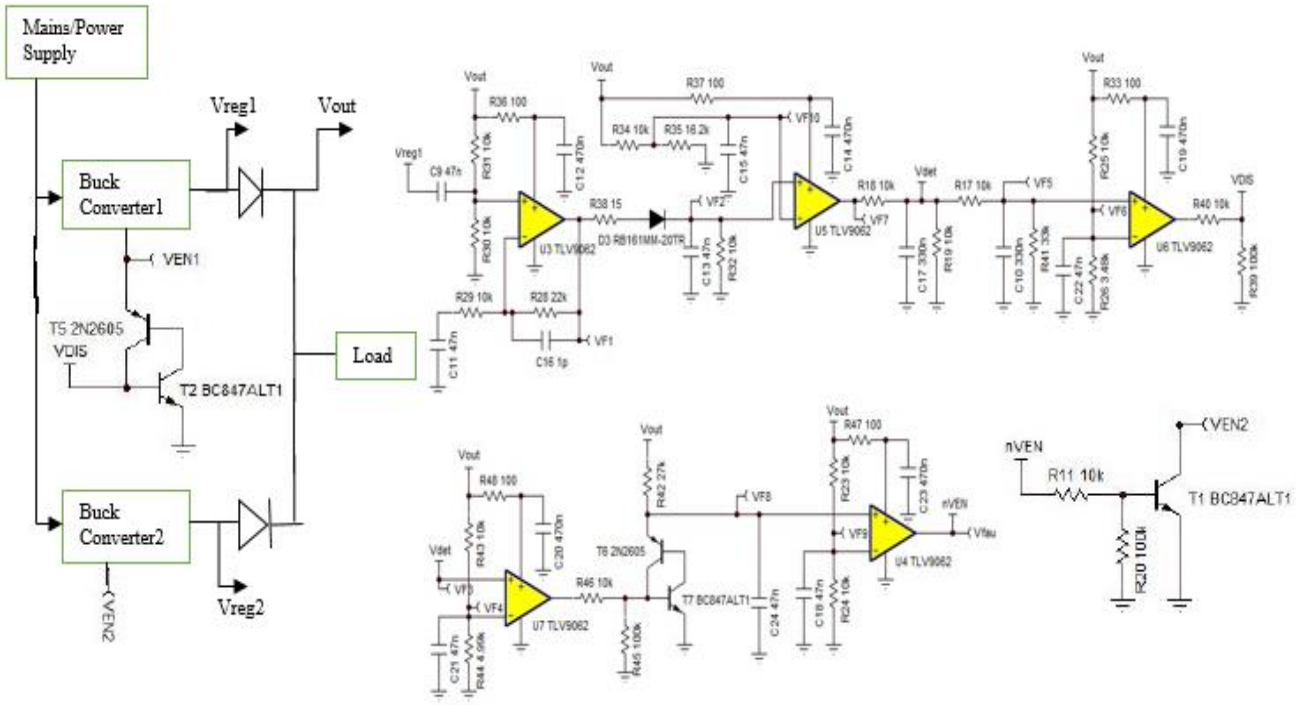

Fig. 4 Schematic Representation of Proposed Fault- Tolerant Scheme

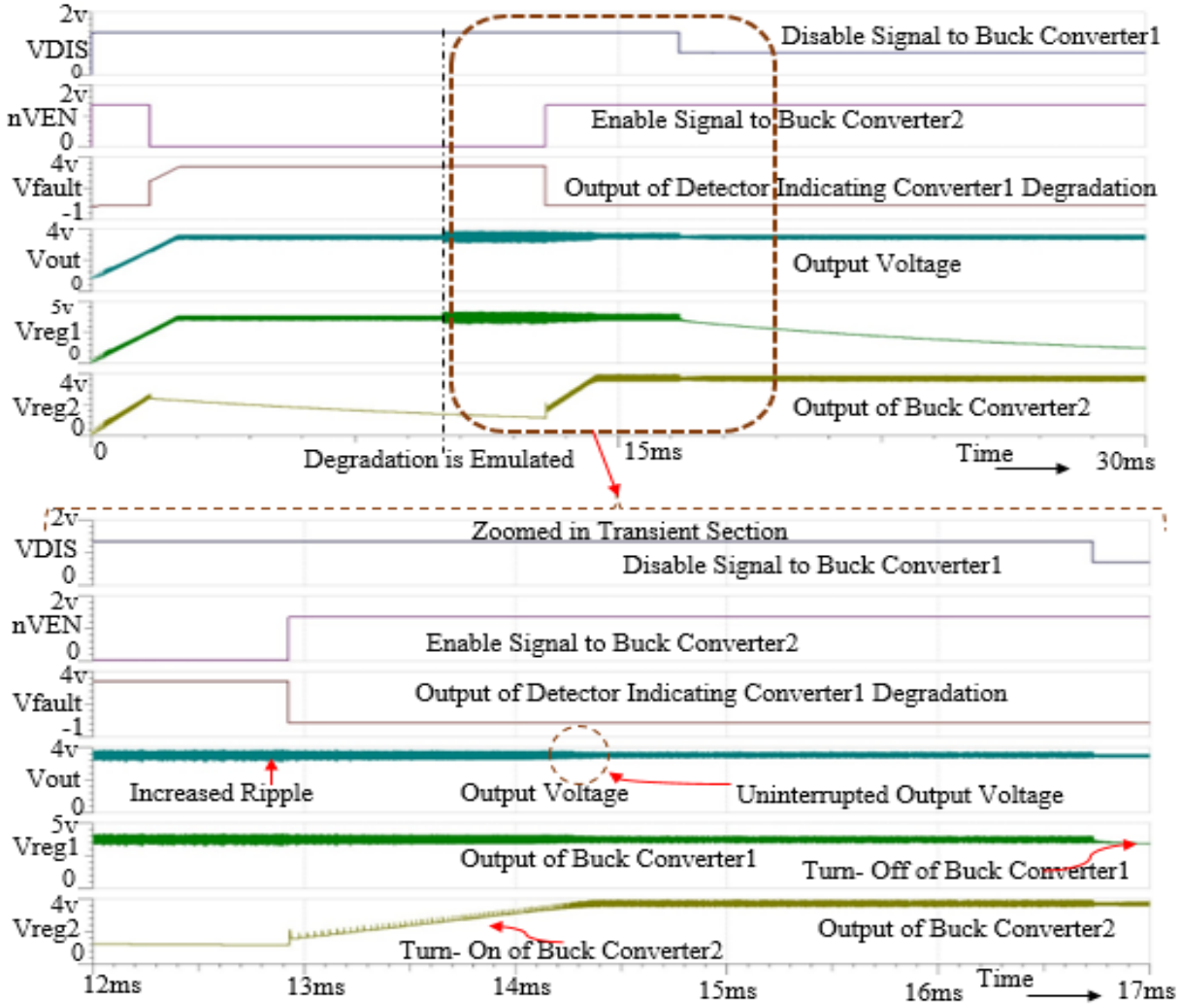

Fig. 5 Simulation Result of the Proposed Method. Here, Vreg1 and Vreg2 are the output voltages from Buck Converter1 and Buck Converter2 respectively. Vfault is the fault indicating signal. nVEN and VDIS are enable signal given to Buck Converter2 and disable signal given to Buck Converter1 respectively.

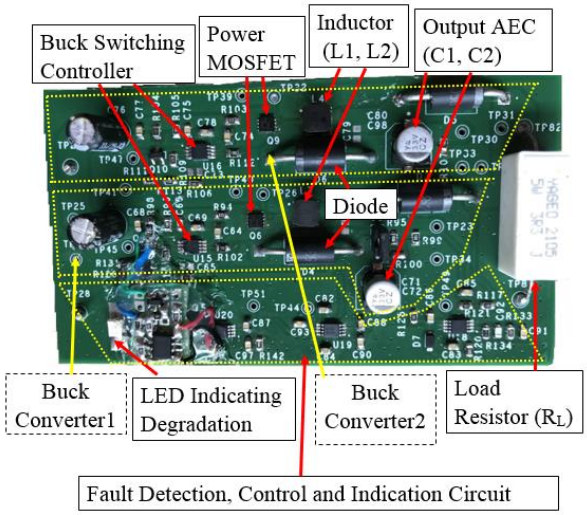

Fig. 6 Prototype of Proposed Solution

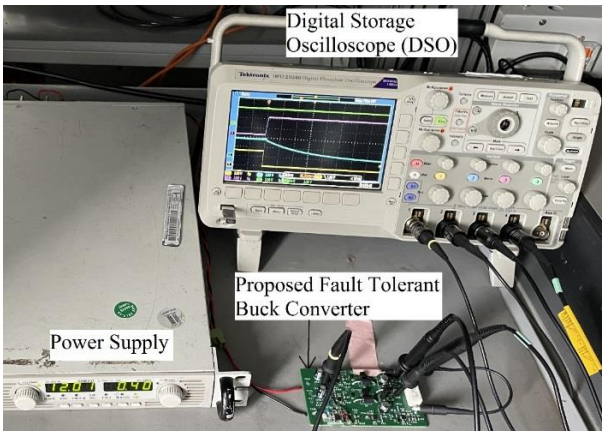

Fig. 7 Experimental Set-up of Proposed System

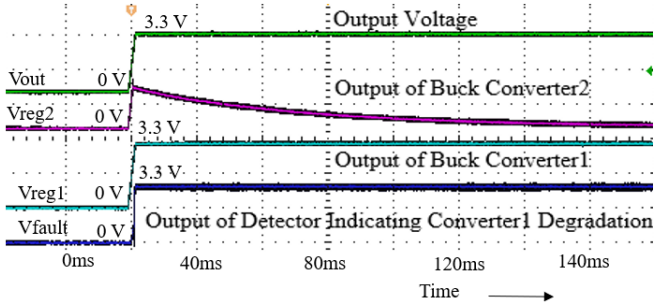

Fig. 8a Output of the Proposed System During Turn -ON and Upon Healthy Operation

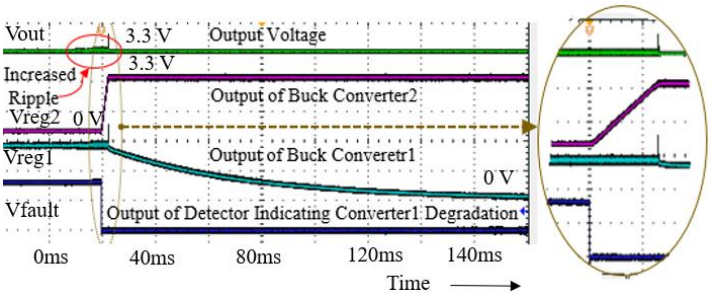

Fig. 8b Experimental Results of Proposed Fault-Tolerant Buck Converter Upon Fault Occurrence During Operation

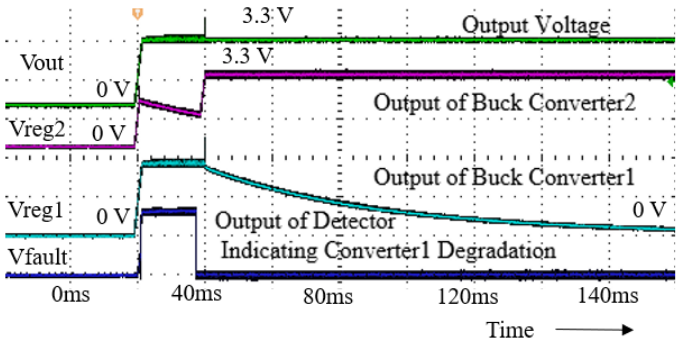

Fig. 8c Output of the Proposed System Upon Turn-On while Regulator1 is Degraded

Table 3a Specifications of the Proposed System

Parameter	Description	Value
Vcc	Input Voltage	12±3 V
Vout	Output Voltage	3.3V
Iout	Output Current	1A

Table 1b Components used in the Proposed System

Component	Description
LM5085	Buck Switching Controller IC
CSD4502Q3A	Power MOSFET
B530C	Diode
L1, L2	4.3uH Inductor
C1, C2	33uF Output AEC
R_L	3.3Ω Load Resistor
LST67K-J1L2-1-Z	LED Indicating Degradation
BC847 *	NPN Transistors*, PNP Transistors**,
2N2605 **	Op-amp***- Used in Fault Detection,
TLV9062 ***	Control and Indication Circuit

Table 4 Comparative Analysis of Proposed system with Existing Systems

Reference Number	Converter Topology Considered	Faults Detected	Diagnostic Variable	Reconfiguration Strategy	Is Redundant system/element always Active?	Complexity/Cost	Is output uninterrupted?	Interruption Time
[14]	Boost	OC/SC	output voltage	Bypass the faulty switch and Phase shift adjustment	Yes	Low	No	15ms
[15]	Buck, Boost, Buck-Boost	OC	Inductor Current	Inclusion of redundant component	No	Low	Yes, for Buck & No, for Boost &Buck-Boost	3us
[16]	Boost	OC	Inductor Current	Inclusion of redundant component	No	Low	No	93us for D=0.2, 4us for D=0.8
[17]	Boost, Buck-Boost	OC	Inductor Current	Bypass the faulty switch and Phase shift adjustment	Yes	Medium	No	Fast
[18]	Boost	OC/SC	Inductor current	Inclusion of additional discrete components	Yes	Low	No	<<1Tsw
[19]	Buck	SC	Voltage across switch Vds	Inclusion of additional discrete components	No	Medium	No	10ms
[20,21]	Series Resonant DC-DC Converter	OC/SC	Inductor Current/Capacitor Voltage	Inclusion of additional discrete components	Yes	Medium	No	45ms
[22]	Buck	OC/Gain variation and Excess Noise	Inductor Current/ Capacitor Voltage	Inclusion of additional discrete components	Yes	High	No	10ms
[23]	Buck, Boost, Buck-Boost	OC/SC (partial)	Inductor Current/Input Voltage	Inclusion of Redundant Legs	Yes	Low	No	NA
[24]	Boost	OC/SC	Voltage Vgs Across Switch	Inclusion of additional discrete components	Yes	Medium	No	~5ms
[25]	Boost	OC/SC	Inductor Current	Inclusion of additional discrete components	No	High	No	<1Tsw

Proposed System	**Buck**	**OC/SC**	**Ripple in the capacitor voltage**	**Inclusion of redundant leg**	**No**	**Low**	**Yes**	**Uninterrupted**
	OC-Open Circuit			NA-Not available				
	SC-Short Circuit			Tsw-1/Switching frequency				