A Look-up Table Based Method for Voltage Balancing of Neutral-Point in Five-level ANPC Converter

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***Abstract*— In this paper, an easily implementable method based on look-up tables is presented for balancing the neutral-point (NP) voltage in a five-level "Active NPC" topology for space vector modulation (SVM). In the proposed method, by utilizing the direction of output phase currents, operating region is divided into six zones. In each zone, there are two look-up tables; one for increasing the NP voltage and the other for decreasing the NP voltage. Since some look-up tables in different zones are identical, six individual look-up tables are obtained for controlling the NP voltage. In the proposed method, just few comparative operators and six look-up tables are utilized; therefore this method has proper implementation capability. Also, the proposed method is experimentally implemented on an active NPC converter which drives an induction motor via rotor field oriented control (RFOC) method. Experimental results verify performance, good dynamic response and effectiveness in balancing the NP voltage in low and high modulation index.**

***Keywords*— Multilevel Inverter, Space Vector Modulation, Active Neutral Point Clamped (ANPC), Voltage Balancing, Motor Drive.**

1. INTRODUCTION

According to proper harmonic spectrum, reduction of rated value of devices, reduction of switching frequency and low $\frac{dv}{dt}$, multilevel converters are widely used in high power and high voltage applications which are utilized in industries such as petrochemical, traction, mining, FACTS, marine applications, etc [1-6].

In higher number of levels, both of neutral-point clamped (NPC) and flying capacitor converters have the problem of balancing the capacitors (dc-link capacitors for NPC and flying capacitors for flying capacitor converters). Recently, several works have been done on balancing the capacitors in NPC [7-10], flying capacitor [11-12] and modular multilevel [13-15] topologies.

The five-level active NPC is one of the most attractive topologies between multilevel converters. As described in [16], the overall switch utilization is low in NPC converters which can lead to limitation of output power. To overcome this drawback, the NPC voltage source converter (VSC) is extended to the ANPC VSC [16-18].

Different modulation methods have been utilized for ANPC VSC [19-22]. In [19], a universal carrier-based PWM design method through hierarchical decomposition concept is proposed to overcome the increasing PWM design complexity of multilevel converter with a high number of output levels. An optimized PSPWM method is proposed in [20]. Also in this paper, an optimized neutral-point potential balance method is proposed, which can make a trade-off between the neutral-point potential balance and the harmonic performance. In [21], a common-mode voltage reduction strategy based on phase-shifted pulse-width modulation (PS-PWM) is proposed for ANPC converter, which can realize the NP voltage and the flying capacitor (FC) voltages balance. In [22], a novel space-vector pulse width modulation (SVPWM)

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technique for a five-level active neutral-point clamped (5L-ANPC) inverter is proposed to eliminate the common-mode voltage (CMV).

Also, different methods are presented which focus on balancing the voltages of DC-link and flying capacitors [23-29]. In [25], a method for balancing the DC-link and flying capacitors is presented in a situation that phase-shifted modulation is utilized. In this method, an optimum zero-sequence voltage is calculated to regulate the neutral-point potential. The voltage across the flying capacitors is also regulated by adjusting the switching duty cycles of two PWM signals, which varies the operation time of redundant switching states in each switching period. Also, in [26], for a carrier-based PWM strategy, the voltage balancing across the flying capacitors is achieved by using a proper selection of redundant switching states, and the neutral-point voltage is controlled by the classical dc offset injection. In selective harmonic elimination pulse-width modulation (SHEPWM), both the voltage across the flying capacitors and the dc-link neutral point can be balanced by a small change in the switching angles, which is decided upon the voltage across the lower dc-link capacitor, the voltage of the flying capacitor and the direction of the load current [27]. The proposed strategy in [28] analyses all vectors characteristics and computes the vector durations based on the NP voltage difference, which can flexibly balance the NP voltage. Also, a simple method is presented in [29]; this voltage balancing control is achieved by carrying out a proper selection of the switching signals of the converter taking into account the actual values of the flying capacitor voltage and the phase current.

In this paper, a method is proposed in order to achieve a simple method with proper performance in neutral point voltage balancing for five-level ANPC which can be combined with SVM. In the proposed method, according to the direction of three-phase currents, the operating area is divided into six different zones. In each zone, two different look-up tables are determined; one for increment of NP voltage and the other for decrement of NP voltage. Since some look-up tables in different zones are identical, six individual look-up tables are obtained for controlling the NP voltage. Afterwards, the proper look-up table would be selected based on the direction of three phase currents and the need for increment/decrement of NP voltage; utilization of this look-up table in selecting the proper output voltage vector leads to balancing the NP voltage. The main advantages of the proposed method for dc-link voltage balancing of Active NPC converter are less computational complexity and simplification of implementation. It should be noted that all of operations for dc-link voltage balancing includes basic logic operators such as and, or, not, etc.

In this paper, at first, multilevel SVM and the method of balancing the flying capacitor voltages are presented in Sections. II and III. Afterwards, the proposed method of balancing the neutral-point (NP) voltage is presented in Section. IV. Finally, the proposed method performance is evaluated by experimental results in Section. V.

2. MULTILEVEL SPACE VECTOR MODULATION

In this paper, SVM is utilized in the 60-degree system. In multilevel SVM strategy in 60-degree system, at first, $\alpha-\beta$ components of voltage are calculated [30-31]:

$$\begin{aligned} V_{\alpha}^{*} &= V^{*}\cos(\theta)-\frac{V^{*}\sin(\theta)}{\sqrt{3}} \\ V_{\beta}^{*} &= V^{*}\cos(\frac{\pi}{3}-\theta)-\frac{V^{*}\sin(\frac{\pi}{3}-\theta)}{\sqrt{3}} \end{aligned} \quad (1)$$

Afterwards, the foursquare, which the voltage vector is placed in (as shown in Fig. 1), will be determined using normalized values of V_{α} and V_{β}:

$$\begin{aligned} &A:(V_{A\alpha},V_{A\beta})=(V_{A\alpha}=\mathrm{int}(V_{\alpha}^{*}),V_{A\beta}=\mathrm{int}(V_{\beta}^{*})) \\ &B:(V_{B\alpha},V_{B\beta})=(V_{A\alpha},V_{A\beta}+1) \\ &C:(V_{C\alpha},V_{C\beta})=(V_{A\alpha}+1,V_{A\beta}+1) \end{aligned} \quad (2)$$

$$D:(V_{D\alpha},V_{D\beta})=(V_{A\alpha}+1,V_{A\beta})$$

After determining the vertices of the foursquare, the triangle of the voltage can be determined using amplitude of reference voltage vector and comparing it with the value of voltage vertices of foursquare (ABD or BCD) [30-31].

Switching times are calculated by utilizing T_s, the value of voltage vertices of the triangle and the amplitude of reference voltage. Typically, for BCD triangle, the system of equations contains three equations and three unknown switching times (T_B, T_C and T_D).

$$\begin{cases} V_{B\alpha}.T_B+V_{D\alpha}.T_D+V_{C\alpha}.T_C=V_\alpha^*.T_s \\ V_{B\beta}.T_B+V_{D\beta}.T_D+V_{C\beta}.T_C=V_\beta^*.T_s \\ T_B+T_D+T_C=T_s \end{cases} \quad (3)$$

In each switching time period, according to the values of V_α and V_β, final voltage vector (and status of the switches) will be determined via a pre-defined look-up table.

3. Flying Capacitors Voltage Balancing

In order to balance the voltages of flying capacitors, redundant voltage vectors related to ANPC should be investigated. According to the voltage vectors of ANPC, vectors of -V_{dc}/2, 0 and +V_{dc}/2 have no effect on voltage of flying capacitors. Therefore, in intervals that these voltage vectors are implemented, flying capacitors voltages are kept constant.

Therefore, only redundant voltage vectors in the voltage levels of V_{dc}/4 or -V_{dc}/4 can be utilized in order to stabilize flying capacitors voltages in V_{dc}/4. In intervals that voltage vectors of V_{dc}/4 or -V_{dc}/4 are implemented, each flying capacitor voltage is compared with reference voltage of V_{dc}/4; also phase current direction is determined. Therefore, according to flying capacitor voltage of each phase and the direction of each phase current, proper voltage vector can be selected using Table. 1. For example, both of V_5 and V_6 produce voltage level of V_{dc}/4 at the output; which for the positive current of the corresponding phase, V_5 causes a decrease in the FC voltage and V_6 causes an increase in the FC voltage. At the moment of implementing the voltage vector, according to the value of FC voltage, if it is needed to increase FC voltage, V_6 is used and otherwise V_5 is used.

4. Neutral Point Voltage Balancing

In order to balance the neutral point voltage, a look-up table based method is proposed for ANPC. The topology of the ANPC is shown in Fig. 2. Redundant vectors are chosen in such a way to equate the upper half of dc-link voltage with lower half of dc-link voltage. This method will be added to the final section of SVM. In the final section of SVM, voltage vector will be selected from look-up table. According to the direction of each output phase current, selected voltage vector can lead to increment, decrement or no-effect on neutral point voltage. It should be noted that the lower half of dc-link voltage ($V_{dc\text{-}2}$) will be compared with half of total dc-link voltage (V_{dc}/2) ($V_{dc}=V_{dc-1}+V_{dc-2}$); therefore if the lower half of dc-link voltage ($V_{dc\text{-}2}$) is lower than half of total dc-link voltage (V_{dc}/2) (in this condition, the upper half of dc-link voltage ($V_{dc\text{-}1}$) is more than half of total dc-link voltage), then the lower half of dc-link voltage ($V_{dc\text{-}2}$) should be increased and lower half of dc-link voltage ($V_{dc\text{-}2}$) should be decreased, and vice versa. In every iteration of SVM calculation, before utilizing look-up table, the proper look-up table (in order to balance the dc-link voltage) should be selected according to the direction and absolute value of output phase currents and also increment or decrement of each half of dc-link voltage. The proper voltage vector will be obtained from this look-up table.

In the dc-link voltage balancing method, neutral point voltage can be assumed relative to both of positive rail (V_{dc-1}) or negative rail (V_{dc-2}). In the following, in proposed method, neutral-point voltage is assumed as V_{dc-2}.

In this method, in each data sampling, the value of three phase currents, and dc voltages are measured. According to the direction and absolute value of three phase currents in each sample, the operating point would be located in one of the following zones:

$$
\begin{aligned}
&1)\ (i_\alpha > 0 \ and\ |i_a| > |i_b| \ and\ |i_a| > |i_c|)\\
&2)\ (i_\alpha < 0 \ and\ |i_a| > |i_b| \ and\ |i_a| > |i_c|)\\
&3)\ (i_b > 0 \ and\ |i_b| > |i_c| \ and\ |i_b| > |i_a|)\\
&4)\ (i_b < 0 \ and\ |i_b| > |i_c| \ and\ |i_b| > |i_a|)\\
&5)\ (i_c > 0 \ and\ |i_c| > |i_a| \ and\ |i_c| > |i_b|)\\
&6)\ (i_c < 0 \ and\ |i_c| > |i_a| \ and\ |i_c| > |i_b|)
\end{aligned}
\qquad (4)
$$

Therefore, in each zone, two look-up tables should be determined; first for increment of neutral point voltage and second for decrement of neutral point voltage. According to identical look-up tables, there are six individual look-up tables for balancing the NP voltage. After determining the zone, in each sample, the proper look-up table should be selected according to the determined zone and also the need for increment or decrement of neutral point. The proper voltage vector will be obtained from this look-up table. Look-up tables are determined based on the following rules:

1) In zone 1 ($|i_a|=|i_b+i_c|$ and $i_a>0$, $i_b<0$, $i_c<0$), effect of selected phase 'a' voltage vector (in increasing or decreasing neutral point voltage) is more than two other phases ('b' or 'c'). This clause can be extended to zones 3 and 5.
2) In zone 2 ($|i_a|=|i_b+i_c|$ and $i_a<0$, $i_b>0$, $i_c>0$), direction of phase currents is opposite in comparison with zone 1. Therefore, look-up table which increases neutral point voltage in zone 2 is the same as look-up table which decreases neutral point voltage in zone 1. This clause can be extended to zones 4 and 6 (accordingly, there are 6 look-up tables in total).
3) Implementing voltage vectors of $-V_{dc}/2$ or $+V_{dc}/2$ in each phase has no effect on neutral point voltage.
4) Implementing voltage vectors of $-V_{dc}/4$ or $+V_{dc}/4$ in each phase leads to different results depending on selected redundant voltage vector and direction of phase current. Implementing the first redundant voltage vector results in no-effect on neutral point voltage. Implementing second redundant voltage vector may result in increment or decrement of neutral point voltage depending on direction of phase current. If instantaneous value of phase current is negative, then neutral point voltage increases and vice versa.
5) Implementing voltage vectors of V3 or V4 in each phase leads to two different results depending on direction of phase current. If instantaneous value of phase current is negative, then neutral point voltage increases and vice versa. It should be noted that both of redundant voltage vectors have same effect on neutral point voltage.

For example, vector 032 ('0' for phase 'a', '3' for phase 'b' and 2 for phase 'c') in zone 1 is investigated to determine its effect on NP voltage. It should be noted that a number between 0 to 4 will be assigned to each phase; '0' means $-V_{dc}/2$, '1' means $-V_{dc}/4$, ... and '4' means $+V_{dc}/2$. In this zone, despite being $i_a>0$, implementing $-V_{dc}/2$ (or vector *V0*) in phase 'a' leads to no effect on NP voltage from phase 'a'. On the other hand, i_b is negative ($i_b<0$) in zone 1, then using first redundant of $+V_{dc}/4$ (V5) results in no-effect on NP voltage. Also second redundant of $+V_{dc}/4$ (V6) leads to increment of NP voltage due to negative value of i_b. According to negative value of i_c, implementing both redundancies of vector 2 (*V3* or *V4*) results in increasing the NP voltage. Consequently, phase 'a' has no effect on NP voltage, phase 'b' has no effect on NP voltage or leads to increment of NP voltage depending on the implementing redundant vector, and finally phase 'c' leads to increment of NP voltage. Therefore, vector 032 in zone 1results in increment of NP

voltage in total. It should be noted that this vector (032) in zone 2 has an opposite effect on NP voltage in comparison with zone 1. Accordingly, vector 032 in zone 2 results in decrement of NP voltage.

Six look-up tables which are used to increase or decrease the NP voltage in different zones are illustrated in Tables. 2-7. These look-up tables are obtained via mentioned rules (1 through 5).

It should be noted that a vector and its redundant vectors produce the same output line voltage. Therefore, there is no difference between a vector and its redundant vectors from viewpoint of output line voltage. It should be noted that selection of proper look-up table for NP voltage balancing would be done at the start of every SVM cycle (sample time); therefore no change between look-up tables would be done inside the SVM cycle.

5. EXPERIMENTAL RESULTS

5.1.Experimental Setup

A laboratory setup is constructed in order to verify the applicability of the proposed method. The test setup configuration and experimental setup are illustrated in Fig. 3 and Fig. 4. The experimental setup consists of controller board, IGBTs, IGBT drivers, flying capacitors, DC-link capacitors, Diod rectifier, voltage sensors, current sensors, switching power supply, and pre-charge circuit. The power circuit and the relation between different parts are shown in Fig. 3. A float-point TMS320F28335 digital signal processor (DSP) is used to implement the control algorithm. Also there are five voltage sensors for three flying capacitors and two dc-lick capacitors. In addition, two current sensors are utilized for two of three phases. The switching power supply produces the ±15V and 5V for controller board. Results are sampled via an 'Advantech USB-4711A Data Acquisition' apparatus. In the experimental setup, the control method of induction motor is rotor field oriented control (RFOC). Block diagram of RFOC is shown in Fig. 5. It should be noted that in active NPC converter, there are three independent switches in each phase. These switches include *S1*, *S5* and *S7* in phase ‘a’ (*S9*, *S13* and *S15* in phase ‘b and *S17*, *S21* and *S23* in phase ‘c’). States of other switches can be determined via the states of these switches.

The sampling frequency of SVM is 1200Hz. Induction motor parameters are shown in Table. 8.

According to the procedure of voltage balancing (presented in Section. IV), at first the operating zone should be determined; afterwards the proper look-up table according to operating zone should be selected. It should be noted that all of operations for dc-link voltage balancing includes basic logic operators such as 'and', 'or', 'not', etc.

Experimental tests are performed in two conditions; "with NP voltage balancer" and "without NP voltage balancer" in high and low modulation indexes (high and low speed references).

5.2.Case Study 1: High Modulation Index

In this case, as shown in Fig. 3, output dc voltage of the diod-rectifier is applied to the both ends of the full dc-link. In the first two tests (high modulation index), in both conditions of with or without NP balancer, the motor accelerates from standstill to 1500rpm in a ramp wise manner; afterwards a speed command of -1500 rpm is applied to the motor at t=4sec in a ramp wise manner (Fig. 6 and Fig. 7). In results of Figs. 6-7, upper half and lower half of the full dc-link voltages (V_{dc-1} and V_{dc-2}), flying capacitor voltages of each phase and the motor speed are shown. In the condition of "without NP-voltage balancer", flying capacitor voltages of each phase are balanced properly; but upper half and lower half of the full dc-link voltages (V_{dc-1} and V_{dc-2}) have significant difference.

In the condition of "with NP-voltage balancer", upper half and lower half of the full dc-link voltages and also flying capacitor voltages are balanced properly. Specifically, in the duration that motor speed decreases from 1500rpm, full dc-link voltage increases due to regenerative mode of operation. In this duration, as shown in Fig. 7, all of dc and FC voltages are also balanced properly according to the full dc-

link voltage. In addition to proper performance, results show that the proposed method has proper dynamic response.

5.3.Case Study 2: Low Modulation Index

For the tests of low modulation index, the motor accelerates from standstill to 150rpm in a ramp wise manner; afterwards a speed command of -150 rpm is applied to the motor at t=4sec in a ramp wise manner. Same as case study 1, in both conditions of with or without NP-voltage balancer, flying capacitors of three phases are balanced as shown in Fig. 8-b and Fig. 9-b. As illustrated in Fig. 8-a, in the condition of "without NP-voltage balancer", there is a significant difference between upper half and lower half of the dc-link voltages. But in the condition of "with NP-voltage balancer", the both half of dc-link voltages are balanced (Fig. 9-a).

It should be noted that tracking speed of capacitor voltage depends on switching frequency, capacitor value, instantaneous load current, and instantaneous output voltage vector.

5.4.Case Study 3: Under unbalanced load

In the proposed method, the process of neutral point voltage balancing depends on the instantaneous value and the direction of three phase currents which are measured in each sample. As the operating zone is determined via the instantaneous value of three phase currents, therefore the load imbalance does not disrupt the performance of the method.

Also, in order to evaluate the performance of proposed method under unbalanced load, three resistors of 30 Ω, 60 Ω and 90 Ω are utilized as three phase unbalanced load. In this test, output line voltage is 110V and 25Hz. As shown in the results of Figs. 10-11, the flying capacitors are balanced in both conditions of with /without NP-voltage balancer. But there is a significant voltage imbalance between upper half and lower half of the dc-link voltage (Fig. 10-a) in the condition of "without NP-voltage balancer". As shown in Fig. 11-a, dc-link voltage is balanced by the proposed method of dc-link voltage balancer.

6. CONCLUSION

In this paper, a look-up table-based and simplified method with proper implementation capability is proposed for controlling the NP voltage in space vector modulation. In the proposed method, six different look-up tables are determined; these tables are selected in different operating conditions according to the direction of phase currents and comparison of V_{dc-1} and V_{dc-2}. Main advantage of the proposed method is its simplicity in implementation and low computing requirements; because just a few comparative operators are needed to determine the operating zone and requirement for increasing or decreasing the NP voltage.

Experimental results show that this method has proper performance and good dynamic response for balancing the NP voltage in low and high modulation indexes. Also other advantages of proposed method are less computational complexity and simplification of implementation.

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Figure Captions:

Fig.1. Space vectors in the non-orthogonal 60-degree coordinate system

Fig. 2. Five-level Active NPC topology

Fig. 3. Test setup configuration

Fig. 4. Experimental setup

Fig. 5. Block diagram of rotor field-oriented control

Fig. 6. Performance of Active NPC in the condition of "without NP balancer" - motor speed accelerates from standstill to 1500rpm then reference speed varies to -1500rpm at t=4sec in a ramp wise manner
(a) Upper half and lower half of the full dc-link voltage (b) Flying capacitor voltages of three phases (c) Motor speed (d) Motor current (e) Line Voltage

Fig. 7. Performance of Active NPC in the condition of "with NP balancer" - motor speed accelerates from standstill to 1500rpm then reference speed varies to -1500rpm at t=4sec in a ramp wise manner
(a) Upper half and lower half of the full dc-link voltage (b) Flying capacitor voltages of three phases (c) Motor speed (d) Motor current (e) Line Voltage

Fig. 8. Performance of Active NPC in the condition of "without NP balancer" in low modulation index- motor speed accelerates from standstill to 150 rpm then reference speed varies to -150 rpm at t=4sec in a ramp wise manner
(a) Upper half and lower half of the full dc-link voltage (b) Flying capacitor voltages of three phases (c) Motor speed (d) Motor Current (e) Line Voltage

Fig. 9. Performance of Active NPC in the condition of "with NP balancer" in low modulation index - motor speed accelerates from standstill to 150 rpm then reference speed varies to -150 rpm at t=4sec in a ramp wise manner
(a) Upper half and lower half of the full dc-link voltage (b) Flying capacitor voltages of three phases (c) Motor speed (d) Motor Current (e) Line Voltage

Fig. 10. Performance of Active NPC in the condition of “without dc-link voltage balancer” under unbalanced loading - Line Voltage=110V - Fundamental Frequency=25Hz
(a) Upper half and lower half of the full dc-link voltage (b) Flying capacitor voltages of three phases

Fig. 11. Performance of Active NPC in the condition of “with dc-link voltage balancer” under unbalanced loading-Line Voltage=110V - Fundamental Frequency=25Hz
(a) Upper half and lower half of the full dc-link voltage (b) Flying
capacitor voltages of three phases

Table Captions:

TABLE 1
Switching states of phase 'a' of 5-level ANPC

TABLE 2
LOOK-UP TABLE FOR INCREASING NP VOLTAGE IN ZONE 1 AND DECREASING NP VOLTAGE IN ZONE 2

TABLE 3
LOOK-UP TABLE FOR DECREASING NP VOLTAGE IN ZONE 1 AND INCREASING NP VOLTAGE IN ZONE 2

TABLE 4
LOOK-UP TABLE FOR INCREASING NP VOLTAGE IN ZONE 3 AND DECREASING NP VOLTAGE IN ZONE 4

TABLE 5
LOOK-UP TABLE FOR DECREASING NP VOLTAGE IN ZONE 3 AND INCREASING NP VOLTAGE IN ZONE 4

TABLE 6
Look-up table for increasing NP voltage in zone 5 and decreasing NP voltage in zone 6

TABLE 7
Look-up table for decreasing NP voltage in zone 5 and increasing NP voltage in zone 6

TABLE 8
MOTOR PARAMETERS

FIGURES:

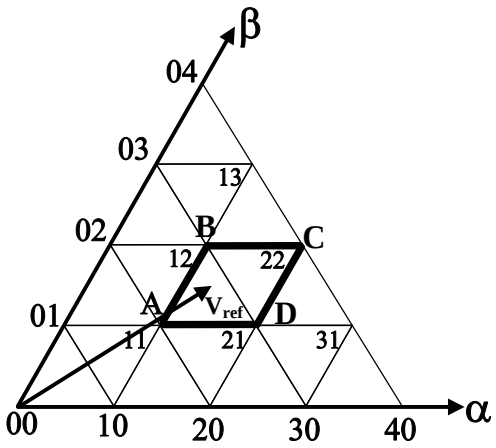


Fig.1. Space vectors in the non-orthogonal 60-degree coordinate system

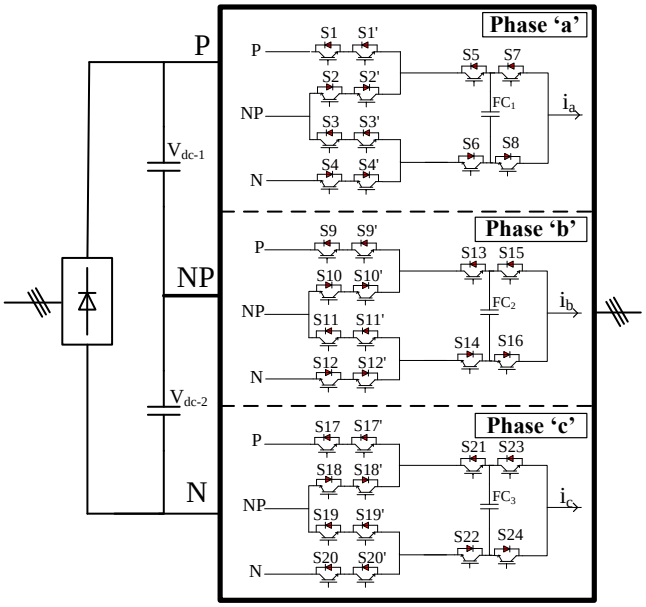


Fig. 2. Five-level Active NPC topology

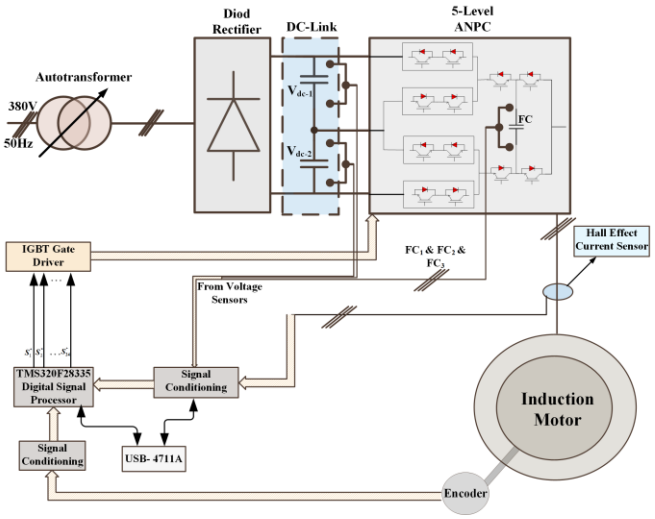


Fig. 3. Test setup configuration

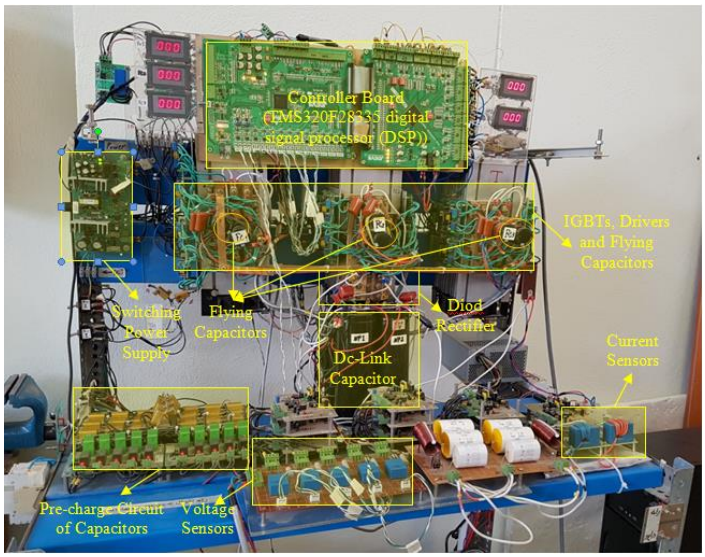


Fig. 4. Experimental setup

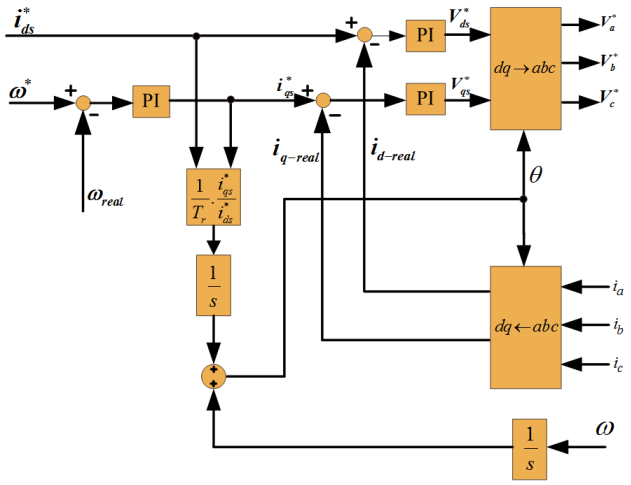
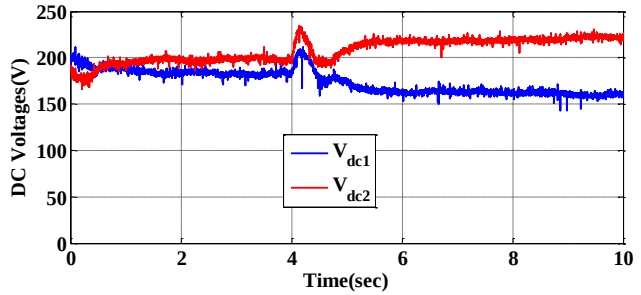


Fig. 5. Block diagram of rotor field oriented control



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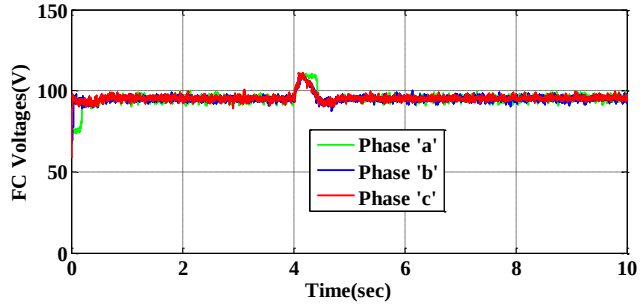

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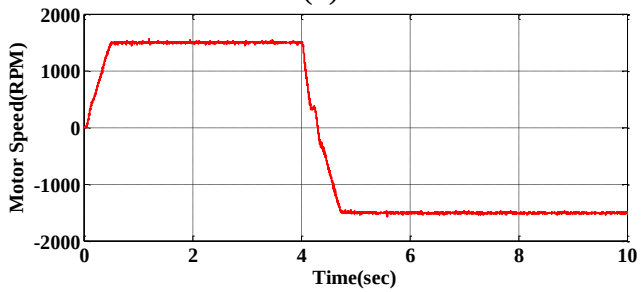

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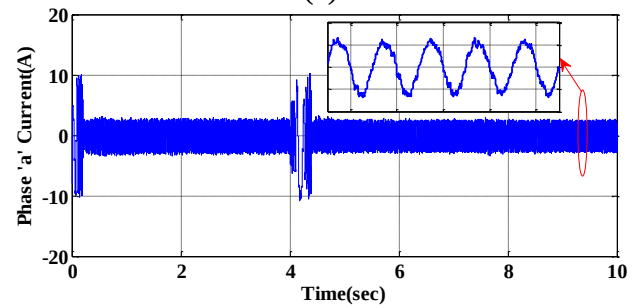

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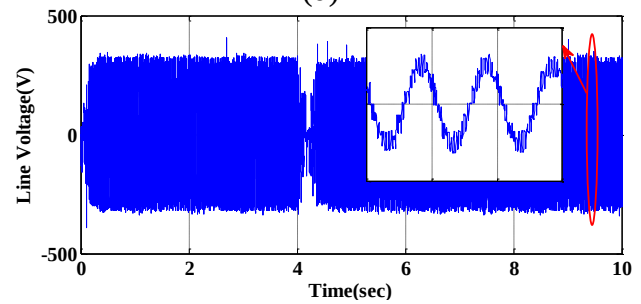
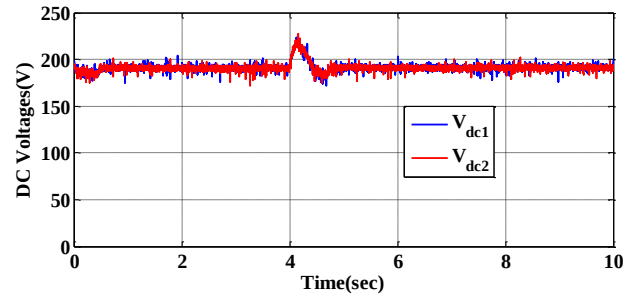


(e)

Fig. 6. Performance of Active NPC in the condition of "without NP balancer" - motor speed accelerates from standstill to 1500rpm then reference speed varies to -1500rpm at t=4sec in a ramp wise manner
(a) Upper half and lower half of the full dc-link voltage (b) Flying capacitor voltages of three phases (c) Motor speed (d) Motor current (e) Line Voltage



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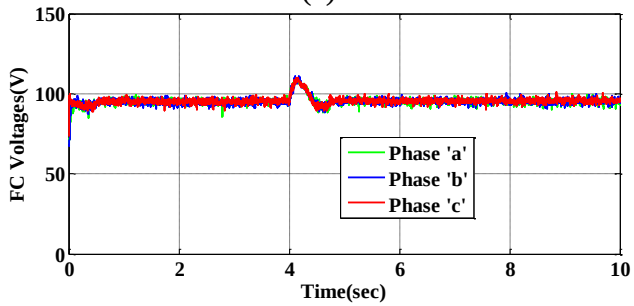

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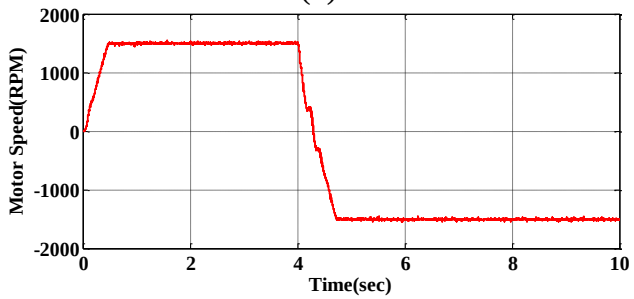

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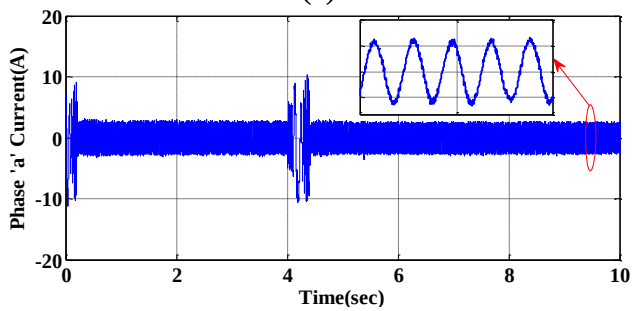

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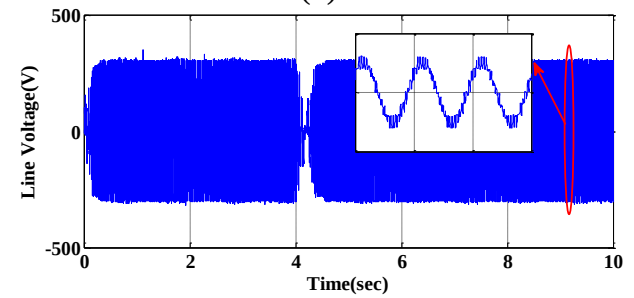
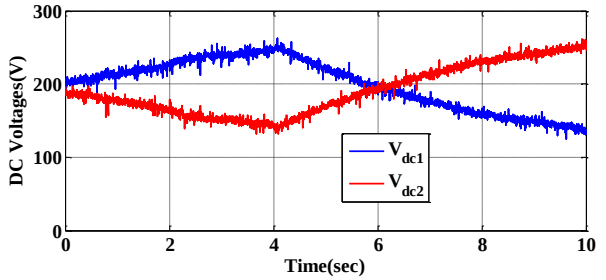


(e)

Fig. 7. Performance of Active NPC in the condition of "with NP balancer" - motor speed accelerates from standstill to 1500rpm then reference speed varies to -1500rpm at t=4sec in a ramp wise manner
(a) Upper half and lower half of the full dc-link voltage (b) Flying capacitor voltages of three phases (c) Motor speed (d) Motor current (e) Line Voltage



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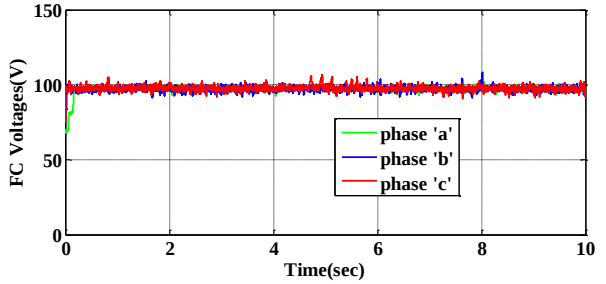

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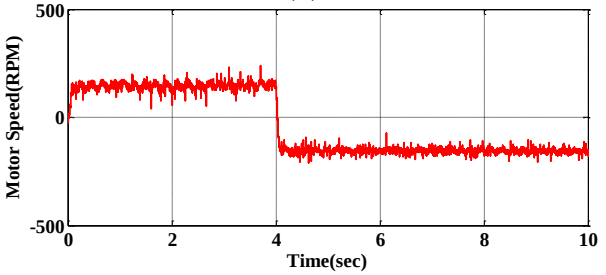

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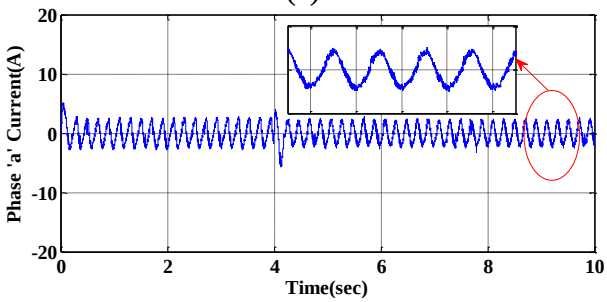

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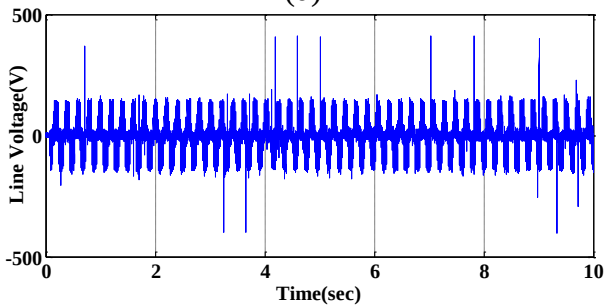
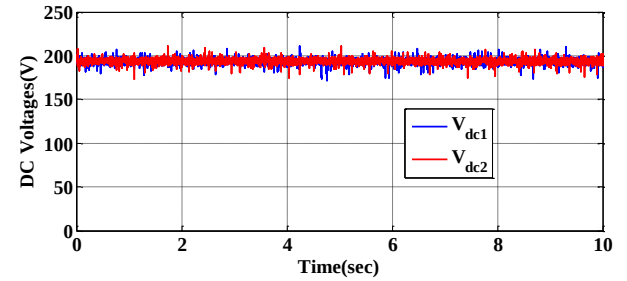


(e)

Fig. 8. Performance of Active NPC in the condition of "without NP balancer" in low modulation index-motor speed accelerates from standstill to 150 rpm then reference speed varies to -150 rpm at t=4sec in a ramp wise manner

(a) Upper half and lower half of the full dc-link voltage (b) Flying capacitor voltages of three phases (c) Motor speed (d) Motor Current (e) Line Voltage



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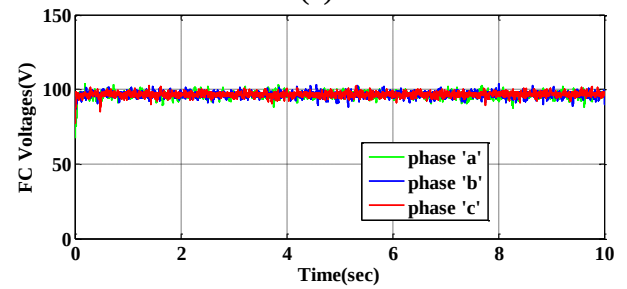

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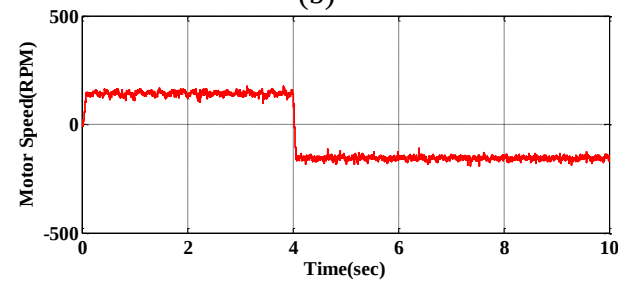

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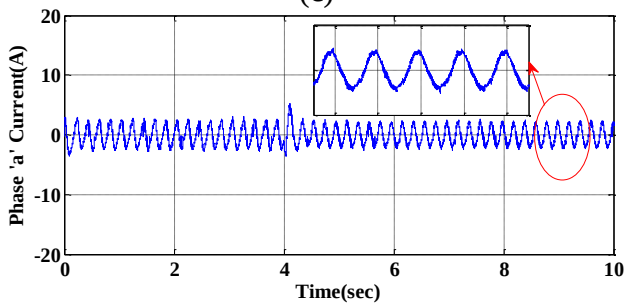

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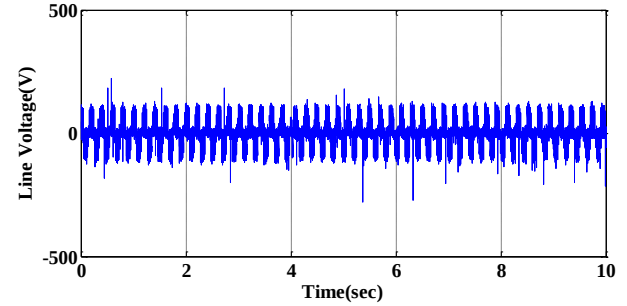

(e)

Fig. 9. Performance of Active NPC in the condition of "with NP balancer" in low modulation index - motor speed accelerates from standstill to 150 rpm then reference speed varies to -150 rpm at t=4sec in a ramp wise manner

(a) Upper half and lower half of the full dc-link voltage (b) Flying capacitor voltages of three phases (c) Motor speed (d) Motor Current (e) Line Voltage

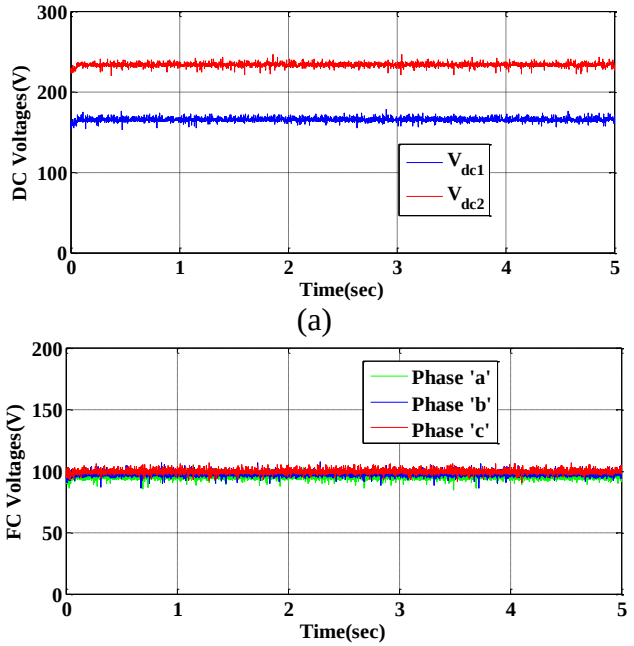

Fig. 10. Performance of Active NPC in the condition of "without dc-link voltage balancer" under unbalanced loading - Line Voltage=110V - Fundamental Frequency=25Hz
(a) Upper half and lower half of the full dc-link voltage (b) Flying capacitor voltages of three phases

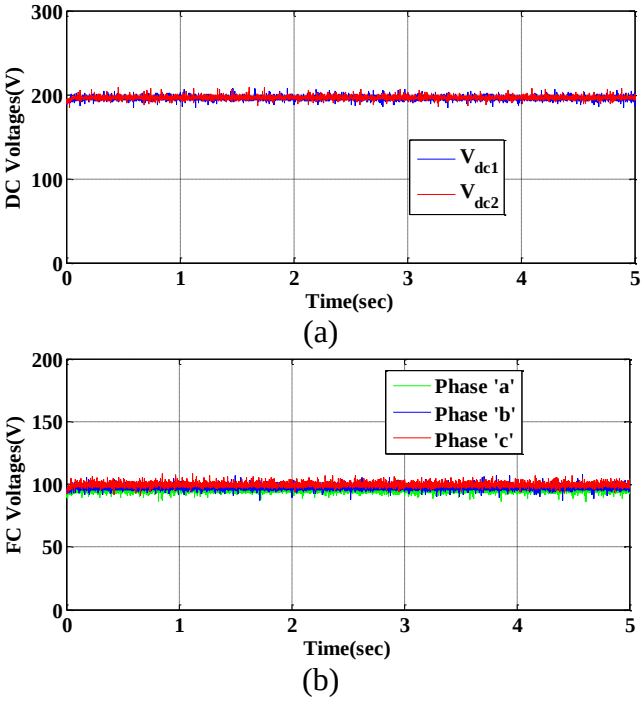

Fig. 11. Performance of Active NPC in the condition of "with dc-link voltage balancer" under unbalanced loading-Line Voltage=110V - Fundamental Frequency=25Hz
(a) Upper half and lower half of the full dc-link voltage (b) Flying capacitor voltages of three phases

.

Tables:

TABLE 1
SWITCHING STATES OF PHASE 'A' OF 5-LEVEL ANPC

Phase voltage level	Effect on FC of phase 'a'		Output voltage of phase 'a' relative to "NP"	(S1,S1',S2,S2',S3,S3', S4,S4',S5,S6,S7,S8)
	$i_a>0$	$i_a<0$		
V_0	0	0	$-V_{dc}/2$	(0,0,1,1,0,0,1,1,0,1,0,1)
V_1	-	+	$-V_{dc}/4$	(0,0,1,1,0,0,1,1,0,1,1,0)
V_2	+	-	$-V_{dc}/4$	(0,0,1,1,0,0,1,1,1,0,0,1)
V_3	0	0	0	(0,0,1,1,0,0,1,1,1,0,1,0)
V_4	0	0	0	(1,1,0,0,1,1,0,0,0,1,0,1)
V_5	-	+	$V_{dc}/4$	(1,1,0,0,1,1,0,0,0,1,1,0)
V_6	+	-	$V_{dc}/4$	(1,1,0,0,1,1,0,0,1,0,0,1)
V_7	0	0	$V_{dc}/2$	(1,1,0,0,1,1,0,0,1,0,1,0)

TABLE 2
LOOK-UP TABLE FOR INCREASING NP VOLTAGE IN ZONE 1 AND DECREASING NP VOLTAGE IN ZONE 2

αβ	-4	-3	-2	-1	0	1	2	3	4
-4					044	043	042	041	040
-3				034	033	032	031	030	140
-2			024	023	022	021	020	130	240
-1		014	013	012	011	010	120	341	340
0	004	003	002	001	000	443	442	441	440
1	104	103	102	434	433	432	431	430	
2	204	314	424	423	422	421	420		
3	304	414	413	412	411	410			

4	404	403	402	401	400				

TABLE 3
LOOK-UP TABLE FOR DECREASING NP VOLTAGE IN ZONE 1 AND INCREASING NP VOLTAGE IN ZONE 2

αβ	-4	-3	-2	-1	0	1	2	3	4
-4					044	043	042	041	040
-3				034	144	143	142	141	140
-2			024	134	244	243	242	241	240
-1		014	124	234	233	232	231	230	340
0	004	114	224	223	222	221	220	330	440
1	104	214	213	212	211	210	320	430	
2	204	203	202	201	200	310	420		
3	304	303	302	301	300	410			
4	404	403	402	401	400				

TABLE 4
LOOK-UP TABLE FOR INCREASING NP VOLTAGE IN ZONE 3 AND DECREASING NP VOLTAGE IN ZONE 4

αβ	-4	-3	-2	-1	0	1	2	3	4
-4					044	043	042	041	040
-3				034	144	143	142	141	140
-2			024	134	244	243	242	241	240
-1		014	013	234	344	343	342	341	340
0	004	003	002	001	000	443	442	441	440
1	104	103	102	101	100	210	431	430	
2	204	203	202	201	200	310	420		
3	304	303	302	301	300	410			
4	404	403	402	401	400				

TABLE 5
LOOK-UP TABLE FOR DECREASING NP VOLTAGE IN ZONE 3 AND INCREASING NP VOLTAGE IN ZONE 4

αβ	-4	-3	-2	-1	0	1	2	3	4
-4					044	043	042	041	040
-3				034	033	032	031	030	140
-2			024	023	022	021	020	130	240
-1		014	124	123	122	121	120	230	340
0	004	114	224	223	222	221	220	330	440
1	104	214	324	323	322	321	320	430	
2	204	314	424	423	422	421	420		
3	304	414	413	412	411	410			
4	404	403	402	401	400				

TABLE 6
LOOK-UP TABLE FOR INCREASING NP VOLTAGE IN ZONE 5 AND DECREASING NP VOLTAGE IN ZONE 6

αβ	-4	-3	-2	-1	0	1	2	3	4
-4					044	043	042	041	040
-3				034	144	143	031	030	140
-2			024	023	244	243	020	130	240
-1		014	124	234	344	010	120	230	340
0	004	114	224	223	222	221	220	330	440
1	104	214	324	434	100	210	320	430	
2	204	314	424	423	200	310	420		
3	304	414	413	301	300	410			
4	404	403	402	401	400				

TABLE 7
LOOK-UP TABLE FOR DECREASING NP VOLTAGE IN ZONE 5 AND INCREASING NP VOLTAGE IN ZONE 6

αβ	-4	-3	-2	-1	0	1	2	3	4
-4					044	043	042	041	040
-3				034	033	032	142	141	140
-2			024	134	022	132	242	241	240
-1		014	013	012	122	232	342	341	340
0	004	003	002	112	444	443	442	441	440
1	104	103	102	212	322	432	431	430	
2	204	203	202	312	422	421	420		
3	304	303	302	412	411	410			
4	404	403	402	401	400				

TABLE 8
Motor Parameters

$R_s(\Omega)$	3.0
$R_r(\Omega)$	2.66
L_m(H)	0.179
L_{ls}(H)	0.0148
L_{lr}(H)	0.0148
Number of Pole Pairs	2
Rated Speed (rpm)	1420
Rated Power (kW)	3