Design and control of a dual-function device with simultaneous DVR and FCL capability

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Abstract-Dynamic voltage restorer (DVR) is a protecting device for sensitive loads which compensates grid voltage fluctuations. Although using fault current limiting devices (FCL) is a method of protecting loads and electrical networks against short circuits. In recent years, some methods have been proposed to combine these two devices to reduce the cost of converters and use the benefits of each device simultaneously. A new topology and control method to combine a DVR and an FCL is presented in this paper, which with just adding a switch to the conventional DVR, the FCL performance will be available for the network. The FCL-DVR has been developed to provide excellent dynamic performance and faster response time to network failures while maintaining appropriate reliability and a low converter cost. The performance ability of the proposed device is investigated by simulation results.

Keywords: Dynamic voltage restorer, Fault Current Limiter, Power electronic converter, Voltage Source Converter, Power Quality.

1. Introduction

A well-known device for protecting sensitive loads from grid-voltage variations is the Dynamic Voltage Restorer (DVR). By injecting correct three-phase voltages in series with the line voltage, this device keeps the load voltage constant [1]. The DVR

usually consists of an injection transformer, a harmonic filter, a voltage source converter (VSC), and a control block [2-3]. The energy for compensating the voltage sag can be achieved by using a parallel transformer or a separate source, where self-recovery management and fast response will be the most important tasks of the control system [4]. In addition to DVRs, Fault Current Limiters (FCLs) are employed to protect sensitive loads from network short circuits. The FCL's can be categorized into three major groups, including: Superconducting Fault Current Limiter (SFCL), Positive Temperature Coefficient (PTC) resistor, and Solid-State Fault Current Limiter (SSFCL) [5].

With recent advancements in high-power semiconductors, SSFCL topologies have sparked a lot of interest. They are divided into three categories: series switches, bridges, and resonant switches. Many methods have been suggested to design solid-state FCLs [6].

In order to provide acceptable power quality for sensitive loads, both voltage fluctuations and short circuit current limiting concerns must be addressed. In recent years, it has become increasingly appealing to combine these two protective devices and create a dual-function FCL-DVR that controls voltage fluctuations while also reducing short circuit current [7-12]. The most significant advantage of this dual function device is the reduction of device components and the realization of a cost-effective converter. It's worth noting that DVRs must guard against network short circuits, thus this combination will automatically solve the problem.

In the literature, some approaches for combining these two technologies have been discussed. In [10], a dual-functional dynamic voltage restorer (DFDVR) is proposed that limits the fault current by controlling a brake chopper circuit and anti-parallel thyristors. The disadvantage of this method is that the fault current is not limited

to the proper range, and in the short circuit mode, a significant current flows through the designed circuit and network. The other approach described in [11] involves connecting the output terminals of a normal back-to-back DVR with a crowbar bidirectional thyristor switch. The same as with the prior design, the main disadvantage is inappropriate fault current restriction (about ten times of nominal current during the fault). A topology for the FCL-DVR is suggested in [12], which employs virtual impedance during the short circuit fault by rerouting the short circuit current through the converter and back to PCC. The drawback of this method is that all off the power semiconductors are in the circuit during the fault.

Unlike previous studies in this field, this work presents a method for changing the available DVR to FCL during a short circuit fault simply by adding an appropriate power electronic switch. The idea is based on changing the Voltage Source Converter (VSC) to a passive rectifier during the fault and splitting the DC bus link to enable fast charging of DC link capacitor. A precise analysis is performed to reveal the effects of each component's value during the short circuit fault. In order to correctly respond to network conditions and control the FCL-DVR system in both of its operational modes, a control approach has been developed. The device is intended to protect a 20kV line by compensating for up to 45% sag voltages and 25% swell voltages while limiting the fault current to 1.7 times the nominal current. Numerous simulations and mathematical analyses are used to show the impact of the proposed DVR-FCL device.

2. Dynamic Voltage Restorer combined with FCL

During system fluctuations, the DVR's performance ensures that the load voltage is maintained properly. When a voltage sag or swell occurs, the DVR injects a voltage in series with the source voltage to maintain the load voltage constant.

However, when a severe fault occurs, such as a ground fault, the DVR, as a series device, should be protected from high current faults. Turning the DVR into an FCL has the advantage of swiftly decreasing the fault current and protecting the DVR and the loads' equipment. The proposed DVR-FCL is shown in Fig.1, where the device is placed in series with the high voltage line. Reforming a DVR with an FCL, bring over the feature of protecting the load transformer against short circuit faults on the load side.

Moreover, this device can help circuit breakers (CB's) disconnect the faulty line properly. Also, there is no requirement to upgrade the CBs during network development and restructuring. When a fault occurs in the network, the short circuit fault is detected by the controller, and the device switches from DVR mode to FCL operating mode, preventing the increase of line current. Although, when the fault is removed, the device switches back to DVR mode and gets ready to compensate subsequent power supply voltage distortion. In this section, the methodology of designing a DVR-FCL device is described.

A. Design method

The parallel and series parts of the proposed DVR-FCL are shown in Figure. 1 for clarity. The series component employs a series Transformer (T2) and three distinct single-phase voltage source converters in order to precisely correct for unbalanced, harmonic, sag or swell voltages in each phase. A three-phase rectifier and parallel transformer are used in the parallel section to produce DC link energy (T1).

When a short circuit fault is detected at the load side, all the VSC switches are turned off by the control system. The device in FCL mode can be modelled as represented in Fig.2. Using the methodology in [13], the effect of each component in the short circuit current for the worth case can be derived using the state variable analysis.

The state variables of the system are shown in equation (1), where L_f and C_f are the values of LC filter, R_l and L_l are the total values of the line and series transformer resistors and inductors, V_S is the fault voltage and C_{DC} is the DC link capacitor. V_{cf}, V_{CDC}, $I_1$and I_f are the voltages of capacitors and inductor currents, respectively.

$$\begin{pmatrix} \frac{dV_{cf}}{dt} \\ \frac{dV_{C_{DC}}}{dt} \\ \frac{dI_1}{dt} \\ \frac{dI_f}{dt} \end{pmatrix} = \begin{pmatrix} 0 & 0 & \frac{1}{C_f} & -\frac{1}{C_f} \\ 0 & 0 & 0 & \frac{1}{C_{DC}} \\ -\frac{1}{L_1} & 0 & -\frac{R_1}{L_1} & 0 \\ \frac{1}{L_f} & -\frac{1}{L_f} & 0 & 0 \end{pmatrix} \begin{pmatrix} V_{cf} \\ V_{c_{DC}} \\ I_1 \\ I_f \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ 1 \\ 0 \end{pmatrix} V_s \qquad (1)$$

Figure. 3 shows the relation between line current and various DC link capacitor values, demonstrating how decreasing the capacitor value will lower the peak value of fault current (C=1pu is referred to the DC-link capacitor in DVR mode). However, a high-value DC link capacitor is necessary for the DVR to operate normally. As a result, in this design, the DC link capacitor is divided into two portions (C1 and C2), with the series S1 switch being deemed to be open when the VSC converter switches are switched off.

As seen in Figure. 1, capacitor C2 remains in the circuit and is not disconnected when the fault occurs. Due to the large size of the DC link capacitance in DVRs, manufacturers typically produce these capacitors by paralleling numerous smaller capacitors for lower production costs. Indeed, capacitor C2 is one of multiple parallel DC link capacitors and has a substantially lower capacitance than the separated capacitance (C1). Due to the design and construction of the DVR, the load current always passes through the high-voltage winding of the T2 transformer during normal operation. This causes current to flow through the LC filter and inverter on the low-

voltage side of the transformer. If the whole capacitance is removed in faulty conditions, the current inside the filter decreases to zero, causing an impulse voltage on the filter inductor. In fact, the proposed design only retains a small portion of the overall capacitance (C2) and cuts off the rest. If the C2 value is set lower than a certain value, the impulse voltage across the filter inductor will be higher than the circuit design and a larger inductor will be required, increasing the design cost. Accordingly, the optimal value in this design for C2 is calculated about 0.06 pu. This prevents the LC filter's current from suddenly changing, which in turn prevents the inductor's generated impulse voltage from occurring. Following the removal of the fault, the S switches and VSC are reset to DVR mode functioning. The DC link capacitance (Cdc) is designed using equation (2) [14–15].

$$W_{rec} = W_{inv} + \frac{1}{2} C_{dc} (V_{dc\max}{}^2 - V_{dc\min}{}^2) \qquad (2)$$

where W_{rec} is the energy supplied to the DC link by the rectifier, W_{inv} is the energy extracted from the DC link by the inverter, $V_{dc\max}$ and $V_{dc\min}$ are the maximum and minimum DC link voltages, respectively, and C_{dc} is the DC link capacitance.

The calculated value is the minimal capacitance that should be used in the DVR mode to keep the required DC link voltage drop within bounds.

2.1.Control Method

This device's control system is divided into two sections. The DVR controlling subsystem is the first part, and the fault current controlling subsystem is the second. Many techniques are suggested in the literature for controlling DVRs. One of the most used control methods is the feedback control method, which is based on calculating the reference voltage of DVR according to the feedback from the load side [16-17]. The

Discrete Fourier Transform (DFT) control technique is used in [18] to determine the amplitude of sag/swell voltages and carry out the necessary compensation.

In this paper, the control approach in DVR mode employs the difference between the load voltages and its desired value as a signal command for the VSI PWM generator, which is very fast to compensate any voltage fluctuations in the source voltage.

The SPWM approach is employed as the modulation technique for VSI since each phase of the converter operates independently [19]. An overview of the various components of controller sections is shown in Figure. 4.

The control subsystems for phase "a" are shown in Figures. 5 through 8; the remaining two phases employ the same architecture.

The error voltage is obtained to be produced by the converter in the DVR mode by subtracting the actual line voltage from the reference voltage in the comparator subsystem (Figure. 5).

The compensation subsystem is designed to adapt the error voltage in accordance with changes in the DC bus due to variations in the DC bus voltage during fluctuations in the line voltage. As seen in Figure. 6, a new coefficient for the reference signal is introduced by dividing the DC link voltage by the intended voltage of the DC link (capacitor voltage at full charge).

When the DC link voltage exceeds the required value, this block multiplies a coefficient less than one by the reference signal; when the capacitor voltage falls, this block multiplies a coefficient higher than one by the reference signal. Line current samples for each phase, are delivered to the fault detector block (Figure. 7), where, in the event of a short circuit fault, this block transmits command signals to the mode

detection block instructing it to switch the operating mode from DVR to FCL (Figure. 8).

When a short circuit occurs, the "S" switches are detached; however, after the fault is cleared, they do not reconnect unless the voltage difference between C1 and C2 falls below the specified small value (10 V in this design). The "mode detection subsystem" will activate the crowbar IGBT and connect a suitable resistor in parallel with the DC link capacitors to lower the voltage if it detects any voltage difference between the C1 and C2 capacitors. The control system permits the S switches to reconnect when the difference between the capacitor voltages falls below the threshold value. It should be noted that this approach does not disrupt or impede the limiting process. The mode detection subsystem of the control system prepares the VSC IGBTs, “S” switches and Crowbar IGBT commands with the logical control system.

3. Simulation results

This section simulates the approach described in the paper and presents and analyzes the outcomes of device performance in various operating modes. Table. 1 provides a list of circuit parameters.

3.1. Device performance during the sag voltages

Three-phase Sag voltages with 45% depth, beginning at 0.1 seconds and lasting for 0.2 seconds is provided to show the device performance during the Sag voltage. As shown in Figure. 9, the proposed device is activated in DVR mode instantly after the sag voltage is detected and compensates the reduced voltage.

The waveforms clearly show the device's operating speed, which begins to correct for less than one-hundredth of a second after the sag voltage arises and helps to maintain a balanced three-phase load voltage at its nominal value. As seen in Figure 9,

when the sag voltage is removed, the output of this device becomes zero and returns to standby.

3.2.Device performance during the swell voltages

Figure. 10 depicts the suggested device's performance for a three-phase swell voltage. In this section of the simulation, a swell voltage of 1.25 per unit of nominal voltage is evaluated. Figures. 10 (a) to (c), respectively, depict the source voltage with the swell, the injected voltages of the suggested device with the proper phases and amplitudes, and the sensitive load voltages that have not altered. As is evident, the protective mechanism acts quickly and eliminates the voltage fluctuations. Following the detection of swells, the device injects voltages with the proper amplitudes and a 180° phase difference from the source phases.

3.3.Device performance during the unbalanced power supply

Load protection against unbalanced voltages is another aspect of the proposed device. The device with high dynamic compensates for any source voltage unbalance and sets up the proper load voltage thanks to the quick control mechanism.

Figure. 11 shows that the voltage source becomes significantly unbalanced at 0.15 sec. As can be seen, phase "a" in this period is equal to 0.9 per unit, phase "b" to 0.55 per unit, and phase "c" to 1.25 per unit. The suggested device injects voltages in phases "a" and "b" with the same phases and adequate amplitudes, while in phase "c" it injects a voltage with a 180° phase difference from these phases to reduce the overvoltage and keep the load voltages constant.

3.4.Device performance during the harmonic voltage

This device offers a quick and desired reaction to voltage harmonics, according to the suggested device controller. A third-order harmonic with an amplitude of 0.25 per unit and a fifth harmonic with an amplitude of 0.15 per unit are carried by the power supply in Figure. 12. This figure illustrates how the protective device performs in the presence of harmonic source voltage. As can be seen, this device responds very well and injects voltages into the system to minimize the influence of these harmonics on the sensitive load.

3.5.Device operation in a three phase to ground fault

This section analyzes how the device reacts to short circuit faults and simulates one of the worst fault types. This protection device limits the currents of all three phases in the event of a short circuit fault in one or two phases.

It should be emphasized that the short circuit current limiting is the priority mode in the proposed control. If a sag or swell voltage detection coincides with a short circuit fault on the sensitive load side, the device will enter fault current limiting mode and remain in this mode until the fault is removed. An appropriate FCL should be capable of limiting the sudden current surge that occurs at the start of a short circuit fault. In most designs presented in the field of limiters, the fault current amplitude at the beginning will reach up to about 2.5 per-unit in the best limiting operation, which needs to consider high extra value for element design. In the proposed design, it will be shown that the fault current will not exceed more than 1.7 per-unit in its first peak, which is a significant advantage of this design.

One of the worst short circuit conditions is three phases to ground fault, thus the device response to this fault is simulated. Figure. 13 depicts the line current and the C2

portion of the DC link capacitor current during a three-phase fault to ground. The peak current reaches to 1700A and shortly restricted to very low current following through the filter capacitor during the short circuit. The device is in FCL mode, and the short circuit current is correctly limited.

3.6.The output voltage of VSC

In this section, the output voltage of VSC in each mode is shown. The study is performed in three different conditions. First, a sag fault with 45% depth, second a 1.25 per-unit swell fault, and finally, a three phase to ground fault is applied to the system. It should be noted that this analysis is only performed on one phase of the device, but the other two phases function similarly.

As can be seen in Figure. 14, the maximum inverter output voltage belongs to the swell condition, which is about 3500 volts. Therefore, in this design the switches should be able to withstand a voltage of 3500 volts. This is due to the rise of voltage on the primary winding side of the T1 transformer, which causes the DC link voltage to rise, and then, inverter output voltages are increased. The voltage reaches to 3500V because the threshold voltage of the crowbar resistor is set to 3500V to protect the device from overvoltage. This voltage in the output can be decreased so that lower voltage switches can be utilized in the inverter if the threshold value is set to lower values.

As shown in Figure 14, the voltage of the inverter during the short circuit (t=0.88s to 1s) is less than its voltage during the sag/swell voltage, implying that in the proposed design, a typical DVR can be utilized as a fault current limiter with minor structural modifications and without changing the power of its elements.

4. Conclusion

The proposed solution offers a new topology and structure to upgrade the standard DVR to include fault current limiting functionality without modifying the baseline power of the DVR parts. The suggested control method in the DVR mode compensates for all source voltage variations, including harmonic content, unbalanced voltages, and sag/swell voltages. Additionally, this design can control the sudden current surge that occurs at the start of a short circuit fault. The simulation results demonstrate the suggested design's capacity to deliver quick and precise compensating voltage as well as effective fault current limiting.

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Table 1.

Circuit elements	Element value
Voltage Source	3ph, 20 KV, 50 HZ
Sensitive Load	3ph, 380 V, 50 HZ , 500 KW, 500 VAR (QL)
T1 transformer	Yg-Yg, 200 KVA, 50 HZ, 20KV/1.85KV
T2 transformer	200 KVA, 50 HZ, 3KV/20KV
T3 transformer	Yg-Yg, 1000 KVA, 50 HZ, 20KV/380V
Thevenin impedance (Z_{th})	R_{th}=0.5 mΩ, L_{th}=0.5 mH
LC filter inductor and capacitor in each phase	L=250 µH, C=15 µF
C1 capacitance	5.99 mF
C2 capacitance	0.4 mF
Crowbar resistor	50 Ω

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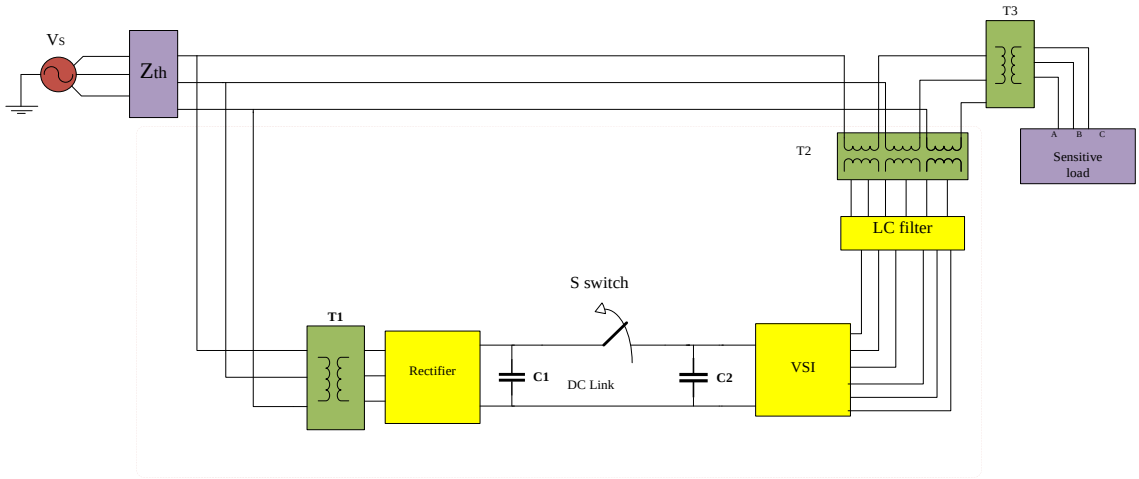

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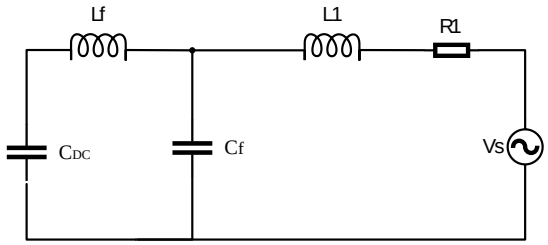

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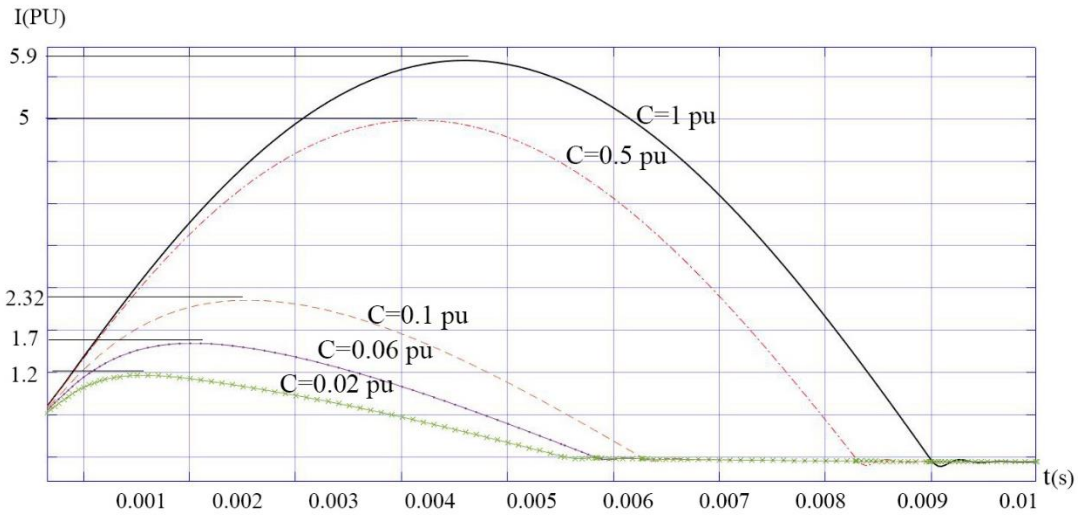

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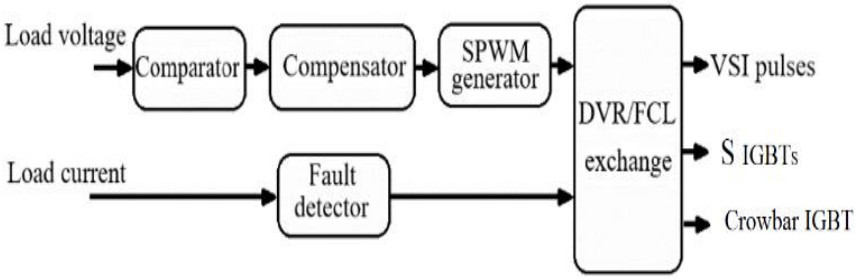

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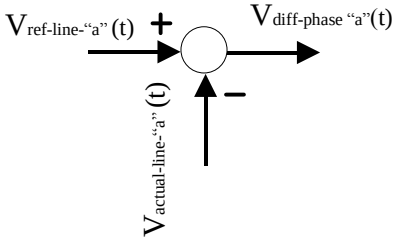

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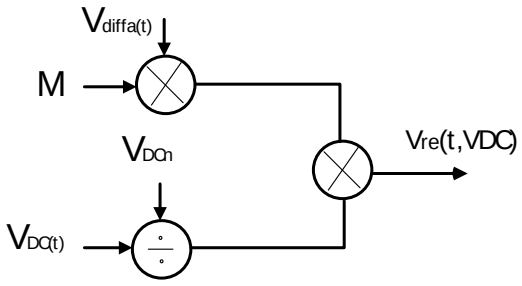

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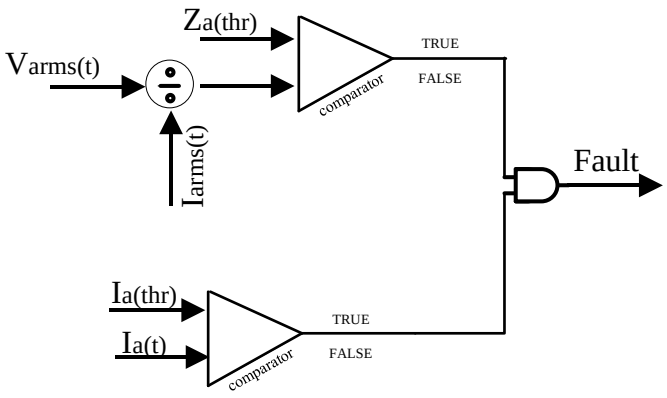

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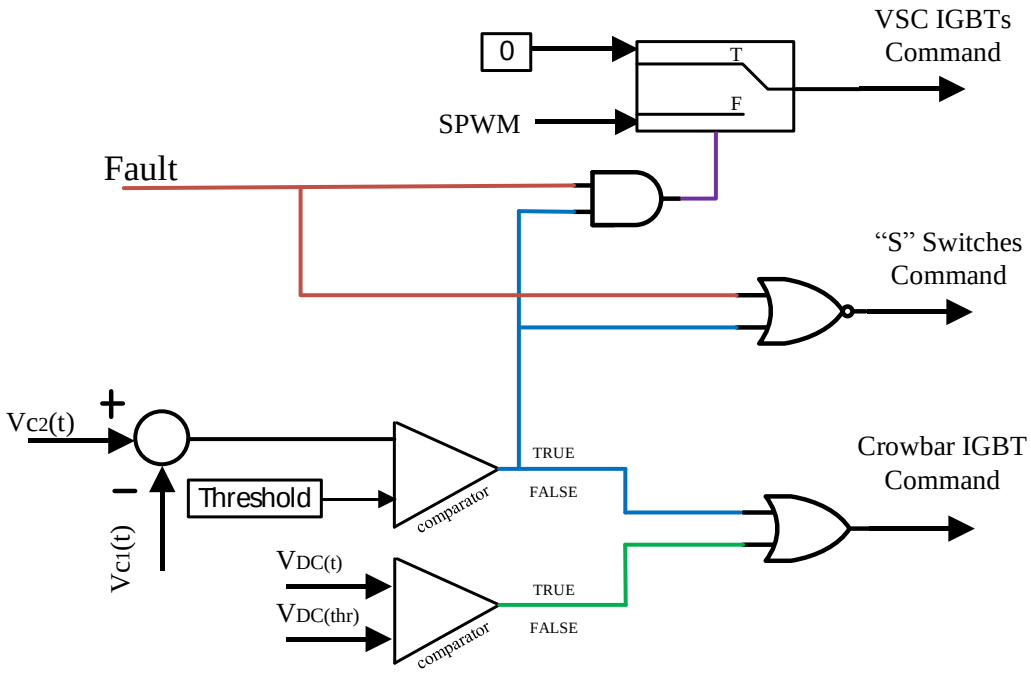

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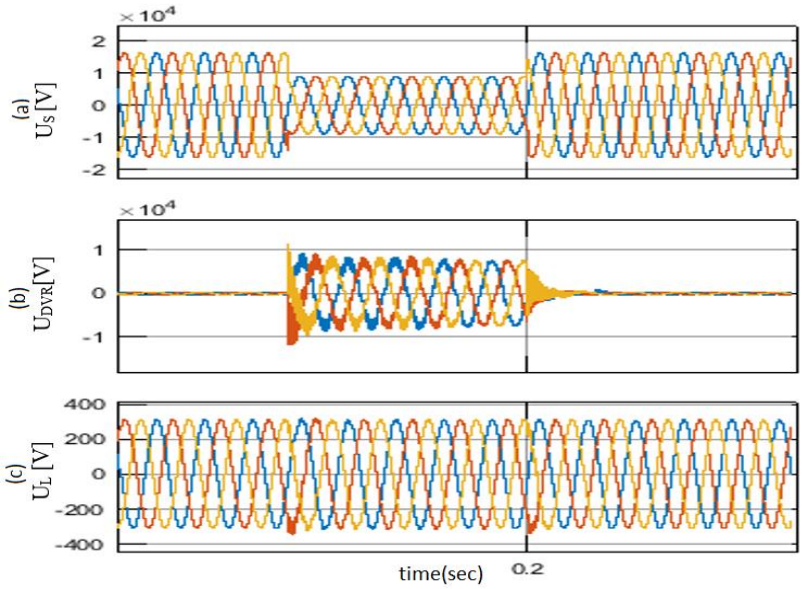

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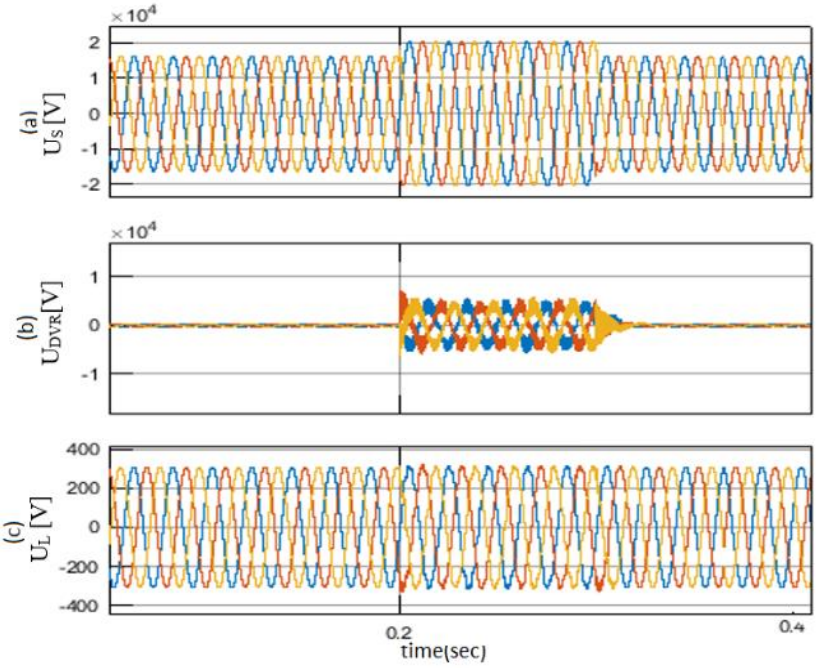

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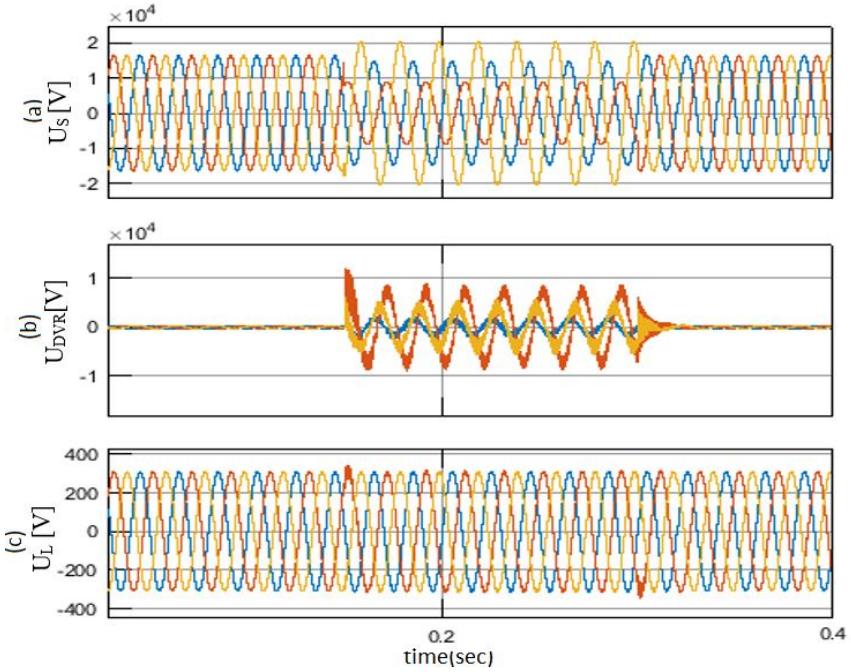

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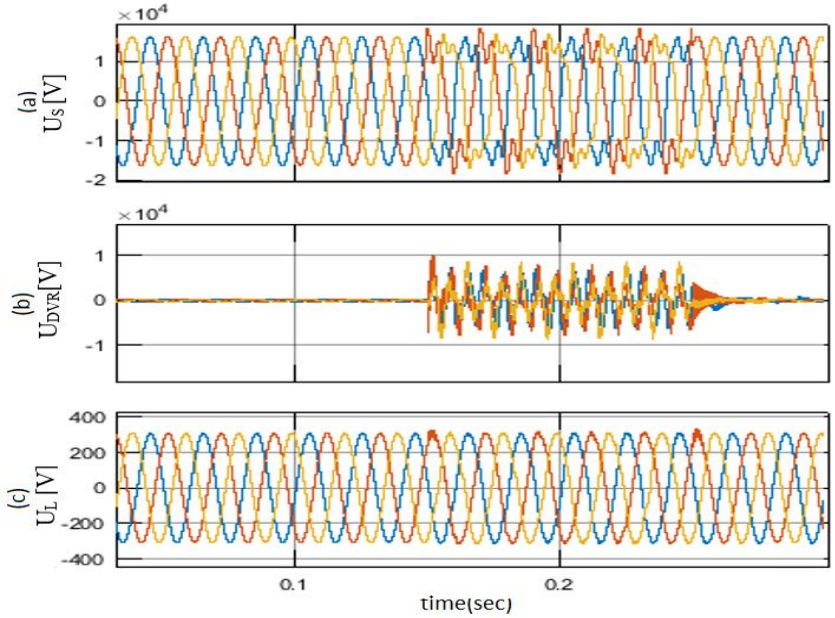

Figure 12.

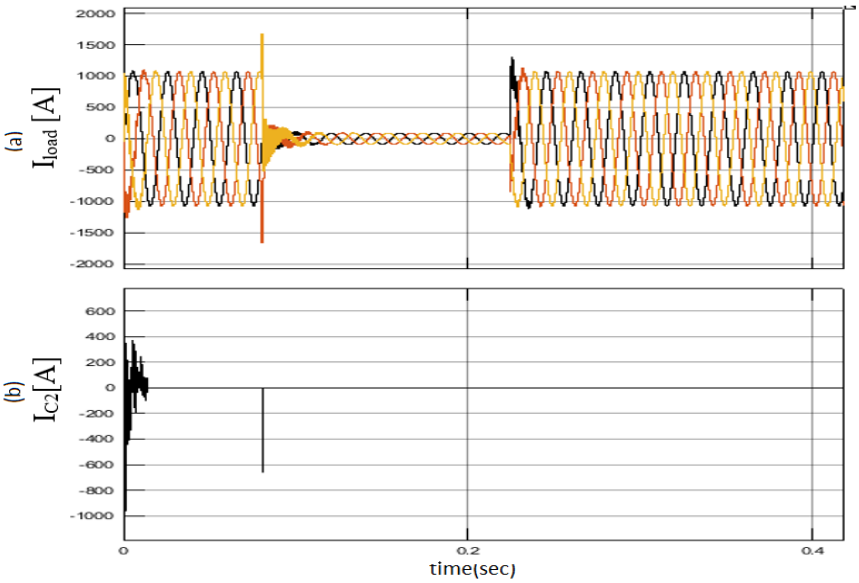

Figure 13.

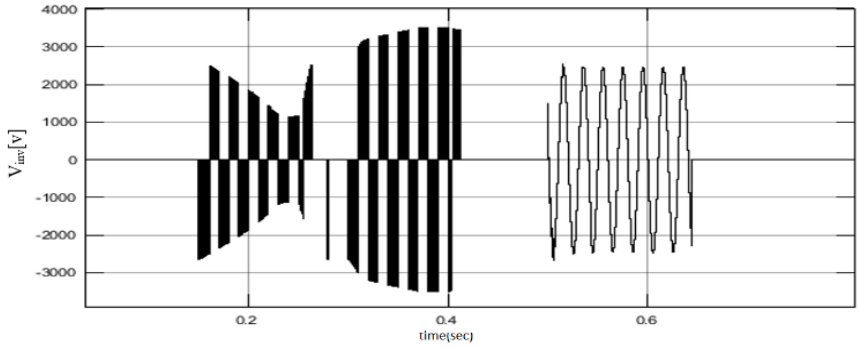

Figure 14.

Biographies

Amir arsalan astereki was born in ahvaz, Iran, in 1992. He received the B.Sc. in Electrical Power Engineering from Jundi Shapur university of Technology, in 2015 and M.Sc. degree in Electrical Machines and Power Electronics from Jundi-Shapur university of Technology, Dezful, Iran in 2019. His research interests include power quality, power system protection, renewable energies and smart grids.

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