Scientia Iranica D (2023) 30(2), 477–491

Sharif University of Technology
Scientia Iranica
Transactions D: Computer Science & Engineering and Electrical Engineering
http://scientiairanica.sharif.edu

Cost-effective architecture of decoder circuits and futuristic scope in the era of nano-computing

B. Kumar Bhoi[a], N. Kumar Misra[b,*], and P. Bharti[a]

a. *Department of Electronics and Telecommunication, Veer Surendra Sai University of Technology, Burla, Sambalpur 768018, Odisha, India (Orchid Id: 0000-0003-2916-2903).*
b. *School of Electronics Engineering, Vellore Institute of Technology (VIT) - AP University, Amaravati, Andhra Pradesh, India (Orchid Id: 0000-0002-7907-0276).*

Received 1 August 2021; received in revised form 28 May 2022; accepted 19 September 2022

KEYWORDS
QCA;
Decoder;
Majority gate;
Nano-computing;
Nanometer-scale;
Nanostructures;
Devices.

Abstract. Over the past several decades, the goal of Very Large-Scale Integration (VLSI) has been to miniaturize chip size while increasing computing speed and lowering power consumption. At this time, miniaturisation of size, high computing speed, and low power consumption do not appear to be capable of meeting consumer demand due to limitation in transistor geometry. Quantum dot Cellular Automata (QCA) is a more promising methodology with the potential to optimize power, speed, and area on a nano scale. Combinational circuit design has received a significant amount of research and development attention in the field of nano-computing. This article proposed design of a decoder with an accurate clocking mechanism in QCA and the best design. In terms of cell count, total area, cell area, area coverage, latency, QCA cost, and quantum cost, the novel 2-to-4 decoder achieves values of 87, 0.10 μm^2, 0.0281 μm^2, 28.1, 2.5, 0.625, and 0.25, which is better than the prior work. In comparison to a standard design, the improvements in cell count, total area, cell area, area coverage, latency, QCA cost, and quantum cost are 72.64%, 80%, 72.71%, 28.1%, 64.28%, 97.44%, and 92.85%, respectively.

1. Introduction

A decoder is a type of combinational circuit that can be found in many different circuits, including seven-segment displays, memories, Field Programmable Gate Arrays (FPGAs), Configurable Logic Blocks (CLBs), Programmable Logic Array (PLAs), and microcontrollers. The Quantum dot Cellular Automata (QCA) is a more effective computing technology that has been validated for the nano-scale [1]. In the QCA design, the logical information is transmitted by electron polarization due to Columbic interaction in the quantum cell, whereas in the CMOS design, transmission is accomplished through the charging and discharging concept [2].

This article discusses the design of decoders based on the QCA paradigm, including design implementation and simulation within the context of QCA technology. The Majority Gate (MG), which is a type of logic gate, makes it possible to perform QCA computing at the level of logic gates. The interaction between quantum dots in a quantum computing array generates logic information that is stored in each cell

*. *Corresponding author.*
E-mail addresses: bkbhoi_etc@vssut.ac.in (B. Kumar Bhoi); neeraj.mishra3@gmail.com (N. Kumar Misra); prityb28@gmail.com (P. Bharti)

doi: 10.24200/sci.2022.58661.5846

of the array. This interaction is caused by the direction in which electrons flow. QCA technology, which encodes logic information using electrons rather than current and voltage levels, is fundamentally distinct from conventional digital logic gates [3], which is an important point to keep in mind. QCA technology encodes logic information using electrons.

The proposed effort aims to take this technology one step further by providing a robust design of the decoder architecture in QCA technology. We designate decoder types such as 2-to-4, 3-to-8, and 4-to-16 in QCA technology with low values for cell count, total area, cell area, area coverage, and latency. We also aim to synthesize decoders with low QCA costs. The small cell count implies that less space is needed to accomplish the requisite logic function, and the low clock latency implies that the circuit would operate with less delay. In the future, the suggested circuits will be more competent and better suited for complicated circuit design because of their unique characteristics. Essentially, the suggested decoders have a robust structure and a fast speed. This study will make a substantial contribution to the design of PLAs, microcontrollers, and CPUs in the future.

The main contribution is highlighted as follows:

1. We have designed compact 2-to-4, 3-to-8, and 4-to-16 decoder circuits using coplanar crossover technique in QCA technology;
2. We have measured parameters based on a QCA-based simulator in the proposed decoder circuits;
3. The new decoders are synthesized by an efficient clocking mechanism using QCADesigner 2.0.3 tool;
4. The new decoders are compared with existing designs from the latest works to check the superiority over other circuits.

This article is organized as follows: Section 1 discusses an introduction to the QCA technology. Section 2 elaborates on the preliminaries. Section 3 discusses related works. Section 4 presents the proposed decoder circuits. Section 5 provides the QCA environment and compares the work to existing work. Finally, Section 6 concludes this paper with final remarks.

2. Preliminaries

As illustrated in Figure 1, the essential building block of QCA is the cell, which includes four-dot and two-electron configurations. Figure 2 depicts the polarized and un-polarized conditions in the QCA, as well as the binary logic 0 and 1 stored in the QCA [3]. Polarization states $P = -1$ and $P = +1$ are used to encode the binary numbers '0' and '1', respectively. QCA cells are made from four quantum dots, which are placed at the four corners of the cell to form the

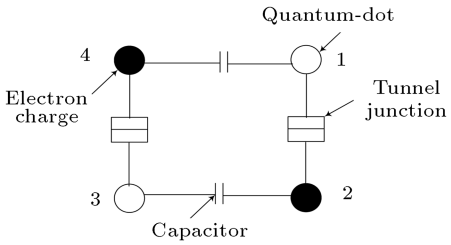

Figure 1. Basic QCA cell.

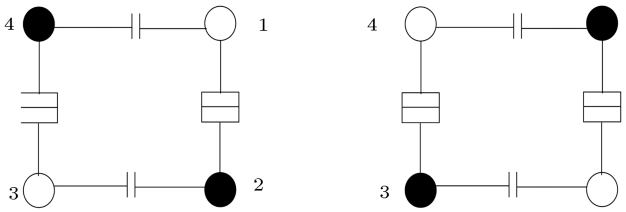

Figure 2. Symbol of logic states: (a) State-0 and (b) state-1.

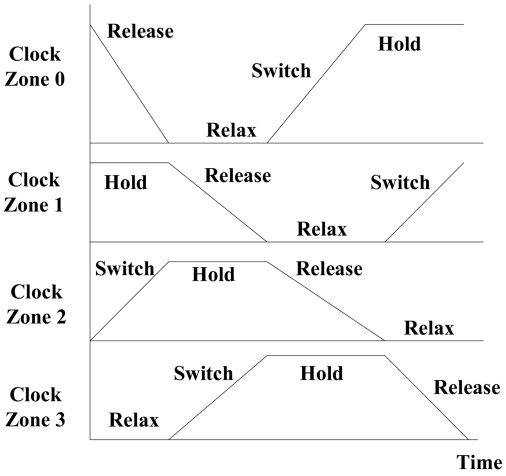

Figure 3. Clocking in QCA.

cell. Because of Columbia repulsion [4], these electrons will be placed diagonally apart from each other at the greatest possible distance. Tunnel connectors, as depicted in Figure 2, are used to connect the various sections of the tunnel. QCA cells [5] are responsible for the construction of three fundamental structures: the MG, the wire, and the inverter. In order to design a QCA wire, a set of QCA cells must be positioned back to back in a configuration where one input and one output cells are present. The binary information flows from the input cell to the output cell with no change at the output cell. QCA clocking is used to provide synchronization and required power between QCA cells [6,7]. Four different types of clock signals that are present between QCA cells are switch, hold, release, and relax [8–10], as shown in Figure 3. The barriers in quantum dots start to increment in the switch stage, while in the hold stage, the barrier holds the high energy that the cell turns into polarized and

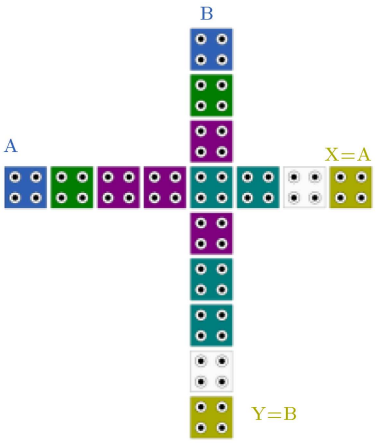

Figure 4. Clock zone-based crossing technique.

holds previous values [11–13]. After the barrier starts to decrement in the release stage, the barrier holds a low energy level in the relax stage and then, the cell becomes an un-polarized state [14–17]. An array of QCA cells with the crossing technique [18] is presented in Figure 4.

3. Related work

Based QCA [1] offers a new paradigm for computation using digital logic circuits. A novel nano-electronic architecture based on cells was presented in [3] and it is composed of quantum dots that are connected. It depicts the manner in which the layout of quantum dot cells may be utilized to carry out suitable computations using the quantum dot cell architecture. Logic devices on a nano scale, such as QCA, were proposed for the first time by Craig S. Lent [4], who was the first to suggest their implementation. In this particular situation, the researchers expressed interest in whether the two electrons situated by each quantum cell were coulombic with the electrons held by the surrounding cells. These cells are in charge of transmitting binary logic information. A variety of circuits, including inverters, MG, and wire crossing circuits, rely on the QCA cell for its operation and design. A metal-dot cell that was linked to a tunnel junction, as well as an electrolytic capacitor, is the subject of the investigation. Due to recent demonstrations, it has been proven that arrays of cells might be utilized to construct logic gates which represent binary information, thus the term "Quadric Cell Array." Based QCA offers a new paradigm for computation using digital logic circuits. It depicts the manner in which the layout of quantum dot cells may be utilized to carry out suitable computations using the quantum dot cell architecture. It was shown in [5] that a cost-effective QCA reversible circuit based on the crossing of the clock zone could be constructed and the viability of it was realized in [6]. The authors suggested that QCA would be a low-cost nanotechnology associated with computer technologies in the future. In [7–10], a design for a 2-to-4 decoder in QCA was created to increase energy dissipation via the decoding process. The suggested decoder is used in the development of n-to-2n decoders, which are described below in detail. In [9], the authors created a 3-to-8 decoder based on QCA which required small crossover values to function properly. The design for a 4-to-16 decoder was demonstrated in [15]. In light of this, we have developed a new decoder circuit that has a smaller cell count and less latency than the previous one. It is possible to reduce the complexity of a circuit using the MG and coplanar crossing methods in combination with decoders, leading to a circuit with a low latency value. The simulation of the newly constructed circuits is carried out with the assistance of the QCADesigner 2.0.3 software package. In order to assess whether or not the innovative decoder circuits are superior to their previous designs, it is required to compare them to existing designs.

4. New design of decoder architecture

The decoder alters the binary-coded input to output only if both of these are not similar to one another. The decoder types such as 2-to-4, 3-to-8, and 4-to-16 lines are the most commonly used binary decoders. Decoder circuits are used in code conversions. The general schematic of the n-to-2n decoder is drawn in Figure 5(a). In the 2-to-4 decoder, only one output remains active at a time, whereas the other remains in the logic state (0). The complete schematic of the 2-to-4 decoder is shown in Figure 5(b). Generally, the

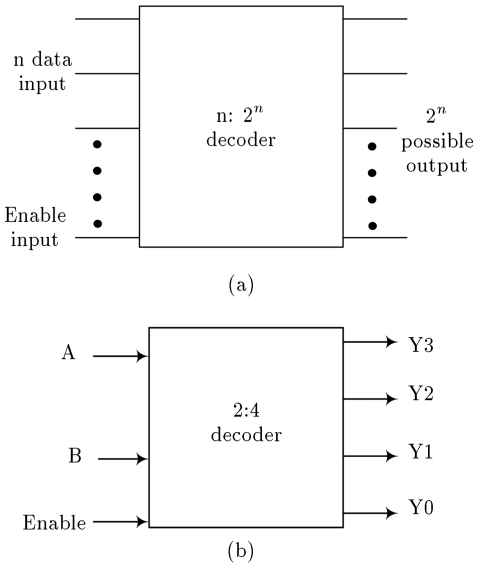

Figure 5. Block diagram of decoder (a) n-to-2n (b) 2:4 circuit.

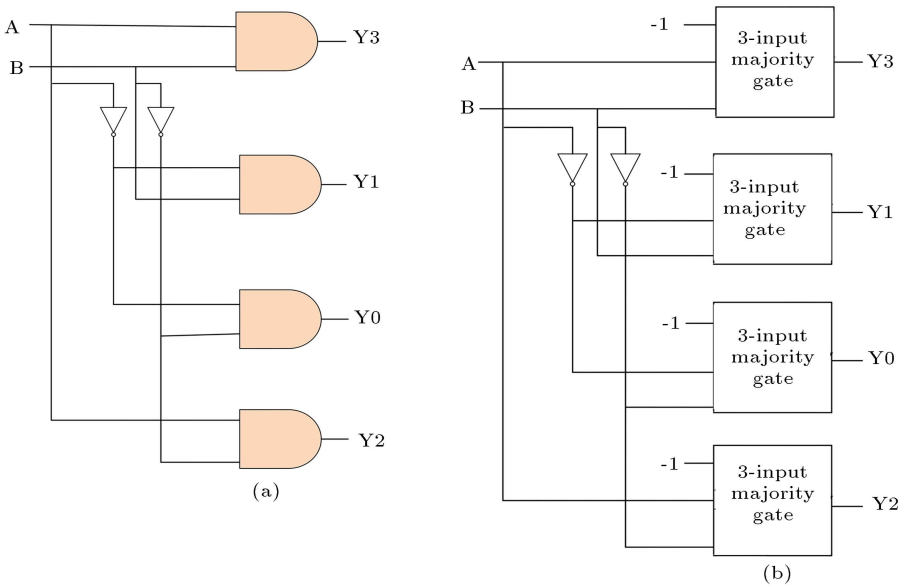

Figure 6. Decoder 2-to-4 circuit: (a) Logic diagram and (b) block diagram using MG.

sum of the bits in the output code has a larger number of bits than the input code.

The general Boolean expressions of the 2-to-4 decoder for each output are expressed as follows:

$$Y_3 = AB, \quad Y_2 = A\bar{B}, \quad Y_1 = \bar{A}B, \quad Y_0 = \bar{A}\bar{B}.$$

As shown in Figure 6(a) and (b), the detailed logic diagram and block diagram employing MG are used to create the final product. Figure 7 depicts the 3-input majority voter gate-based 2-to-4 decoder used in QCA, which has three inputs. It can be seen that the four numbers of MG consist of two inputs and two outputs, respectively. The logic level at the output node is determined by the polarization values of the majority of the input levels at each of the input nodes in the circuit. Figure 8(a) and (b) show the simulation results based on the bus configuration and logic level, respectively.

4.1. New design of 3-to-8 decoder circuit

The MG is useful since it can handle a wide variety of logics, such as NAND and NOR gates. Figure 9 depicts a new 3-to-8 decoder scheme that has been developed. Figure 10(a) and (b) depict the logic and block diagrams based on the model generated by MG. It can be obtained by decoding three inputs to get eight outputs. Figure 6 shows the block diagram of the 3-to-8 decoder circuit.

The general Boolean expressions of 3-to-8 decoder for each output are expressed as follows:

$$Y_0 = \bar{A}\bar{B}\bar{C}, \quad Y_1 = \bar{A}\bar{B}C,$$

$$Y_2 = \bar{A}B\bar{C}, \quad Y_3 = \bar{A}BC,$$

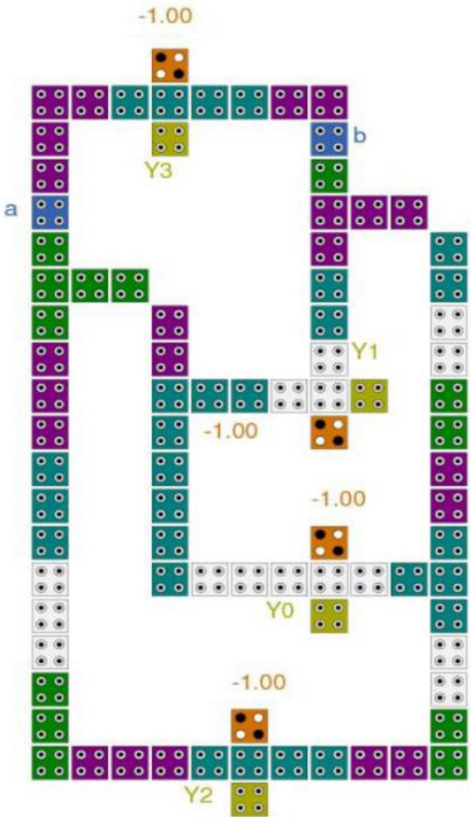

Figure 7. Layout of 2-to-4 decoder circuit.

$$Y_4 = A\bar{B}\bar{C}, \quad Y_5 = A\bar{B}C,$$

$$Y_6 = AB\bar{C}, \quad Y_7 = ABC.$$

It is apparent from the QCA layout of the 3-to-8 decoder in Figure 11 that the proposed 3-to-8 decoder has a small cell count and minimal majority gates.

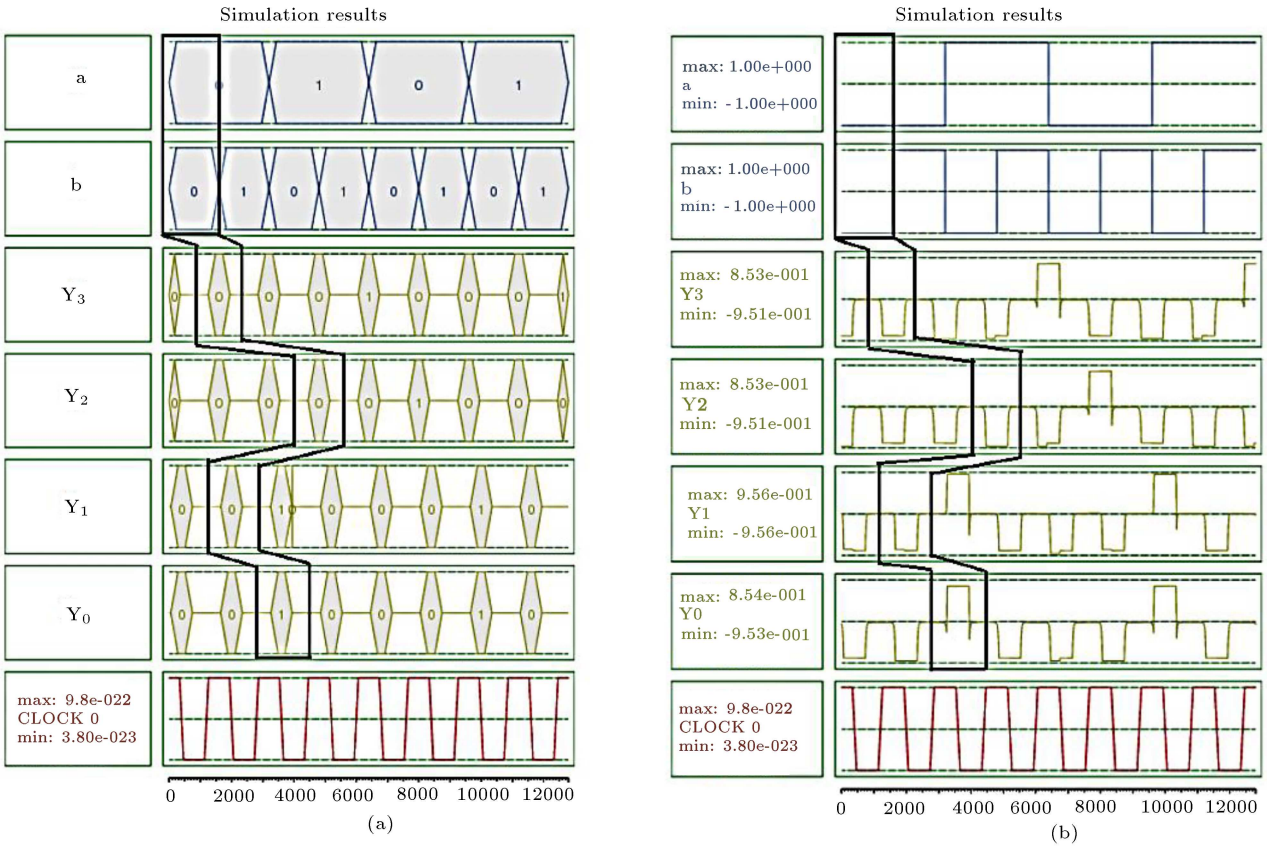

Figure 8. Simulation result of 2-to-4 decoder: (a) Bus-layout and (b) output waveform.

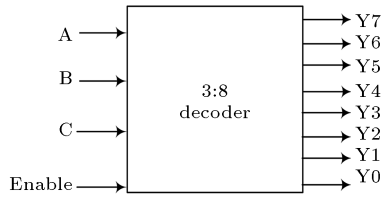

Figure 9. General schematic of 3-to-8 decoder circuit.

Based on the simulation results of the 3-to-8 decoder in Figure 12, the logic of the 3-to-8 decoder function is successfully implemented. Figure 12(a) and (b) represent the simulation using the bus and input/output waveform of the 3-to-8 decoder, respectively.

4.2. New design of 4-to-16 decoder circuit

The logic of a 4-to-16 decoder can be obtained by cascading two 3-to-8 decoder circuits. Whenever two 3-to-8 decoder circuits are cascaded, which enable (E) to perform as input. When an input (E) is active in the upper circuit, it is deactivated in the lower circuits. The complete schematic of the 4-to-16 decoder is presented in Figure 13(a). Figure 13(b) depicts the logic diagram of the 4-to-16 decoder. One inverter is connected to enable (E) for the second module of the 3-to-8 decoder and, hence, to enable (E) to act as a controller, as shown in Figure 13(a). The detailed QCA schematic and layout of the 4-to-16 decoder circuit are presented in Figure 14(a) and (b), respectively. Figure 15(a) and (b) represent the simulation using the bus and input/output waveform of the 4-to-16 decoder, respectively.

5. Default QCA environment parameters and comparison results

This section presents the findings of an investigation into suggested decoder circuits, which includes a comparison of various characteristics such as cell count, total area, cell area, area coverage, latency, QCA circuit cost, and quantum cost. All of the calculated parameter values that the QCA designer will need to use in their simulation are presented in Table 1.

5.1. Circuit complexity

The design and analysis have shown that the proposed circuit has a lower degree of circuit complexity and delay than the current circuit, which is advantageous. The innovative decoders are compared to current designs from literature research based on cell count, total area, cell area, area coverage, latency, QCA circuit cost, and QCA-quantum cost, among other metrics. Tables 2, 3, and 4 are the three tables that explain decoders

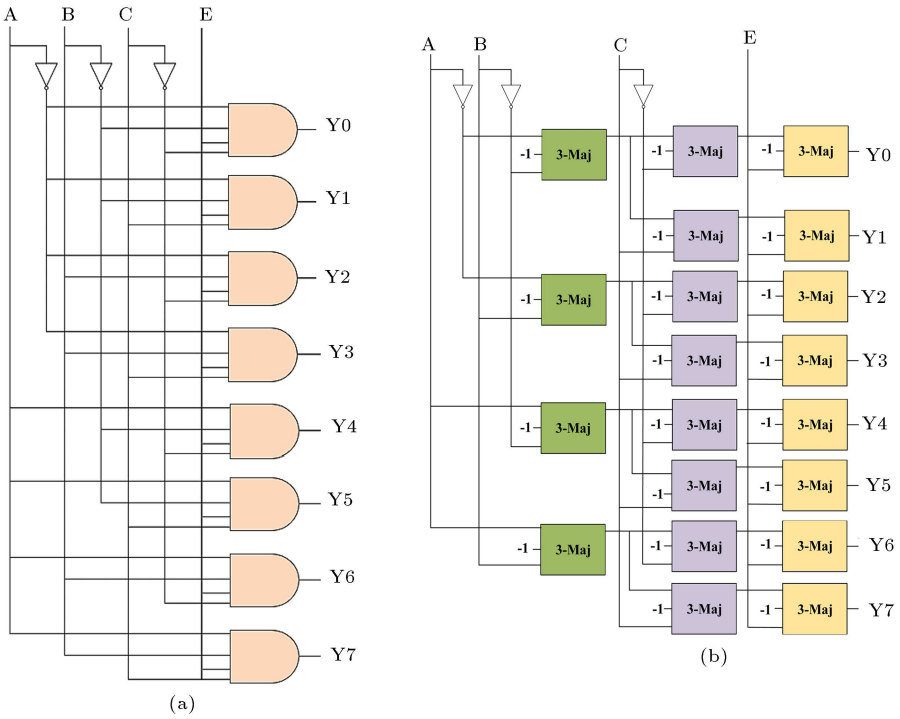

Figure 10. Decoder 3-to-8 circuit: (a) Logic diagram and (b) block diagram using MG.

Table 1. Design parameters for simulation in QCA Designer.

Parameters	Coherence vector	Bistable approximation
Cell size	18 nm × 18 nm	18 nm × 18 nm
Dot diameter	5 nm	5 nm
Radius effect	80 nm	65 nm
Number of samples	–	12,800
Convergence tolerance	–	0.0010
Relative permittivity	12.9	12.9
Clock high	9.8×10^{-22} J	9.8×10^{-22} J
Clock low	3.8×10^{-23} J	3.8×10^{-23} J
Clock amplitude factor	2.0000	2.0000
Relaxation time	4.135×10^{-14} S	–
Time step	7×10^{-16} S	–
Layer separation	11.5 nm	11.5 nm
Cell separation	2 nm	2 nm

Table 2. Comparison of the 2-to-4 decoder circuit.

Decoder circuit	CC	TA (μm^2)	CA (μm^2)	AC	Latency	QCA-CC	QC
New 2-to-4	87	0.10	0.0281	28.1%	2.5	0.625	0.25
2-to-4 [7]	193	0.25	0.062	24.8%	3	2.25	0.75
2-to-4 [8]	318	0.50	0.103	20.6%	7	24.5	3.5
2-to-4 [9]	268	0.30	0.086	28.67%	7	14.7	2.1
2-to-4 [10]	270	0.38	0.0874	230%	7	18.62	2.66

Note: CC: Cell Count; TA: Total Area; CA: Cell Area; AC: Area Coverage;
QCA-CC: QCA Circuit Cost; QC: Quantum Cost.

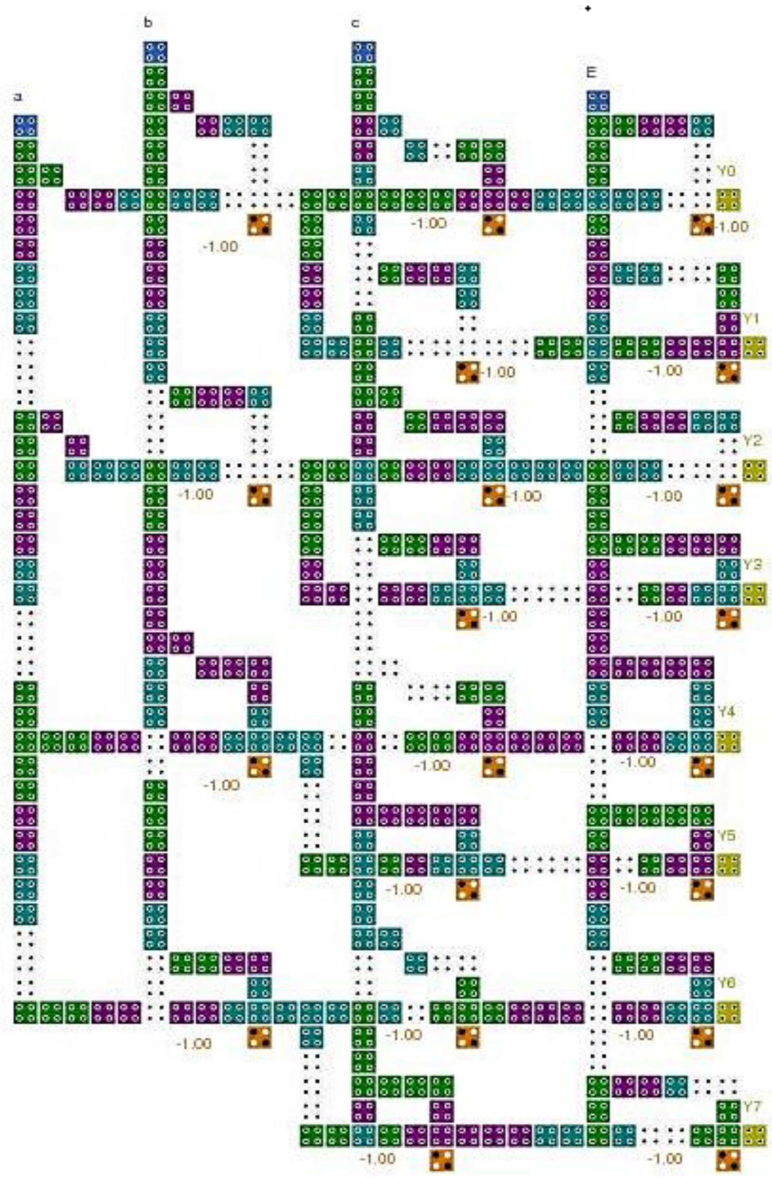

Figure 11. QCA-cell-based layout design of the 3-to-8 decoder circuit.

Table 3. Comparison of the 3-to-8 decoder circuit.

Decoder circuit	CC	TA (μm^2)	CA (μm^2)	AC	Latency	QCA-CC	QC
New 3-to-8	476	0.57	0.154	27.01	9	46.17	5.13
3-to-8 [9]	1076	2.24	725.76	32400	–	–	–

Note: CC: Cell Count; TA: Total Area; CA: Cell Area; AC: Area Coverage;
QCA-CC: QCA Circuit Cost; QC: Quantum Cost.

Table 4. Comparison of the 4-to-16 decoder.

Decoder circuit	CC	TA (μm^2)	CA (μm^2)	AC	Latency	QCA-CC	QC
New 4-to-16	1004	1.33	0.325	24.4	17	384.37	22.61
4-to-16 [15]	1874	2.94	607176	20652244.898	177	92107.26	520.38

Note: CC: Cell Count; TA: Total Area; CA: Cell Area; AC: Area Coverage; QCA-CC: QCA Circuit Cost; QC: Quantum Cost.

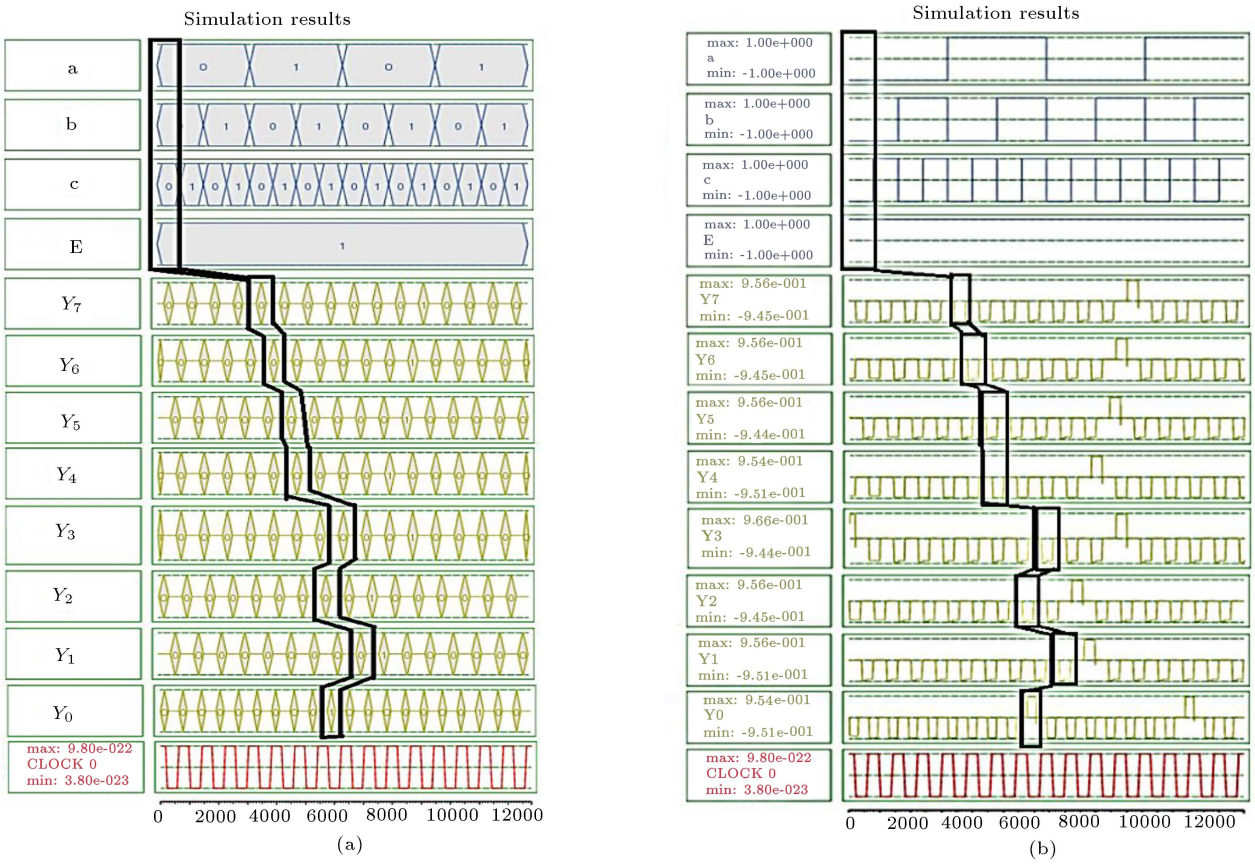

Figure 12. Design of 3-to-8 decoder circuit: (a) Bus layout and (b) output waveform.

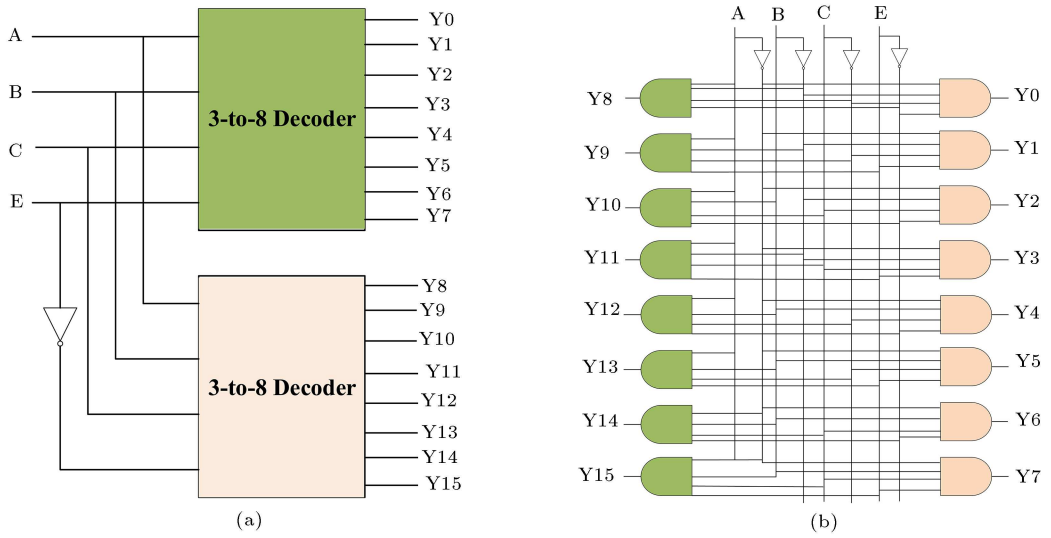

Figure 13. Design of 4-to-16 decoder: (a) Block diagram and (b) logic circuit diagram.

comparatively. When comparing the proposed design to other previous designs, we observe that it has lower values in terms of cell count, total area, cell area, area coverage, QCA circuit cost, and quantum cost, among other things. The required latency for the proposed decoder is likewise strikingly low, allowing for a more economical design while maintaining less area coverage, which ensures a minor delay in the transmission of information.

5.1.1. Cell count

The total number of QCA cells employed in the circuit layout can be defined as the total number of cells in the circuit. As a result, the cell count of a circuit

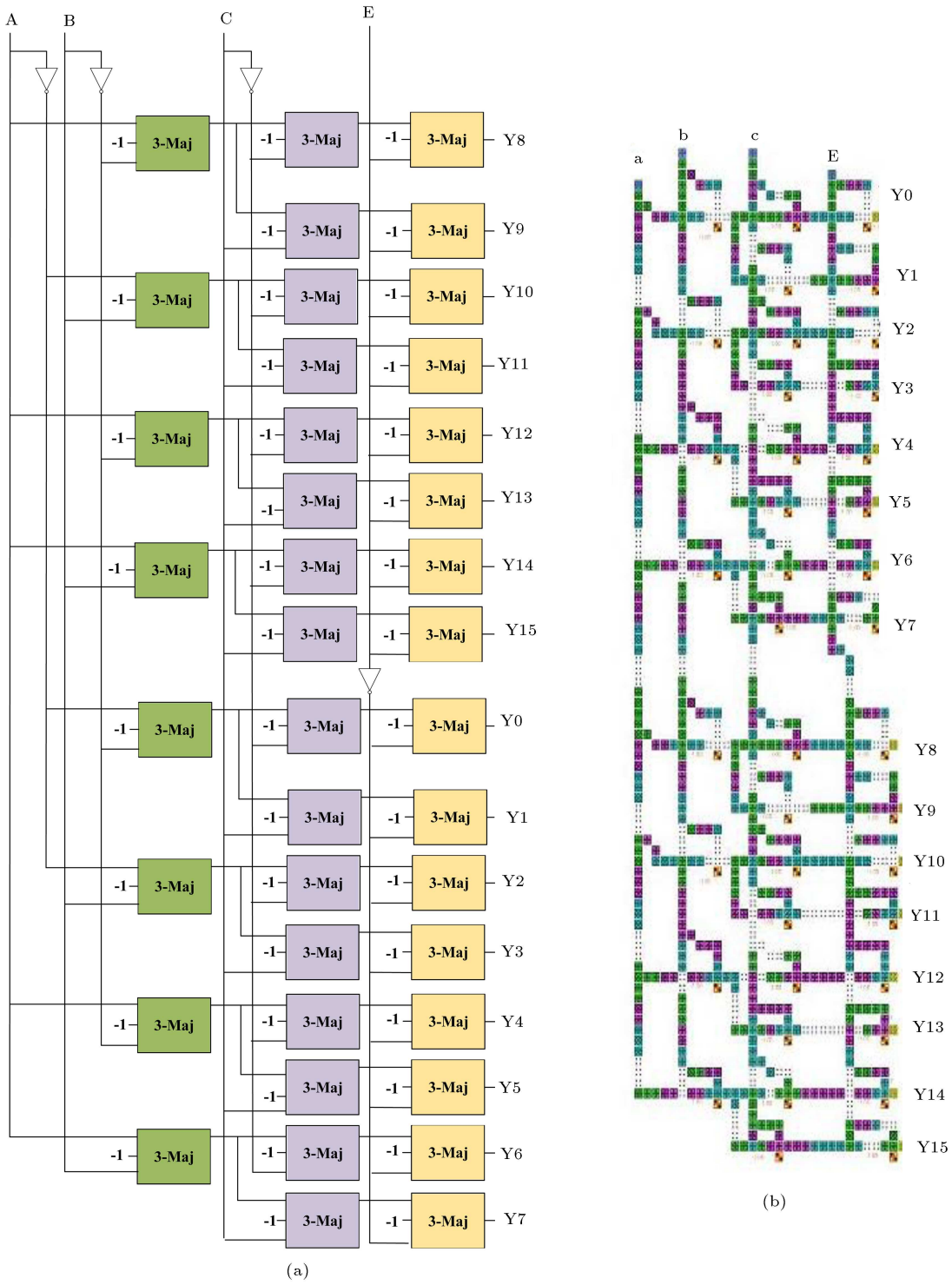

Figure 14. Decoder 4-to-16: (a) Majority gate design and (b) layout.

can be used to determine the area required for the fabrication of the circuit. The 2-to-4 decoder circuits, 3-to-8 decoder circuits, and 4-to-16 decoder circuits all require 87, 476, and 1004 cells, respectively. Tables 2 to 4 show the total number of cells in each of the circuits that have been presented. In the case of a decoder, the suggested 2-to-4 decoder circuit improves the cell count by 54.92%, 72.64%, 67.53%, and 67.78% as compared to the existing work [7–10]. Additionally, the suggested 3-to-8 decoder circuit is 55.76% more efficient than the existing 3-to-8 decoder circuit [9]. The suggested 4-to-16 decoder is 46.42% more efficient than the existing decoder circuit in terms of cell count [15].

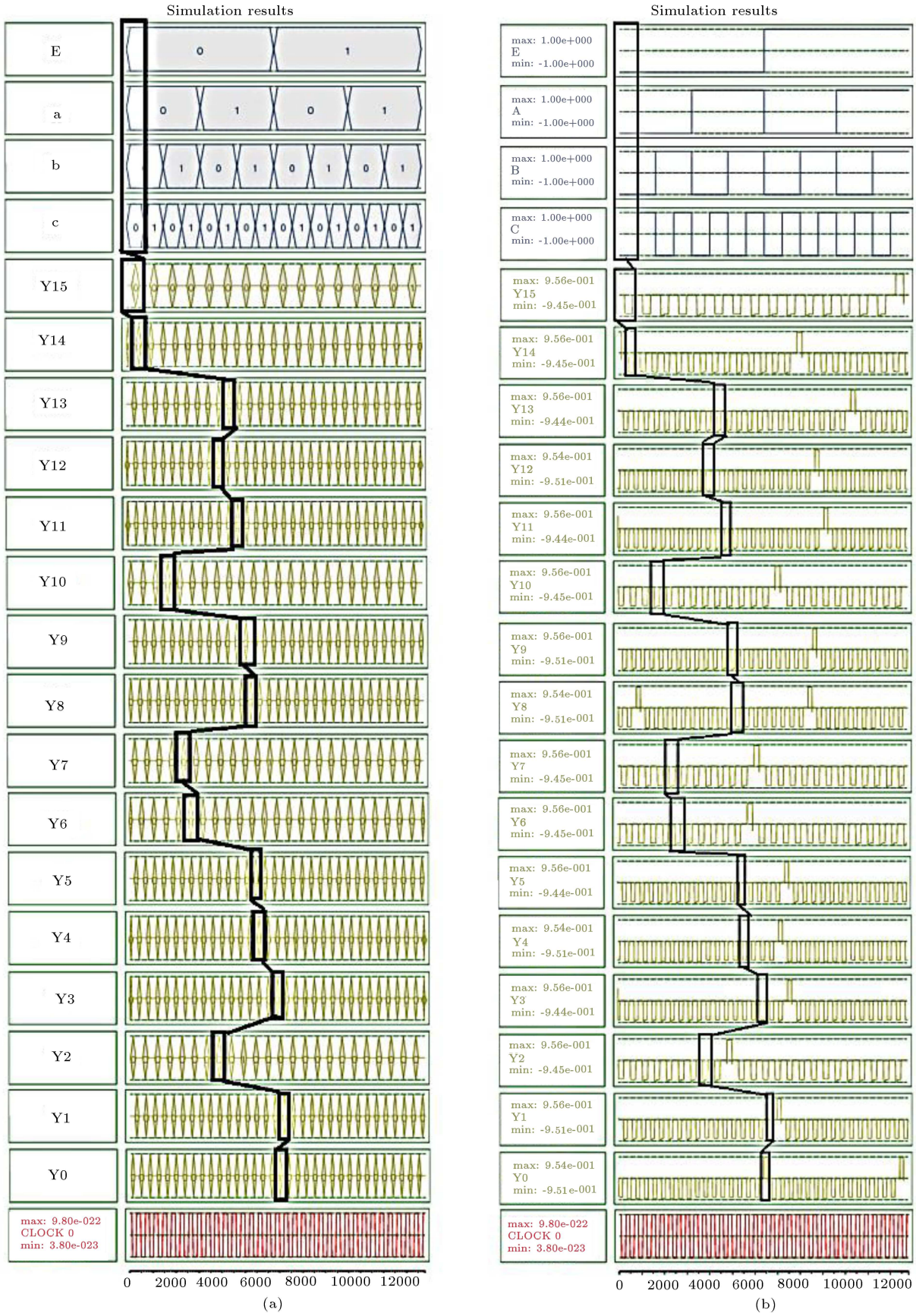

Figure 15. Simulation result of the 4-to-16 circuit: (a) Bus-layout and (b) output waveform.

5.1.2. Total area

Based on the total area allocated to building the circuit, it is possible to compute the total area used by the circuit. When calculating the integration density of a circuit, the full area needed for the circuit is taken into account. The proposed 2-to-4 decoder, 3-to-8, and 4-to-16 decoder circuits have the total areas of 0.10 μm^2, 0.57 μm^2, and 1.33 μm^2, respectively, whereas the proposed 2-to-4 decoder circuits have the total areas of 0.10 μm^2, 0.57 μm^2, and 1.33 μm^2, respectively, whereas the proposed 2-to-4 decoder circuits have 80%, 66.67%, 73.68%, and 60% more efficient than the existing 2-to-4 decoder circuit in terms of total area than the proposed 2-to-4 decoder circuit [7–10], because the total area required for the proposed 2-to-4 decoder circuit is smaller as a result of the smaller cell count. In terms of the number of total areas utilized in the circuit, the proposed 3-to-8 decoder circuit is 74.55% more efficient than the current 3-to-8 decoder circuit [9,15]. As an example, in the case of a 4-to-16 decoder circuit, the proposed model is 54.76% more efficient than the already existing 4-to-16 decoder.

5.1.3. Cell area

Cell area is the total area utilized by the cells to design the layout of a circuit. Cell area can be measured by calculating the percentage of the total area used by the cells. This is manipulated by the product of one cell area (18 nm × 18 nm) with the cell count used in the design. Our investigation shows that the cell areas consumed by the proposed 2-to-4 decoder, 3-to-8 decoder, and 4-to-16 decoder circuits using three input MG are 87 × 18 nm × 18 nm = 28188 nm^2 = 0.0281 μm^2, 476 × 18 nm × 18 nm = 154224 nm^2 = 0.154 μm^2, and 1004 × 18 nm × 18 nm = 325296 nm^2 = 0.325 μm^2, respectively. Upon analyzing the cell areas of new circuits based on the conventional literature, the cell areas of the proposed 2-to-4 decoder circuit are 4.67%, 72.71%, 67.32%, and 67.84%, being more efficient than the existing 2-to-4 decoder circuit in [7–10], respectively. Similarly, the proposed 3-to-8 decoder circuit is 99.7% more efficient than the existing 3-to-8 decoder circuit [9] in terms of the total area. Similarly, in the case of a 4-to-16 decoder circuit, the proposed decoder circuit is 1.6% more efficient than the existing decoder circuit in terms of total area [15].

5.1.4. Area coverage

Area coverage of the circuit is defined as the percentage of the total area used in the layout. The area efficiency of a circuit can be determined by the value of area coverage. Area coverage of the proposed 2-to-4 decoder, 3-to-8 decoder, and 4-to-16 decoder circuits is calculated by 28.1%, 27.01%, and 24.4%, respectively.

5.1.5. Latency

Latency is defined as the maximum clock period required to reach data from input to output. In the proposed circuits, the clock delays are 2.5, 9, and 17 clock periods for the proposed 2-to-4, 3-to-8 decoder, and 4-to-16 decoder circuits, respectively. In Tables 5, 3, and 4, the latency of the proposed circuits is analyzed with respect to those of the prior circuits, and it is demonstrated that the proposed circuits have a less delay. Similarly, the proposed a 2-to-4 decoder circuit requires 64.28%, 64.28%, 64.28%, and 16.67% smaller clock periods than the existing circuit. The proposed 3-to-8 decoder circuits are cost-efficient in terms of area coverage. The proposed 4-to-16 decoder circuit requires a 90.39% smaller clock period than the existing decoder circuit.

5.1.6. Number of inverters

The number of the inverters utilized in 2-to-4, 3-to-8, and 4-to-16 decoder circuits is calculated, with the number of inverters being 2, 3, and 4, respectively.

5.1.7. Number of the MG

In this proposed work, the number of the 3-input MG of the proposed 2-to-4, 3-to-8, and 4-to-16 decoder circuits is 4, 20, and 40 respectively, as shown in Table 5. Similarly, the number of inverters of the proposed 2-to-4, 3-to-8, and 4-to-16 decoder circuits is 2, 2, and 4, respectively as shown in Table 5.

5.2. Quantum cost and QCA circuit cost

QCA-quantum cost is defined as the product of the total area and latency of a circuit. In Tables 2, 3, and 4, the comparative results are presented. It is mandatory that the QCA-quantum circuit cost be as low as possible. In this work, QCA-quantum costs of the proposed 2-to-4, 3-to-8, and 4-to-16 decoder circuits are 0.25, 5.13, and 22.61, respectively; similarly, QCA circuit costs for the mentioned decoder circuits are 0.625, 46.17, and 387.37, respectively. From Tables 2, 3, and 4, it can be observed that the comparison of the existing decoder circuit with the proposed 2-to-4 decoder in terms of quantum cost illustrates the percentage values of 66.67%, 92.85%, 88.09%, and 90.60% with respect to the values obtained in [7–10], respectively. Similarly, the proposed 4-to-16 decoder circuits experienced a 95.65% reduction in quantum cost [15]. Similarly, the QCA circuit cost comparison for the proposed 2-to-4 decoder circuit includes the percentage values of 72.22%, 97.44%, 95.74%, and

Table 5. Analysis of numbers for majority gate and inverters of the proposed decoder circuit.

Decoder circuit in QCA	MG	Inverter
2-to-4	4	2
3-to-8	20	2
4-to-16	40	4

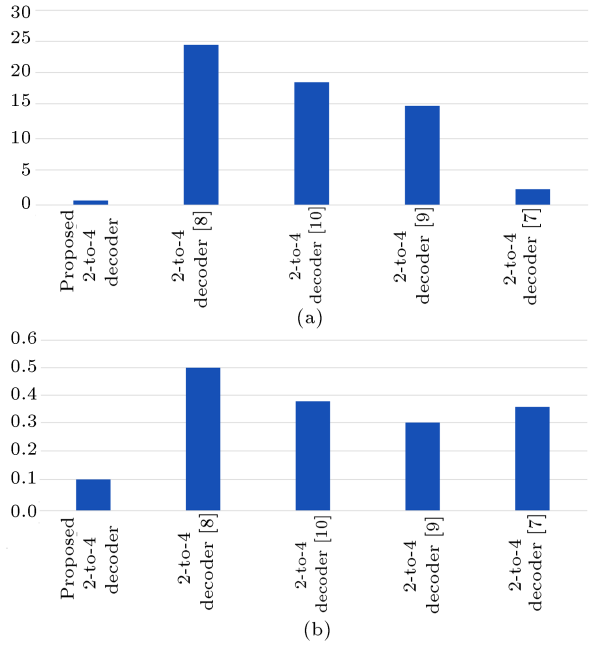

Figure 16. Comparison of a 2-to-4 decoder circuit in terms of (a) cell count and (b) total area.

96.64% with respect to the values obtained in [7–10], respectively. From Figure 16(a) and (b), it is observed that the number of cells and the total area are smaller in the proposed 2-to-4 decoder than those in [7–10], respectively.

The latency and quantum cost are lower in the proposed 2-to-4 decoder circuit than those in the existing works [7–10], respectively, as shown in Figure 17(a) and (b). The proposed 2-to-4 decoder has lower QCA circuit costs than those in [7–10], respectively, as shown in Figure 18. From Figure 18(a) and (b), it is observed that the number of cells and the total area in the proposed 3-to-8 decoder circuit are smaller than those in the 3-to-8 decoder circuit [9].

From Figure 19(a) and (b), it is observed that the cell count and total area of the proposed 4-to-16 decoder circuit are less than those of the 4-to-16 decoder [15]. From Figure 20(a) and (b), the QCA latency and QCA circuit cost are lower than those in [15]. Figure 20 shows that a 4-to-16 decoder circuit has a smaller value of quantum cost, implying its efficiency. It is observed that the proposed 4-to-16 decoder circuit has lower cell area consumption than the 4-to-16 decoder [15]. Hence, the above illustrates that the proposed 4-to-16 decoder and 2-to-4 decoder circuits are cost-efficient in terms of latency and area coverage. The proposed 3-to-8 decoder circuit is efficient in terms of area coverage.

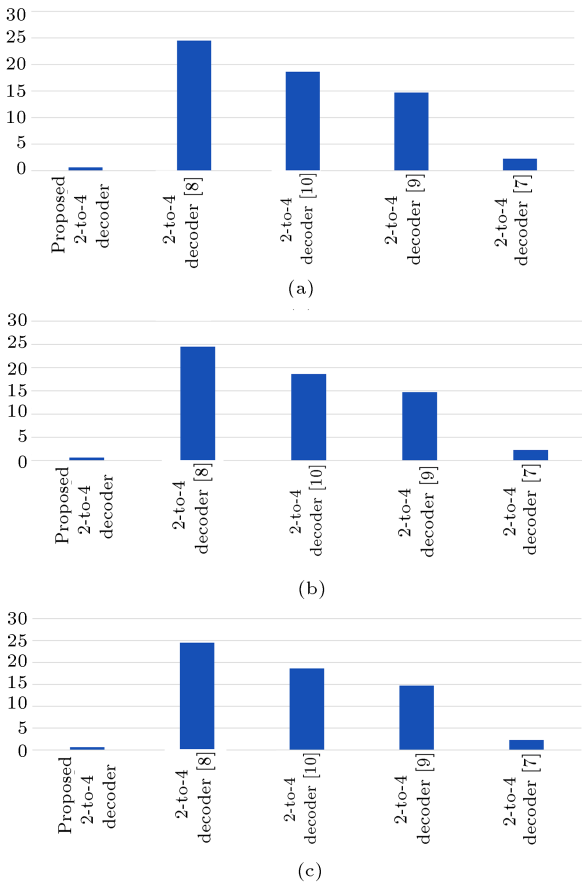

Figure 17. Comparison of a 2-to-4 decoder circuit in terms of (a) latency, (b) quantum cost, and (c) QCA quantum cost.

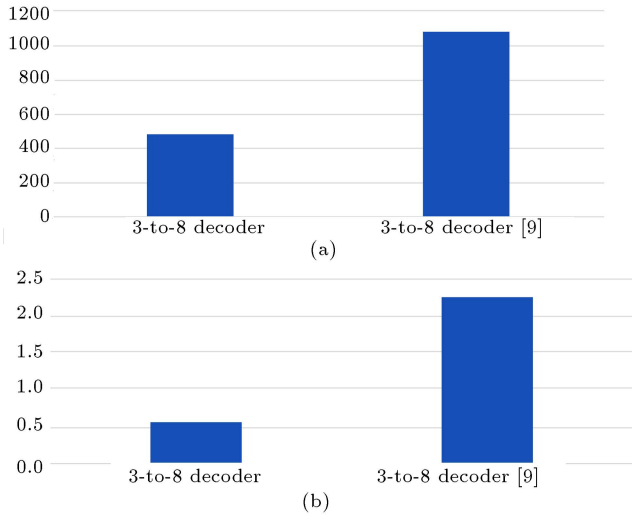

Figure 18. Comparison of the proposed 3-to-8 decoder circuit and [9] (a) cell count and (b) total area.

6. Conclusion

Quantum, dot Cellular Automata (QCA) is a cutting-edge computing innovation that offers many advantages to end users such as reduced energy usage and enhanced processing speed. Many different types of decoders including 2-to-4, 3-to-8, and 4-to-16 circuits were designed in this investigation. Every aspect of

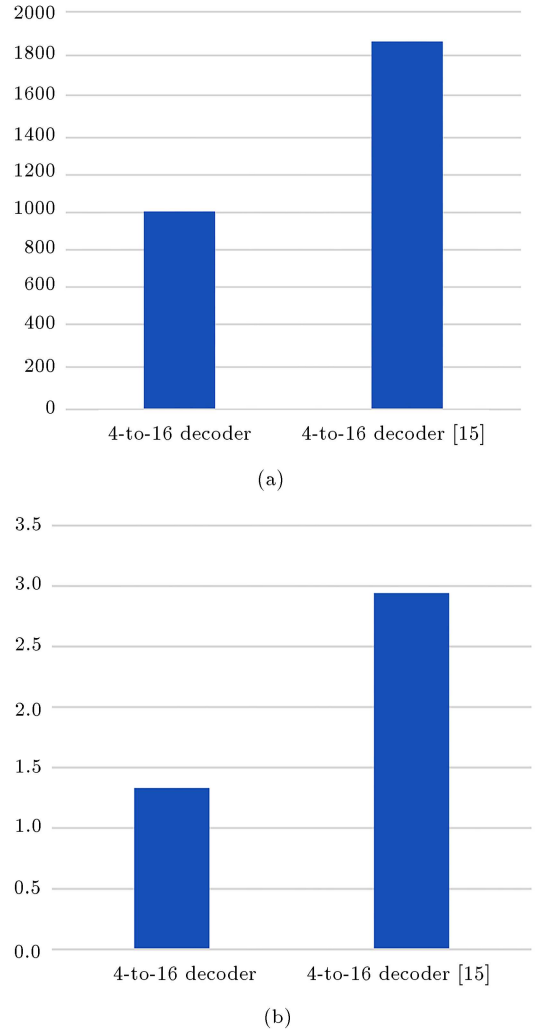

Figure 19. Comparison of the proposed 4-to-16 decoder circuit and [15] in terms of (a) cell count and (b) total area.

the QCA circuit was enhanced in the newly built circuit. This included the complexity of the circuit, the quantity of QCA cells, and the QCA circuit cost. The proposed 4-to-16 decoder needs an area of 1.33 μm^2. The smallest area of design required for these circuits was 0.10 μm^2, and the smallest amount of delay caused by these circuits was 2.5 clock periods for the 2-to-4 decoder. The proposed 4-to-16 decoder circuit had a maximum quantum cost of 22.61 and a QCA circuit cost of 384.37. The quantum cost of the new decoder circuit was reduced by 92.85%, 16.72%, and 95.85% compared to those of the current decoder circuits including 2-to-4 circuit, 3-to-8 circuit, and 4-to-16 circuit, respectively. Thus, it can be concluded that the proposed QCA circuits are more effective than their counterparts in terms of both area and speed. After contrasting the new and old designs, it was found that the newly designed circuits required significantly less area coverage, lower latency, and less QC than the previously designed circuits.

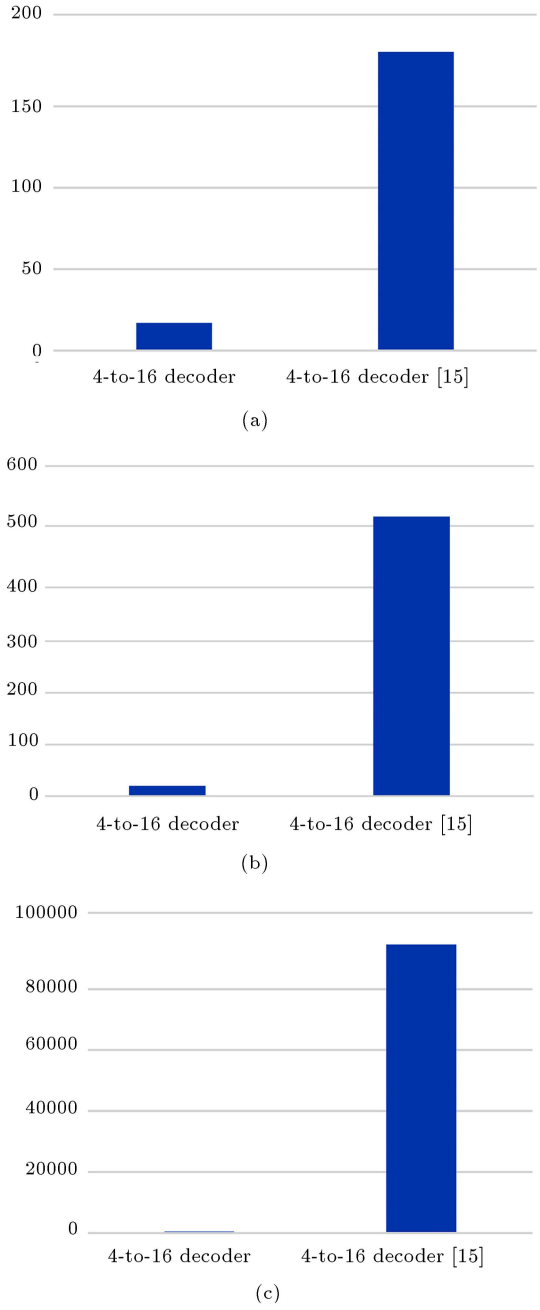

Figure 20. Comparison of the proposed 4-to-16 decoder in terms of (a) latency, (b) QCA quantum cost, and (c) QCA quantum cost.

References

1. Misra, N.K., Wairya, S., and Sen, B. "Design of conservative, reversible sequential logic for cost efficient emerging nano circuits with enhanced testability", *Ain Shams Engineering Journal*, **9**(4), pp. 2027–2037 (2018).

2. Misra, N.K., Sen, B., and Wairya, S. "Novel conservative reversible error control circuits based on molecular QCA", *Int. J. Comput. Appl. Technol.*, **56**(1), pp. 1–17 (2017).

3. Rahmani, Y., Heikalabad, S.R., and Mosleh, M. "Design of a new multiplexer structure based on a new fault-tolerant majority gate in quantum-dot cellular automata", *Optical and Quantum Electronics*, **53**(9), pp. 1–19 (2021).

4. Kaity, A. and Singh, S. "Optimized area efficient quantum dot cellular automata based reversible code converter circuits: Design and energy performance estimation", *The Journal of Supercomputing*, **77**(10), pp. 11160–11186 (2021).

5. Afrooz, S. and Navimipour, N.J. "An effective nano design of demultiplexer architecture based on coplanar quantum-dot cellular automata", *IET Circuits, Devices & Systems*, **15**(2), pp. 168–174 (2021).

6. Pathak, N., Misra, N.K., Bhoi, B.K., et al. "Optimization of parameters of adders and barrel shifter based on emerging QCA technology", *Radioelectronics and Communications Systems*, **64**(10), pp. 535–547 (2021).

7. Sherizadeh, R. and Navimipour, N.J. "Designing a 2-to-4 decoder on nanoscale based on quantum-dot cellular automata for energy dissipation improving", *Optik*, **158**, pp. 477–489 (2018).

8. Lantz, T. and Peskin, E. "A QCA implementation of a configurable logic block for an FPGA", *IEEE International Conference on Reconfigurable Computing and FPGA's (ReConFig 2006)*, pp. 1–10 (2006)

9. Kianpour, M. and Sabbaghi-Nadooshan, R. "A conventional design and simulation for CLB implementation of an FPGA quantum-dot cellular automata", *Microprocessors and Microsystems*, **38**(8), pp. 1046–1062 (2014).

10. Kianpour, M. and Sabbaghi-Nadooshan, R. "A novel modular decoder implementation in quantum-dot cellular automata (QCA)", In *2011 International Conference on Nanoscience, Technology and Societal Implications*, pp. 1–5 (2011).

11. Goswami, M., Tanwar, R., Rawat, P., et al. "Configurable memory designs in quantum-dot cellular automata", *International Journal of Information Technology*, **13**(4), pp. 1381–1393 (2021).

12. Banerjee, S., Bhattacharya, J., and Chatterjee, R., et al. "A novel design of 3 input 8 output decoder using quantum dot cellular automata", *IEEE 7th Annual Information Technology, Electronics and Mobile Communication Conference (IEMCON)*, pp. 1–6 (2016)

13. Vieira, L.G.L., Vieira, L.F.M., Vieira, M.A.M., et al. "Geometric greedy router in quantum-dot cellular automata", *AEU-International Journal of Electronics and Communications*, **128**, 153498 (2021).

14. Navidi, A., Sabbaghi-Nadooshan, R., and Dousti, M. "TQCAsim: an accurate design and essential simulation tool for ternary logic quantum-dot cellular automata", *Scientia Iranica*, **29**(6), pp. 3249–3256 (2021).

15. Kassa, S., Gupta, P., Kumar, M., et al. "Rotated majority gate-based 2n-bit full adder design in quantum-dot cellular automata nanotechnology", *Circuit World*, **48**(1), pp. 48–63 (2021)

16. Yaqoob, S., Ahmed, S., Naz, S.F., et al. "Design of efficient N-bit shift register using optimized D flip flop in quantum dot cellular automata technology", *IET Quantum Communication*, **2**(2), pp. 32–41 (2021).

17. Misra, N.K., Sen, B., Wairya, S., et al. "Testable novel parity-preserving reversible gate and low-cost quantum decoder design in 1D molecular-QCA", *Journal of Circuits, Systems and Computers*, **26**(09), 1750145 (2017).

18. Pal, J., Pramanik, A.K., Sharma, J.S., et al. "An efficient, scalable, regular clocking scheme based on quantum dot cellular automata", *Analog Integrated Circuits and Signal Processing*, **107**(3), pp. 659–670 (2021).

Biographies

Bandan Kumar Bhoi received his PhD from Veer Surendra Sai University of Technology, India; an MTech degree from IIIT Hyderabad, India; and a BTech in ECE from Biju Patnaik University of Technology, India. He worked as a design engineer in the VLSI industry from 2010 to 2011. He is working as an Assistant Professor in ECE at Veer Surendra Sai University of Technology, India. His research areas include reversible computation, QCA, and reconfigurable computing architectures.

Neeraj Kumar Misra is an Associate Professor at Vellore Institute of Technology (VIT)-AP University Amaravati, India. He has more than 11 year experience in teaching and research. He did BTech from Integral University, Lucknow, and Post-Graduation, first class with Distinction. He was awarded full-time PhD under the Teaching Education Quality Improvement Program (TEQIP-II), Government of India and World Bank Fellowship from Dr. A.P.J. Abdul Kalam Technical University. He has published 7 Indian National Patents and 3 international patent Grants. He has published more than 50 research publications including SCI, SCOPUS, UGC, and IET Inspec, as well as reputed conferences, etc. Under his supervision, 14 MTech (completed) and 2 PhD (ongoing) students completed their programs. He has received the best paper award in International Conference on Advancement in Signal Processing & Integrated Networks (SPIN) at Amity University, Noida in 2011 and Best paper award in Springer sponsored International Conference on Micro/Nanoelectronics Devices, Circuits, and Systems at

NIT Silchar, Assam, India. He has a member of ISTE, ACM, IAENG, IEEE, IRED, World Research Council, IETE, etc. His research interests include quantum computing, reversible computing, fault-tolerant circuit architecture, QCA technology, nano-magnetic logic, DFT, and low power and reliability-aware VLSI circuits.

Prity Bharti received MTECH degree in VLSI and Signal Processing from Veer Surendra Sai University of Technology India in the year 2018 and BTECH in Electronics and Telecommunication Engineering from Biju Patnaik University of Technology, Odisha, India in 2016 and an Intermediate in Science from Jharkhand Academic Council, Ranchi India in 2011. She has strong academic records, overall. She is a passionate, self-motivated, responsible, reliable, and very hard-working person who is proficient in working very well both in a team environment and individual initiative. Her research area includes Quantum-dot Cellular Automata (QCA), device modeling, and DSP applications.