Scientia Iranica D (2023) 30(4), 1314–1329

Sharif University of Technology
Scientia Iranica
Transactions D: Computer Science & Engineering and Electrical Engineering
http://scientiairanica.sharif.edu

A 24 GHz circularly polarized on-chip antenna for short-range communication application

S. Mandal[a], H. Singh[a], S.K. Mandal[a,*], A.K. Mal[a], R. Mahapatra[a], and P.R.T. Naidu[b]

a. *Department of Electronics & Communication Engineering, NIT Durgapur, Durgapur-713209, West Bengal, India.*
b. *Department of Space, Semi-Conductor Laboratory, Punjab, Pin-160071, India.*

Received 1 January 2021; received in revised form 5 August 2021; accepted 14 February 2022

KEYWORDS
Miniaturized antenna;
Circular polarization;
On-chip antenna;
CMOS;
System-on-chip.

Abstract. This article presents a design method for a miniaturized, Circularly Polarized (CP), concentric ring-shaped monopole on-chip antenna for 24 GHz short-range application. The proposed antenna covers a 22–29 GHz automotive radar spectrum with a resonance at 24 GHz. Taking a simple circular ring-shaped patch as the reference antenna, this study introduces a small gap in the closed-loop structure that helps provide the required travelling wave current distribution to realize the CP property. Then, a smaller circular ring is incorporated inside the reference antenna to improve the antenna performance in terms of the CP characteristics. Finally, the proposed antenna is tuned to obtain the CP characteristics in the desired band ranging from 23.2 GHz to 27 GHz with 3–dB with Axial Ratio (AR) bandwidth of 3.8 GHz. It offers a maximum gain of −4.5 dBi and wide angular range coverage (HPBW $> 75^\circ$ in both E and H-plane). The standard CMOS process with only one level of mask (metal patterning) is used to better understand the functions of the designed antenna. Compact size (3.8 mm × 4 mm × 0.678 mm), simple design layout, and high performance make the antenna a suitable candidate for System-on-Chip (SoC) application.

1. Introduction

The ever-growing demand for a miniaturized, low-cost complete Radio Frequency (RF) system has encouraged researchers towards a proper design and implementation of on-chip antennas. The main feature that has brought this emerging domain to the attention of the research community is the feasibility of antenna integration with other necessary analog and digital modules on the same silicon wafer to make an application-specific, truly-effective, compact System-on-Chip (SoC) at a very reasonable price. In addition, on-chip antennas eliminate the need for bond wires and impedance matching networks. However, the main drawback here is the electrical properties of silicon wafer, i.e., low resistivity and high relative permittivity, which are ill-suited for designing an efficient antenna on it. These two factors result in absorption and dissipation of power instead of radiation. As a result, both gain and efficiency of the on-chip antenna become very low. Although it has been investigated that the

*. *Corresponding author.*
E-mail addresses: sanjuktamandal2@gmail.com (S. Mandal); harshvardhan8289@gmail.com (H. Singh); sujit.mandal@ece.nitdgp.ac.in (S.K. Mandal); akmal@ece.nitdgp.ac.in (A.K. Mal); rajat.mahapatra@ece.nitdgp.ac.in (R. Mahapatra); teja@scl.gov.in (P.R.T. Naidu)

doi: 10.24200/sci.2022.57325.5202

dielectric loss in high-resistive Si is less than that in low-resistive Si [1,2], such high-resistive Si is not suitable for the bulk CMOS process. Consequently, different methods such as inserting an artificial magnetic conductor layer beneath the antenna [3] and incorporating a convex-shaped silicon lens at the backside of the substrate [4] have been reported to improve the antenna efficiency.

Another important issue that should be taken into consideration while designing an on-chip antenna is to avoid or minimize the effect of interference from other electronic circuit components integrated on the same silicon wafer. In a standard CMOS process layout, there are 6–7 metal layers embedded in the insulating layers. The antenna is generally placed on the top metal layer while different circuit components are integrated on the bottom layer. One of the methods to prevent the coupling of EM signal with the substrate as well as other circuit components integrated within the substrate is to use one intermediate metal layer as the ground for the antenna, as proposed in [5]. Such an intermediate ground layer isolates the antenna from the lossy Si substrate and thus, prevents the interference of the RF signal with other circuits designed on the substrate.

The on-chip antenna is mainly used for short-range applications like intra- and inter-chip communication [6,7], biomedical application [8,9], RF energy harvesting [10], and short-range automotive radar application [11,12], to name a few. Designing on-chip automotive radar sensors is a trendy topic because in the present scenario, a traveler's primary concern while taking a step out is whether or not they will safely reach their destination. This fearful thought comes to mind automatically as daily newspapers are currently flooded with coverage of severe road crashes happening in every part of the world. Vulnerable Road Users (VRUs) are the primary victims of road crashes. The VRUs are referred to as those who have no protective metal shielding, such as pedestrians, pedal cyclists, and motor cyclists [13]. To reduce the number of road crashes and their severity, smart vehicular systems equipped with advanced radar technology are now used and they help drivers in a reliable environment sensing. European Commission (EC) issued a standard transport policy in September 2001, aiming to diminish road fatality to a great extent [14]. Radar technology is currently becoming a crucial part of the European e-safety program owing to its most attractive feature, i.e., weather independent characteristic. For such an application, European Conference of Postal and Telecommunications Administration (CEPT) released 5 GHz bandwidth starting from 21.65 to 26.65 GHz in 2005. In 2002, US-based organization Federal Communication Commission (FCC) allocated 22–29 GHz band to short-range automotive radar applications [15].

To explore the above-mentioned band, several works have been reported in the recent past from both industry and academia. Experimental validation of a 24 GHz Frequency-Modulated Continuous Wave (FMCW) radar system module comprising a transmitter and five-element array antenna along with a digital signal processing unit was reported in [16] to measure the accurate distance. In [17], a 24 GHz radar system module of 3 cm $\times$ 3 cm in size containing a Circularly Polarized (CP), dual-orthogonal fed microstrip patch antenna for automotive applications was presented. Array antennas like Microstrip Franklin Array Antenna (MFAA) and grid array antenna designed on ROGERS Corp. substrate for short-range radar applications were discussed in [18] and [19], respectively. All of these antennas are termed as off-chip antennas as they are designed on Printed Circuit Board (PCB). With the advancement of on-chip technology, radar transceiver circuits are now being realized on a silicon wafer using different process technologies like Si-Ge [20,21], Si-CMOS [22,23], Si-Ge BiCMOS [24], etc.

Most of the antennas designed for radar system are Linearly Polarized (LP) off-chip antennas [25–27]. However, a 24 GHz LP on-chip antenna was reported in [28]. In [29], a 24/60 GHz dual-band on-chip antenna was introduced using CMOS technology. The LP antennas possess inherent critical shortcomings. For example, if the electromagnetic signal reflected from the target is rotated at angle θ upon propagation, the power received by the LP antenna at the receiving end is reduced by a factor of cos θ, which reduces the overall efficiency of the radar system. This problem can be sorted out by replacing the LP antenna with a CP antenna since the CP antennas can receive signal effectively even when the signal is rotated.

In this context, this paper presents a highly miniaturized, CP on-chip antenna with wide angular coverage and significant gain for precise object scanning in 24 GHz automotive short-range radar application. The proposed antenna is designed with the standard CMOS process layout in mind, so that it can be easily integrated with other necessary RF modules, with the goal of creating a compact automotive SoC radar in the future. It offers the advantage of less space consumption and lower cost than those of the conventional off-chip radar system.

The rest of the paper is organized as follows. Section 2 addresses detailed antenna design steps, followed by the results and analysis given in Section 3. Section 4 discusses post fabrication work. Finally, Section 5 presents the concluding remarks.

2. Proposed CP on-chip antenna

2.1. Design layout and fabrication process

A cross-sectional view of the fabrication process layout

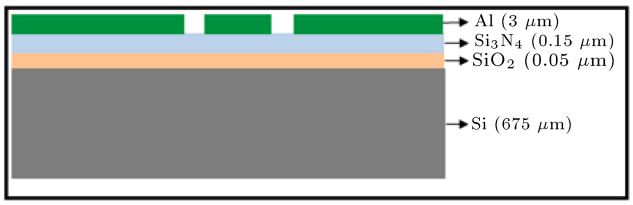

Figure 1. Fabrication process layout.

is illustrated in Figure 1. In this study, a Floating Zone (FZ) was first processed, and 675 μm thick excessively pure 6″ silicon wafer ($\tan\delta = 0.01$ and $\varepsilon_r = 11.8$) with an orientation of <100> was chosen as the substrate for designing the antenna. Initially, on the surface of the wafer, two thin insulating layers of SiO_2 ($\varepsilon_r = 4$) with a thickness of 0.05 μm and Si_3N_4 ($\varepsilon_r = 7.5$) with a thickness of 0.15 μm were grown through thermal oxidation and Low-Pressure Chemical Vapor Deposition (LPCVD) processes, respectively. The stack of silicon-di-oxide and silicon nitride was chosen for stress balancing. The key factor in adopting an insulating layer before metallization is that metal can diffuse into the semiconductor material and make a metal-semiconductor junction (Schottky Barrier). As a result, adhesion of a metal to the insulator is a completely better option than adhesion to the semiconductor, and the insulating layer contributes to IC compatibility. Finally, at the top, Aluminium (Al) layer of 3 μm in thickness was used to realize the radiating structure. It was deposited using DC magnetron sputtering, followed by a metal masking process through 365 nm UV lithography. Finally, metal was removed using the chlorine-based RIE etching process and photoresists were stripped out through oxygen plasma cleaning.

2.2. Reference antenna design

To better understand the function of the CP on-chip antenna, first, a Coplanar Waveguide (CPW) fed, circular ring-shaped radiating patch was designed, as shown in Figure 2. The feed line with the $G_{sg}/W_f/G_{sg}$ configuration of 0.11/0.18/0.11 (mm) was also used here to achieve 50 Ω characteristics impedance. Since the available RF connectors cannot be fitted with this type of tiny-sized on-chip antenna, GSG (Ground-Signal-Ground) probe is generally used for characterizing the fabricated antenna prototype. The GSG probe provides a precise planar contact for both ground and signal lines of the CPW feed, and the proper pitch size (spacing between signal and ground) of the probe ensures excellent performance. CPW feeding in designing an on-chip antenna is highly recommended for the following reasons:

(a) It simplifies fabrication step and reduces the manufacturing cost and time as well since only one mask is required to fabricate this CPW feed;

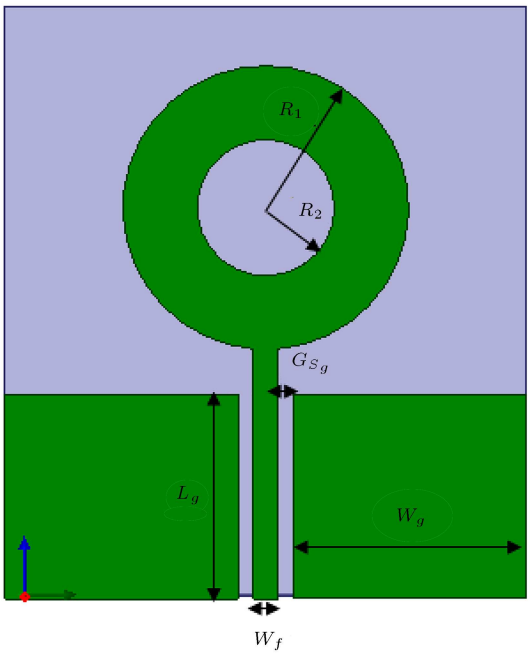

Figure 2. Geometry of the reference monopole on-chip antenna (where, $L_g = 1.375$ mm, $W_g = 1.7$ mm, $W_f = 0.18$ mm, $G_{sg} = 0.11$ mm, $R_1 = 1.04$ mm, and $R_2 = 0.5$ mm).

(b) It eliminates the need for via holes;

(c) It allows the computer-controlled on-wafer measurement technique in a more precise manner up to several tens of GHz;

(d) It has the potential to offer wideband characteristics due to its low dispersion;

(e) It reduces radiation loss; and

(f) It offers easy integration of other surface mounting devices in a very compact way.

Microstrip line feed is mostly avoided in such cases because the standard CMOS process does not support enough separation between the ground plane and radiating element. As a result, the performance of the antenna will be degraded to a great extent due to the formation of image current [30]. Further, other modules of a SoC may be adversely affected by the interference caused by the metal layer acting as a ground plane for microstrip feed.

The variations in the return loss (S_{11}) characteristic for different values of circular patch radius (R_1) are presented in Figure 3. According to the observations, the parameter R_1 is responsible for the variation of both upper and lower cutoff frequencies. With an increase in the R_1 value, the lower cut-off frequency gradually shifts to the left side while, the upper cut-off frequency shifts to the right side, resulting in bandwidth enhancement. The optimum value of $R_1 = 1.04$ mm provides the best S_{11} characteristics with a resonating frequency of 24 GHz.

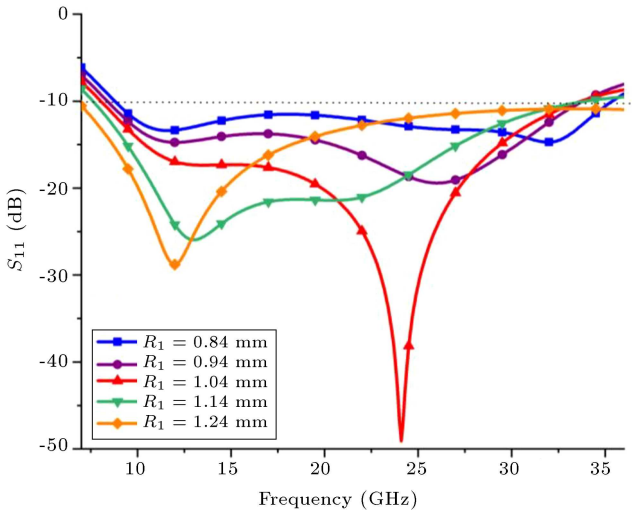

Figure 3. Return loss characteristics for different values of R_1 with a fixed optimum value of $R_2 = 0.5$ mm.

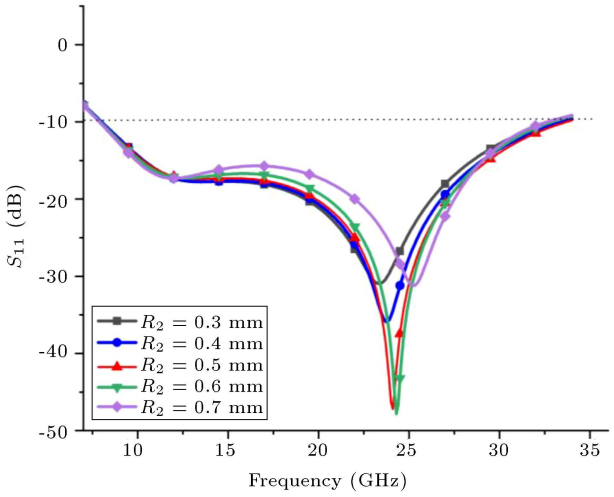

Figure 4. Return loss characteristics for different values of R_2 with a fixed optimum value of $R_1 = 1.04$ mm.

Figure 4 shows the effect of altering the values of the circular slot radius (R_2) on the S_{11} characteristics. In case R_2 changes from 0.35 mm to 0.95 mm, even though the upper and lower cut-off frequencies remain almost the same, gradual improvement in the curve of the characteristics is clearly noticed. Based on these two parametric studies, it can be deduced that the resonating frequency of the antenna can be tuned through proper selection of R_1 and R_2. In this design, the resonating frequency of 24 GHz is obtained with the optimum values of R_1 and R_2 as 1.04 mm 0.5 mm, respectively. This reference antenna covers the ultra-wideband automotive radar spectrum and exhibits the fractional bandwidth of 107.25%.

2.3. Realization of the circular polarization

Polarization of the EM wave indicates the magnitude and time-varying orientation of the electric field vector. Depending on the current distribution in the antenna structure, the radiated field becomes either linear or circular. A loop antenna with standing-wave current distribution usually generates a LP wave [31,32]. On the contrary, a uniform travelling wave circular current distribution is required to generate a CP wave [33]. Different techniques used for creating a travelling wave current distribution in a loop-structured antenna are listed below:

1. Exciting the antenna with two different sources of equal magnitude and phase differed by 90° [34];
2. Using the antenna loaded with resistors [35]; and
3. Using the antenna loaded with a reactance [36].

Among these three techniques, the last one is employed in this design because of its easy implementation. In order to incorporate such reactive load, a small gap (G) as a perturbation element is introduced in the designed reference antenna, as shown in Figure 5(a).

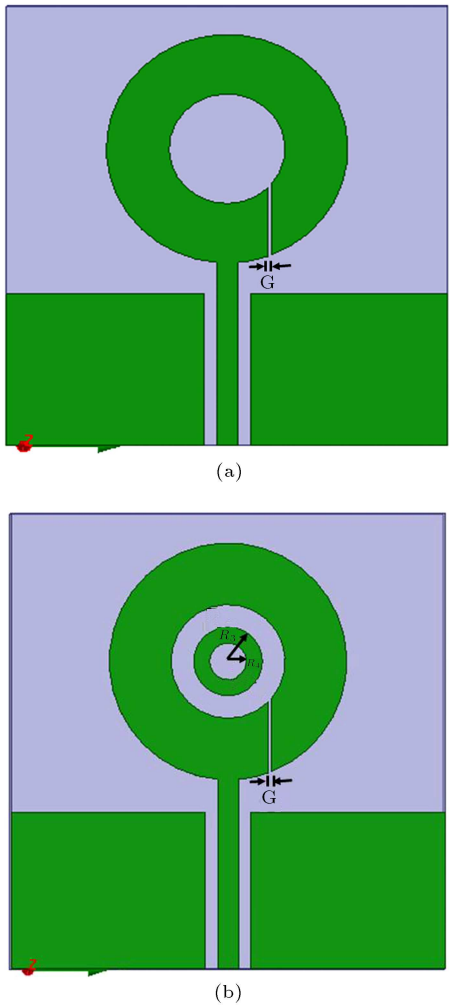

Figure 5. Design steps of the CP antenna (a) Inclusion of the gap ($G = 30$ μm) and (b) incorporation of the inner loop ($R_3 = 0.3$ mm and $R_4 = 0.16$ mm); all other parameters are same as reference antenna.

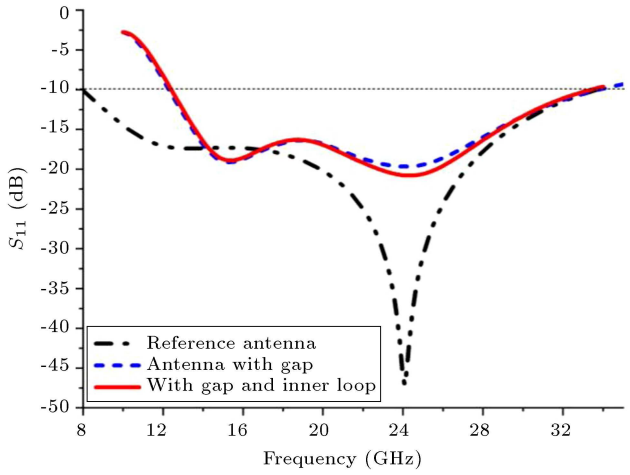

Figure 6. S_{11} comparison of the reference antenna, antenna with gap, with gap and inner loop.

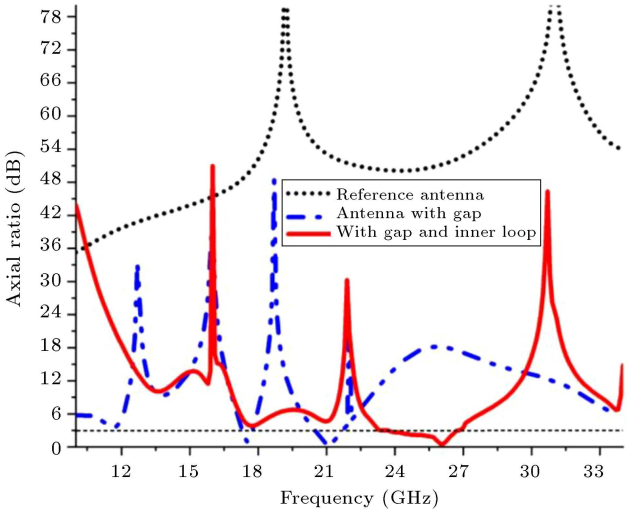

Figure 7. Axial ratio comparison of the reference antenna, antenna with gap, and antenna with gap and inner loop.

The air gap provides capacitive loading and according to the observations, the resulting antenna structure is a suitable candidate for generating the CP EM wave. Finally, as shown in Figure 5(b), an extra inner loop, is added to the proposed antenna to obtain the CP mode within the desired band of operation.

The S_{11} and Axial Ratio (AR) characteristics of the antenna in the respective design steps are presented in Figures 6 and 7, respectively. Compared to the reference antenna (Figure 6), incorporation of the air gap leads to impedance mismatching, which in turn causes degradation of the S_{11} characteristics. The lower cut-off frequency also shifts to the right due to the reduced current conduction path. As observed in Figure 7, such incorporation has a great impact on the AR characteristics. It helps a LP reference antenna at an axial ratio of ≥ 20 to become CP with the axial ratio of ≤ 3 at two different frequency bands (17.3 to 17.74 GHz and 20.5 to 21.7 GHz). The voltage drop across the gap capacitor can be represented by an equivalent load voltage V_L [37], which is equal to $I_F/j2\pi fC_G$, where I_F is feed current, f the operating frequency, and C_G the value of the gap capacitor. In a certain frequency range, this voltage will be equal to the feed voltage (V_F). Given that it is capacitive loading, there will be a 90° phase shift between them. Hence, the condition needed for getting a CP antenna is provided.

The inner loop contributes significantly to the AR bandwidth improvement for the desired band of operation. After its inclusion, the characteristic S_{11} remains the same as in the previous step (Figure 6), while the AR bandwidth is considerably improved and right-shifted to the intended band (23.2 GHz to 27 GHz) (Figure 7). The right-shifted AR bandwidth is obtained due to the parasitic capacitance formation between the outer and inner loops. This capacitance appears in series with a gap capacitance. Since the gap width is smaller than the separation between the two concentric loops, the capacitance between the two loops is less than the gap capacitance. As a result, the lower value of the resultant series capacitance is obtained. This lower value of capacitance will increase the capacitive reactance, which leads to the shifting of the minimum AR point towards right so as to better realize the same V_L and V_F. With the inclusion of the inner loop, a part of the feed power is induced in the inner loop from the outer loop. Some of this induced field is penetrated into the substrate and the remaining part is spread in the surrounding air medium. Therefore, the increased substrate loss leads to a decrease in the quality factor (Q) of the antenna. The AR bandwidth of a CP antenna is related to the Q factor, as shown in [38]:

$$BW_{CP}^{AR} = \frac{AR_{\max} - 1}{\sqrt{AR_{\max}.Q}}, \tag{1}$$

where $AR_{\max}$ is the maximum allowable AR that determines the bandwidth:

$$AR_{\max} = e^{AR_{\max}^{dB}[\ln(10)/20]} \approx 1 + AR_{\max}^{dB}[\ln(10)/20], \tag{2}$$

where $AR_{\max}^{dB}$ is the maximum allowable AR in dB. By substituting the value of $AR_{\max}$ in Eq. (1), we can write BW_{CP}^{AR} as follows:

$$BW_{CP}^{AR} = \frac{AR_{\max}^{dB}[\ln(10)/20]}{\sqrt{1 + AR_{\max}^{dB}[\ln(10)/20].Q}}. \tag{3}$$

Here, followed by performing the binomial expansion in the denominator and neglecting the smaller values, we can simplify Eq. (3) as follows:

$$BW_{CP}^{AR} \approx \frac{AR_{\max}^{dB}[\ln(10)/20]}{Q} \approx \frac{AR_{\max}^{dB}.(0.115)}{Q} \approx \frac{0.348}{Q}. \tag{4}$$

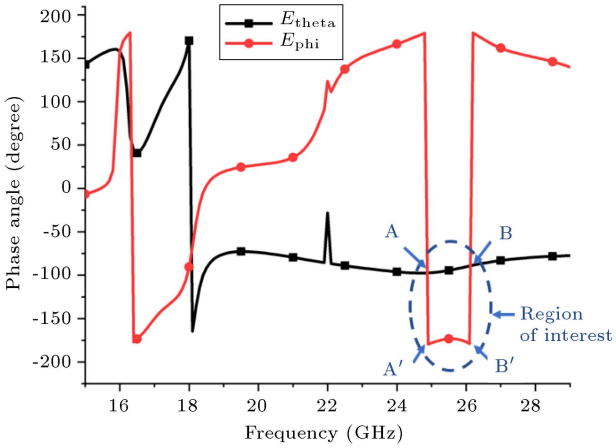

Figure 8. Phase characteristics of the two orthogonal field components of the proposed antenna depicted in Figure 5(b).

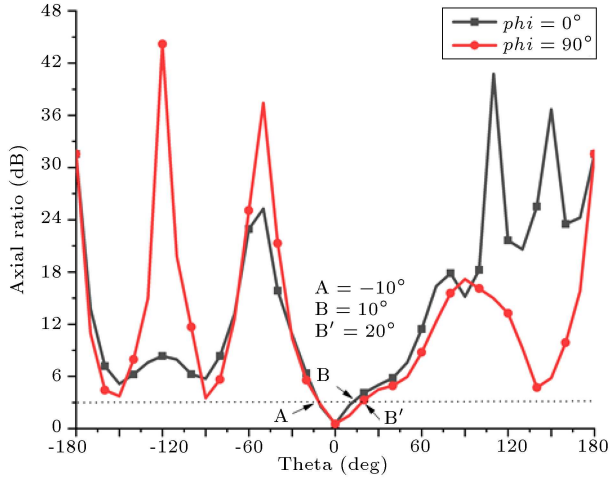

Figure 9. Axial ratio characteristics for different values of theta on the fixed phi plane.

Thus, the decreased Q factor due to the inner loop results in an improvement in the AR bandwidth of the CP antenna.

Figure 8 shows the phase characteristics of two orthogonal field components E_{theta} and E_{phi} of the proposed antenna. In this figure, the desired range under consideration is encircled with an ellipse and the extreme boundary of the region is marked with four points of A, B, A', and B'. The phase angles of the component E_{theta} at two boundary points (points A and B) are 96.4° and 88.5°, respectively. In addition, the phase angles corresponding to the component Ephi at the boundary points (point A' and B') are obtained as 185.2° and 178.7°, respectively. Therefore, in the desired frequency range, the phase difference between the two orthogonal components is observed as approximately 90°, which is another mandatory condition for obtaining circular polarization property.

Figure 9 shows the plot of the AR with respect to θ for two principal phi planes, i.e., $phi = 0°$ (E plane) and $phi = 90°$ (H plane). On the $phi = 0°$ plane, CP is obtained within an angular range of $-10°$ to 10° and on the $phi = 90°$ plane, it is achieved within the angular range of $-10°$ to 20°. This shows that CP polarization is in the boresight direction of the antenna.

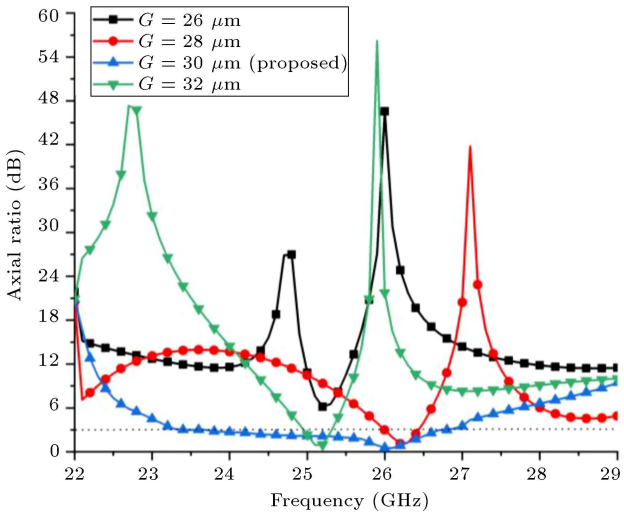

Figure 10. Effect of gap dimension (G) on axial ratio characteristics.

2.4. Parametric analysis

The outer radius (R_3), inner radius (R_4) of the inner loop, and gap width (G) in the outer loop are parametrically optimized to obtain the desired 3-dB AR characteristics.

2.4.1. Effect of G

The effect of the gap dimension (G) on the 3-dB AR bandwidth of the proposed antenna is shown in Figure 10. It is observed that the antenna is characterized by a linear polarization property for all the values of G except $G = 30$ μm. Of note, the magnitude of the gap voltage V_L depends upon the equivalent reactive impedance of the gap, which in turn depends upon the value of C_G and f. The C_G value further depends on the gap width G. Therefore, both gap width and operating frequency control $|V_L|$. At a particular value of G (here it is 30 μm), $|V_L|$ is equal to $|V_F|$ in certain frequency ranges, hence realization of the CP antenna.

2.4.2. Effect of R_3 and R_4

The effects of the variations in the outer radius (R_3) and inner radius (R_4) of the inner loop on the AR characteristics are shown in Figures 11 and 12, respectively. An increase in the value of R_3 reduces the separation between the inner and outer loops; thus, the parasitic capacitance increases. Therefore, at a particular value of R_3, the antenna becomes CP. On the contrary, an increase in the value of R_4 at a fixed R_3 value reduces the inner loop width, and its effect is reflected in the antenna polarization characteristics (Figure 12).

With the optimum values of $G = 30$ μm, $R_3 =$

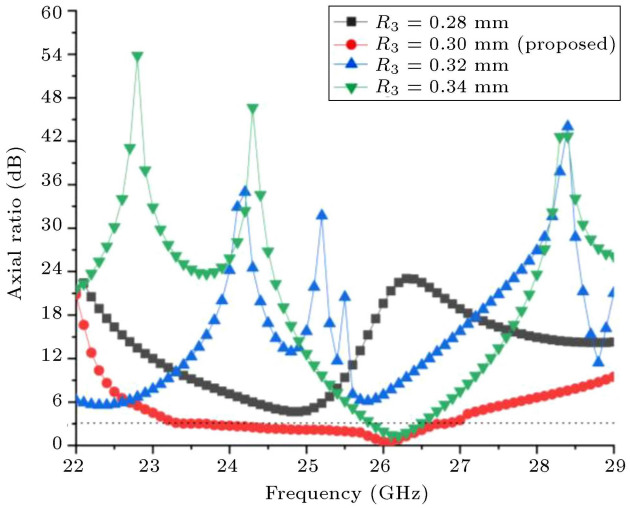

Figure 11. Effect of R_3 on axial ratio characteristics.

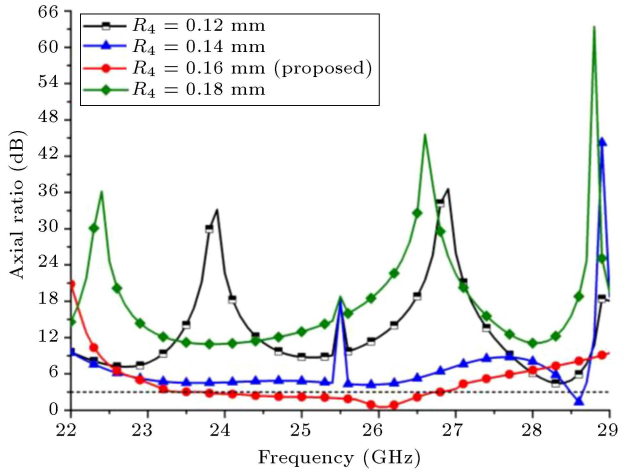

Figure 12. Effect of R_4 on axial ratio characteristics.

0.30 mm, and $R_4 = 0.16$ mm, the proposed antenna achieves the axial ratio of ≤ 3 dB in the frequency range of 23.2 GHz to 27 GHz (14.6%). In this study, the FEM-based EM simulator HFSS v17 is used to design the 3D antenna structure.

3. Results and analysis

3.1. Simulated gain, efficiency, radiation pattern, and surface current distribution

The simulated gain and efficiency characteristics of the proposed antenna are depicted in Figure 13. The gain of the proposed antenna is compared with that of the reference antenna and according to the observations, incorporation of the circular polarization leads to the reduction of the gain. Traditionally, the gain of a CP antenna was less than that of the reference LP antenna, mainly for the following three reasons. The first reason originates from the theoretical background that the gain of a CP antenna would be at least 3 dB less than that of the reference LP antenna [39,40]. The second

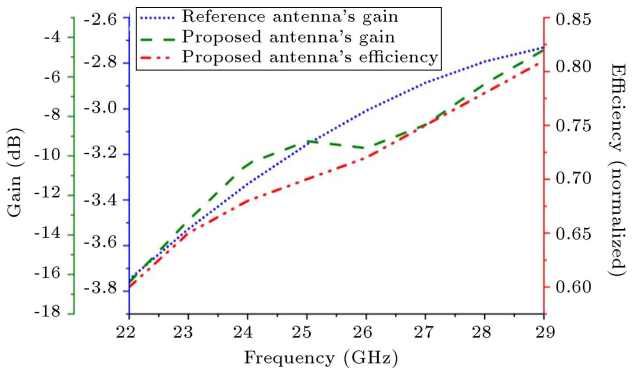

Figure 13. Gain and efficiency plot.

reason is that the antenna gain is dependent on the AR of polarization ellipse. More details about the gain of an antenna starting from circular polarization with $AR = 1$ through elliptical polarization with $AR > 1$ to the linear polarization with $AR \to \infty$ are given in [39–41]. Finally, to include the CP characteristics, the designed reference antenna should be loaded reactively or resistively. Here, the reactive loading is introduced with the small gap G. Creation of the air gap results in achieving CP property. However, the gap disrupts the actual current conduction path and, at the same time, it causes some undesired radiations from the edges of the gap, which in turn reduces the overall gain of the proposed antenna. The proposed CP antenna achieves a gain of -10.4 dBi at 24 GHz, while the reference antenna offers a gain of -3.3 dBi at that frequency. The maximum gain achieved by the proposed antenna is -4.5 dBi. The antenna efficiency varies from 60% to 81% over the operating band.

Although the gain of the CP antenna is less that of one LP reference antenna, they have two have different significances from an application perspective. For example, LP antennas are used with known polarization characteristics of the signal at both transmission and reception ends. However, this polarization characteristic of the received signal alters with respect to the transmitted one due to the transmission medium or reflection from some nearby obstacles; therefore, the LP antenna may not be suitable. In these cases, the CP antenna is preferred.

The 2D radiation patterns in both E and H planes at four different frequencies (23, 24, 26, and 27 GHz) of the operating band are depicted in Figure 14 along with the 3D pattern at 24 GHz. On the E plane, the pattern looks almost like the one that is depicted in Figure 8. The antenna exihibits HPBW of 115° and 75° on the E and H planes, respectively. This type of antenna, with its greater angular coverage, is a suitable candidate for short-range automotive radar due to its ability to accurately detect objects in the nearby environment surrounding the host car.

To determine the polarization of the wave ra-

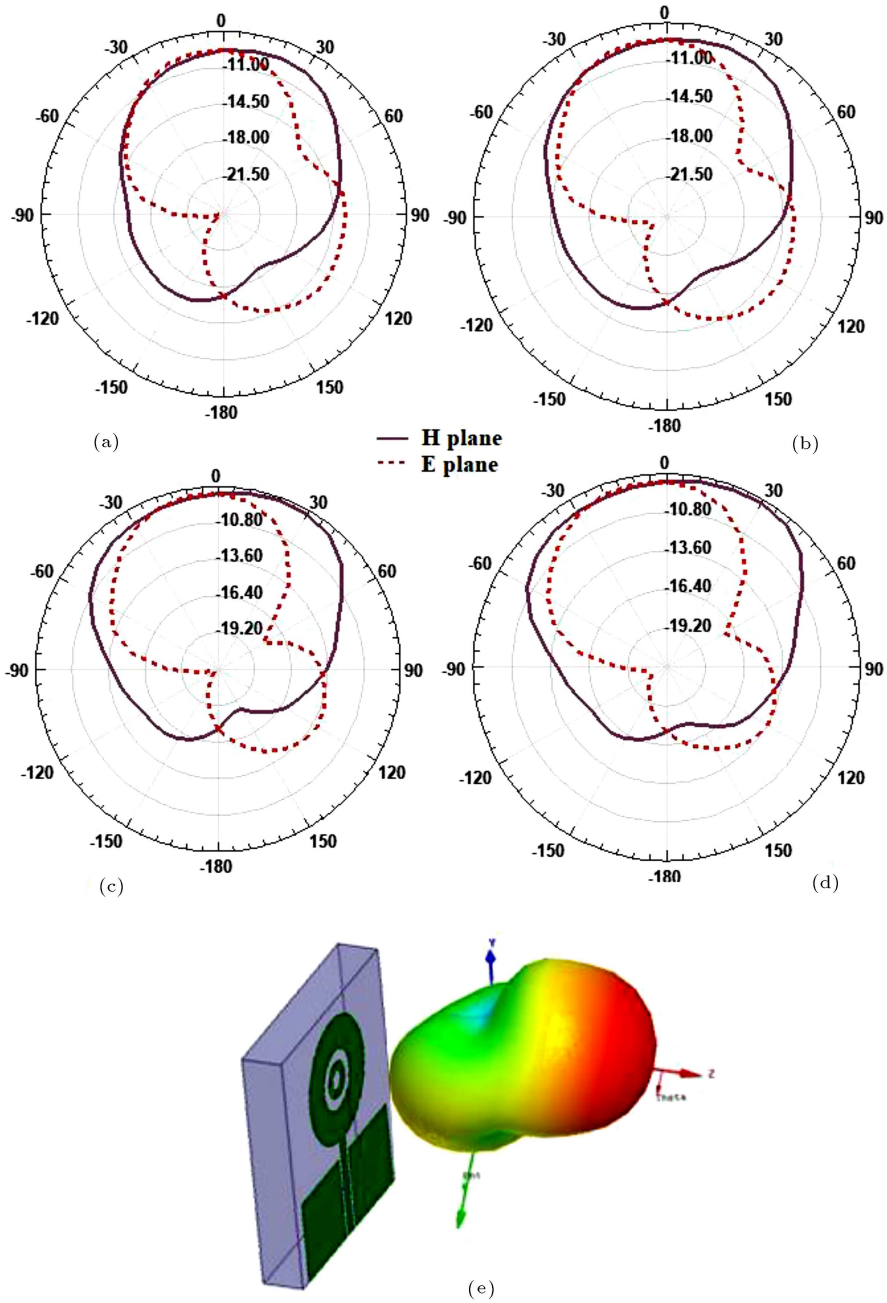

Figure 14. Radiation pattern of the proposed antenna: 2D pattern at: (a) 23 GHz; (b) 24 GHz; (c) 26 GHz; (d) 27 GHz; and 3D pattern at (e) 24 GHz.

diated from the antenna, the current distribution of the radiating patch at 26 GHz is identified and the same is depicted in Figure 15. The direction of the surface current at four different time phases of 0°, 90°, 180°, and 270° is shown in Figure 15(a)–(d), respectively. At each 90° time phase, the current vector is rotated about 90° in the clockwise direction. This indicates that the excited current radiates a Left-Handed Circularly Polarized (LHCP) wave. The E and H field distributions in the radiating patch at 24 GHz are shown in Figure 16(a) and (b), respectively. The E fields do not exist on the east and west sides, and the arrows representing the E field are inward and outward pointing to the south and north sides, respectively. The H fields form a closed loop, as shown in Figure 16(b). This field distribution confirms the excitation of TE_{11} mode at 24 GHz.

3.2. Measured S_{11} characteristics

The fabricated antenna prototype was characterized using a probe station (CASCADE Summit 11000 AP series) and a vector network analyzer (R&S VNA

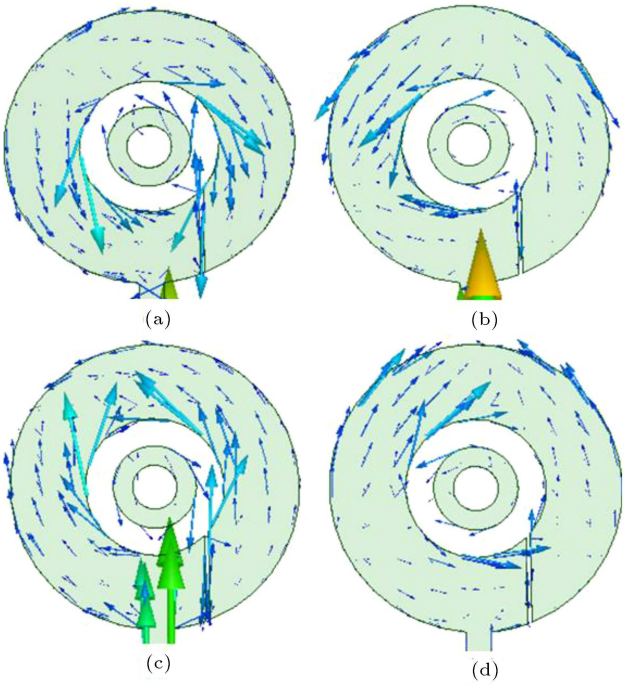

Figure 15. Surface current distribution at 26 GHz for different time phases; (a) 0°, (b) 90°, (c) 180°, and (d) 270°.

ZVA-40). Figure 17 shows the experimental setup for characterizing the fabricated prototype. To start the process, first, an antenna prototype is placed on the metal base of the probe station. The RF cable supplies the required signals as the input to the probe tip via probe head interface from the VNA. GSG infinity probe with the pitch size of 250 μm is used to excite the test antenna. The microscope just above the metal base of the probe station is used to check the proper alignment of the probe tip. The microscopic view can be seen in the probe station monitor and depicted in Figure 17(b). The probe is moved along the upward and downward directions to confirm the planarity of the probe tips. If it imposes an equal number of sliding marks from all three tips, the proper tip contact with the wafer can be confirmed. Next, the probe tips are calibrated to get the best possible error-free measurement result. Different calibration algorithms including SOL (Short Open Load), SOLT (Short Open Load Thru), LRM (Line Reflect Match), LRRM (Line Reflect Reflect Match), etc. are usually implemented within the VNA itself. Depending on the requirement, one of the calibration techniques is chosen. In this case, the SOL technique is implemented. The obtained measured and simulated results are presented in Figure 18. An undesired discrepancy in the measured result is observed in this figure. The critical factor responsible for this inconsistency is Residual Silicon Substrate (RSS) effect. During the dicing process, the extra silicon substrate of 0.2 mm in width is kept to ensure that the die will be free from any kind of

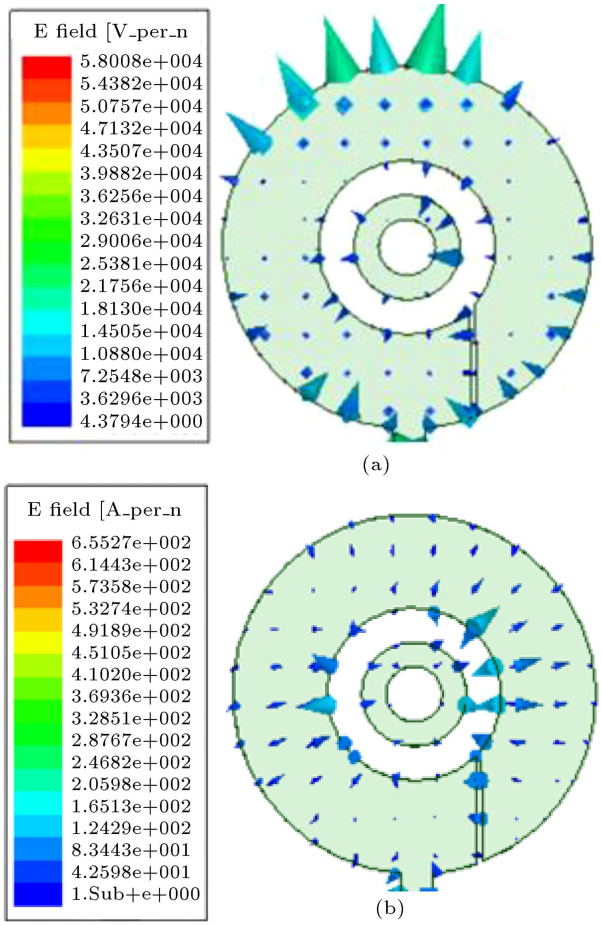

Figure 16. Field distribution in the radiating patch at 24 GHz; (a) E filed distribution and (b) H field distribution.

damage at the time of dicing. This extra lossy silicon substrate adversely affects the return loss characteristic of the test antenna. To validate this phenomenon, this condition was created in the simulation environment. The return loss characteristics of the antenna including the RSS effect is also plotted in Figure 18 along with the other two results. The graph confirms that the RSS effect degrades the antenna characteristics. The measured result is now matched with the post-fabrication simulation result to a great extent. However, reflection from the nearby metal components like the base of the probe station, probe tips, probe positioner, and microscope causes the measured bandwidth to shrink. In case all these negative factors are removed, the measured results are expected to match perfectly with the simulated one. The performance of the proposed antenna is compared with that of other contemporary antennas, the results of which are given in Table 1. Due to the miniaturization and substrate loss, the gain of the OCAs is lower than that of the PCB-based off-chip antennas. However, compared to the antenna reported in [42], the proposed antenna offers a significantly improved gain of -4.5 dBi, which makes it suitable for short-range automotive radar applications.

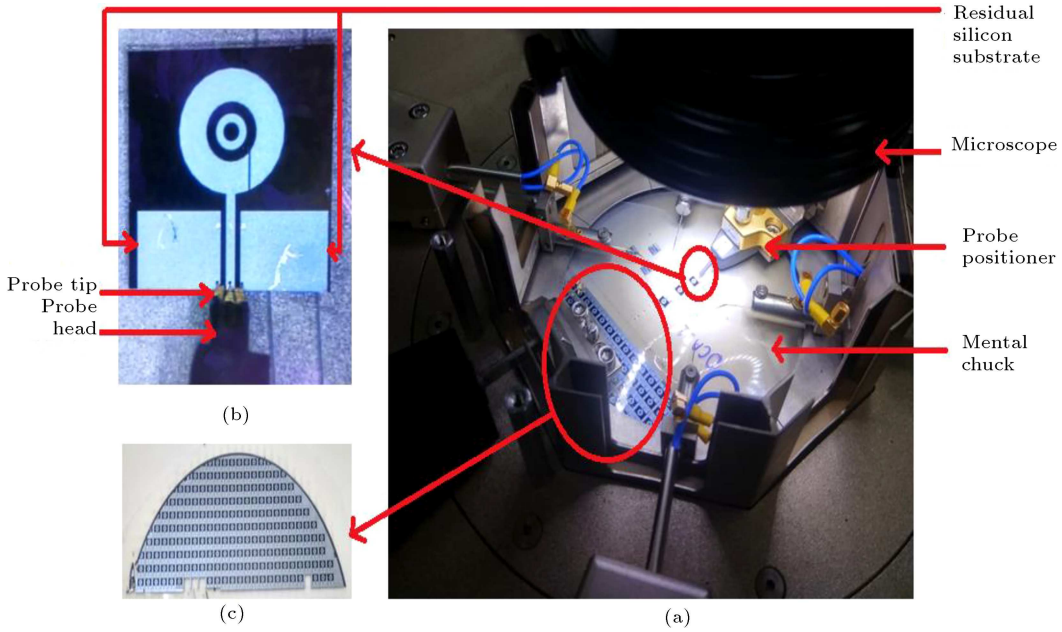

Figure 17. Antenna characterization process (a) Antenna prototype placed on CASCADE Summit 11000 AP series GSG probe station, (b) Microscopic view of the fabricated prototype, (c) $6''$ silicon wafer containing multiple antenna prototypes [Courtesy: Semi-conductor Laboratory, Chandigarh].

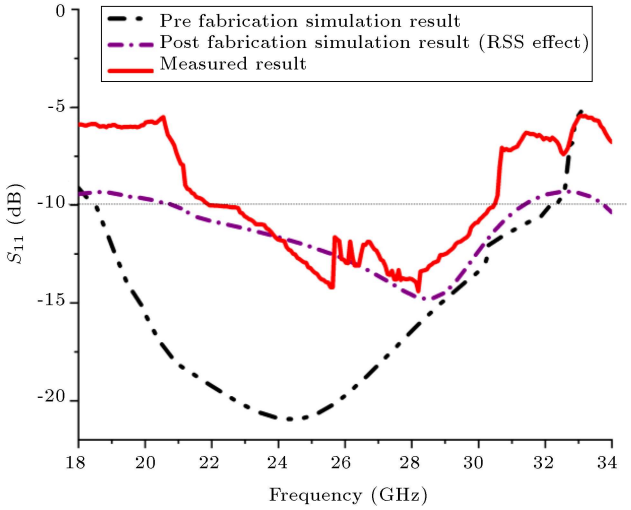

Figure 18. Comparison of pre-fabrication, post-fabrication, and measured result.

4. Post fabrication work

4.1. Gain enhancement

The proposed CP on-chip antenna has lower gain than the conventional off-chip antennas due to its low resistivity and high dielectric constant ($\varepsilon_r = 11.8$) of the silicon substrate. Low resistive silicon leads to a significant substrate loss, while high permittivity confines the greatest portion of the power within the substrate. These two factors contribute to degradation of the on-chip antenna. However, the gain offered by the proposed antenna is higher than that in [28,29,42]. To make the antenna suitably applicable to a real-case scenario, some additional post-fabrication works should be done to improve its gain characteristics. Though high resistive silicon can be used to improve the gain performance [43], the bulk CMOS process does not support such high resistive silicon [44]. The alternative and most suitable option for improving the OCA gain is to apply the micromachining technique wherein a low index region is introduced underneath the radiating antenna by removing a portion of the Si wafer from its bottom. The technique is very much useful as the designed antenna layout is not affected, and it only requires an additional post-fabrication step. In the proposed antenna, a slanted walled cavity of 0.2 mm in height is created just beneath the radiating patch and filled with air ($\varepsilon_r = 1$), as shown as an inset image in Figure 19. The gain characteristics of the antenna at different design steps are depicted in that figure. It can be observed that incorporation of air cavity enhances the gain of the proposed antenna even with respect to that of the reference antenna under consideration.

4.2. Effect of circuit element

In order to design a compact SoC using our designed antenna in the near future, other necessary active circuit elements like transistors, diodes, and passive elements like inductors, capacitors, transmission lines, etc. need to be placed in the close vicinity of the antenna. Therefore, their effect on the performance of the on-chip antenna can no longer be overlooked. The feature size of the active circuit component is almost very small; therefore, they cannot strongly affect the performance of the antenna. On the contrary, the effect

Table 1. Comparison between the proposed antenna and previously reported ones for 24 GHz application.

Ref. no.	Antenna type	Substrate	Size (mm^3)	f_c (GHz)	BW or fractional BW	Axial ratio BW (GHz)	Max. gain (dBi)	HPBW (°) at 24 GHz	Application
[25]	Array of patches	Rogers RO4003C	37 × 71.9 × 0.813	23.7	16.9%	NA	11.1	150 (E-plane) 10 (H-plane)	Developed for automotive radar applications
[18]	Franklin array	Rogers Corp. RO4003	90 × 25 × 0.2	24	0.4 GHz (23.8 to 24.2)	NA	> 10	17 (E-plane) 82 (H-plane)	Designed for vehicle blind spot information systems
[19]	Grid array	RO3003	146 × 18 × 1.6	24	25%	NA	11.59	145 (E-plane) 10.88 (H-plane)	Suitable for UWB automotive short-range radar sensors
[42]	On-chip antenna with a MIM capacitor loading AMC	Si	3.56 × 0.5 × 0.29	24	11.3 GHz (22.5 to 33.8)	NA	−41.8	NM	Can be used wireless chip area network
[29]	Meander-line	Si	1 × 0.75 × 0.3	24/60	15.7 GHz (10 to 25.7) and 8.2 GHz (58.4 to 66.6)	NA	−21.7 at 24 GHz) and −6.5 (at 60 GHz)	NM	Can be used for dual-band millimeter-wave communication systems
[28]	Conductor backed dipole	Si	3 × 0.5 × 0.3	24	10 GHz (20 to 30)	NA	−8	NM	Designed for short-range applications
This work	Concentric loop antenna	Si	3.8 × 4 × 0.678	24	8.5 GHz (21.9–30.4) Measured value	3.8 (23.2 to 27)	−4.5	115 (E-plane) 75 (H-plane)	Proposed for short-range automotive radar application

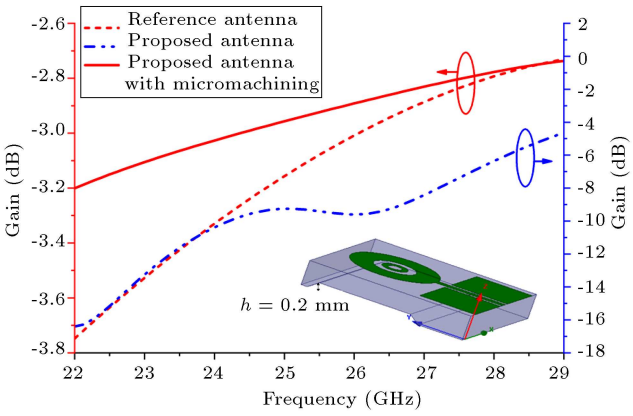

Figure 19. Gain comparison of reference antenna, proposed antenna, and micromachined proposed antenna.

of the passive components (whose size depends upon the operating frequency) cannot be ignored until an effective design strategy is opted. To analyze the whole system, two different simulators are needed; then, the antenna part is simulated in Ansys HFSS or CST studio suite based on the solving maxwell equation in the meshed structures, and the circuit part is simulated in the simulators like cadence or ADS based on the voltage or current bases nodal analysis. First, the antenna part is simulated in the EM simulator and then, their S parameter is extracted and imported to the circuit simulator. The optimization of both simulators is continuously performed until an optimum solution is obtained. It requires extensive research and it will be addressed in our next research article.

In this article, the effect of the most common circuit element, i.e., inductor, on the performance of the proposed antenna is analyzed. Both the on-chip inductor and antenna are designed using the HFSS design kit. The antenna is normally designed on the top metal layer due to the available larger metal thickness for efficient signal transmission through air. The

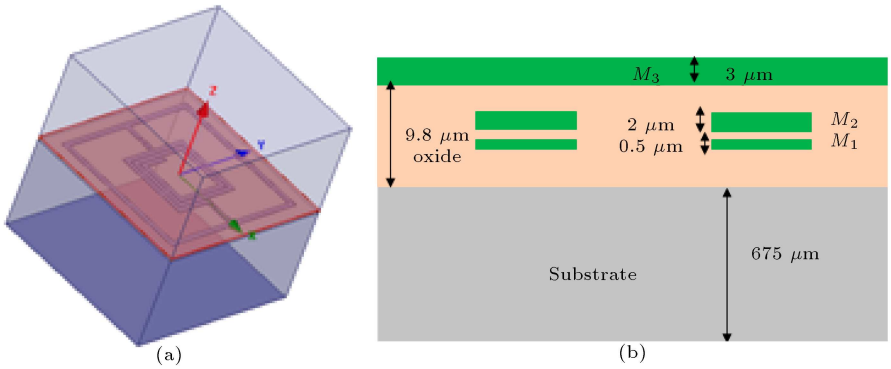

Figure 20. On-chip inductor design: (a) inductor model and (b) process layout.

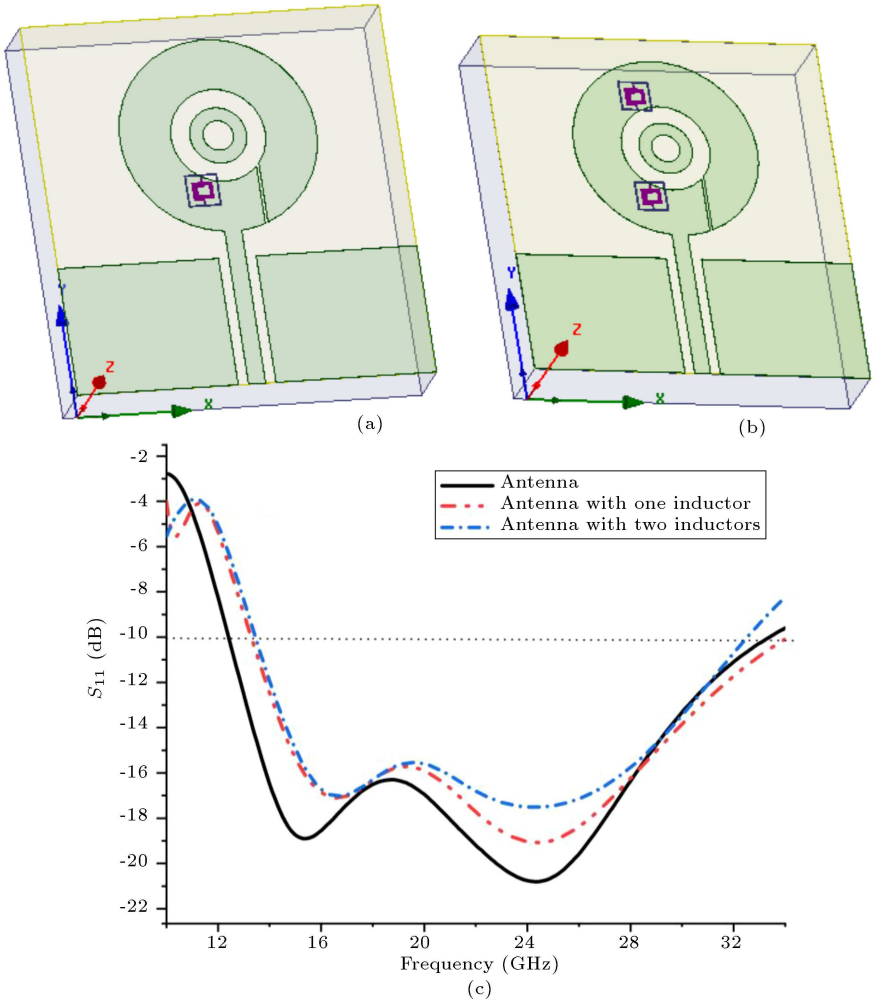

Figure 21. Effect of circuit elements on antenna: (a) incorporation of the first inductor, (b)incorporation of second inductor, and (c) return loss characteristics.

circuit element is generally placed in the intermediate metal layers, and they are connected to the antenna;if required, it can also be placed on the top layer. In this study, a 2.5 turn rectangular spiral inductor is designed (the inductor model is shown in Figure 20(a)) on the intermediate metal layer to analyze its effect on the characteristics of the antenna designed on the top metal layer. The process layout is shown in Figure 20(b). The line width and line spacing of the inductor are taken as 15 μm and 1.5 μm, respectively. The spiral inductor is designed in the M_2 layer of 2 μm in thickness while the underpass is designed in the M_1 layer of 0.5 μm in thickness, and they are connected through vias. First, a single inductor was placed, as shown in Figure 21(a) and then, another inductor with the same specifications is added (Figure 21(b)) to check if any changes will

happen due to the presence of that inductor, as shown in Figure 21(c). According to the graph, incorporation of the first inductor causes lower cut-off frequency to be right-shifted. Apparently, it can be deduced that these changes result from the inductor effect. Of note, the oxide layer thickness is now obtained as 9.8 μm, while its previous value is 0.5 μm. The thicker oxide layer results in a decrement in the capacitance value, which in turn forces the lower cut-off frequency to be right-shifted. This is further proved by incorporating the second inductor. According to the observations, the return loss characteristics remain approximately the same as obtained after the inclusion of the first inductor. Therefore, it can be concluded that the antenna works in an efficient way, considering the effect of the most common circuit element, i.e., inductor, and it is expected to remain operable considering the real effect of the other circuit elements too.

5. Conclusion

In this study, a circularly polarized on-chip antenna covering short-range automotive radar spectrum (22–29 GHz) was designed with just one additional pattern masking level, and the effects of the important design parameters on the antenna characteristics were analytically evaluated. The proposed antenna provided wide angular coverage along with the maximum gain of -4.5 dBi. The measurement results show that unlike the conventional microstrip patch antenna, any change in the substrate dimension during the fabrication process greatly affects the performance of the on-chip antenna. From the post-fabrication simulation and measured results, it can be inferred that Residual Silicon Substrate (RSS) plays an important role in the performance of the fabricated prototype, and this role of the substrate should be taken into account during the antenna design process in the simulation platform.

Acknowledgement

The authors gracefully acknowledge the financial supports provided by Visvesvaraya PhD scheme, Ministry of Communications and Information Technology, Govt. of India, Grant No. PhD-MLA/4(29)/2015-16/01 and Special Manpower Development Programme for Chips-to-System Design (SMDP-C2SD) under Govt. of India, Grant No. 9(1)/2014-MDD (Vol III). The authors are also thankful to Semi-Conductor Laboratory (SCL), Chandigarh for providing fabrication and measurement facility and, also, to Mr. Ayan Karmakar, Senior Scientist, SCL for his enormous and generous support.

References

1. Hung, C. and Weng, M. "Investigation of the silicon substrate with different substrate resistivities for integrated filters with excellent performance", *IEEE Transactions on Electron Devices*, **59**(4), pp. 1164–1171 (2012).

2. Pilard, R., Gianesello, F., Gloria, D., et al. "60 GHz HR SOI CMOS antenna for a system-on-chip integration scheme targeting high data-rate kiosk applications", *IEEE International Symposium on Antennas and Propagation (APSURSI)*, Spokane, WA, pp. 895–898 (2011).

3. Bao, X., Guo, Y., and Xiong, Y. "60-GHz AMC-based circularly polarized on-chip antenna using standard 0.18-μm CMOS technology", *IEEE Transactions on Antennas and Propagation*, **60**(5), pp. 2234–2241 (2012).

4. Babakhani, A., Guan, X., Komijani, A., et al. "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas", *IEEE Journal of Solid-State Circuits*, **41**(12), pp. 2795–2806 (2006).

5. Singh, H., Mandal, S., Mandal, S.K., and Karmakar, A. "Design of miniaturised meandered loop on-chip antenna with enhanced gain using shorted partially shield layer for communication at 9.45 GHz", *IET Microwaves, Antennas & Propagation*, **13**(7), pp. 1009–1016 (2019).

6. Narde, R.S., Mansoor, N., Ganguly, A., et al. "On-chip antennas for inter-chip wireless interconnections: Challenges and opportunities", *12th European Conference on Antennas and Propagation (EuCAP)*, London, pp. 1–5 (2018).

7. Shamim, M.S., Mansoor, N., Narde, R.S., et al. "A wireless interconnection framework for seamless inter and intra-chip communication in multichip systems", *IEEE Transactions on Computers*, **66**(3), pp. 389–402 (2017).

8. Masius, A.A. and Wong, Y.C. "On-chip miniaturized antenna in CMOS technology for biomedical implant", *AEU-International Journal of Electronics and Communications*, **115** (2019). https://doi.org/10.1016/j.aeue.2019.153025

9. Singh, H., Mandal, S., and Mandal, S.K. "Silicon-based ferrite loaded miniaturized on-chip antenna for biomedical applications with improved gain & efficiency", *European Microwave Conference in Central Europe (EuMCE)*, Prague, Czech Republic, pp. 179–182 (2019).

10. Ray, A., De, A., and Bhattacharyya, T.K. "2.45 GHz energy harvesting on-chip rectenna in 0.18 μm RF CMOS process", *IEEE Indian Conference on Antennas and Propogation (InCAP)*, Hyderabad, India, pp. 1–4 (2018).

11. Girma, M.G., Hasch, J., Sarkas, I., et al. "122 GHz radar sensor based on a monostatic SiGe-BiCMOS IC with an on-chip antenna", *7th European Microwave Integrated Circuit Conference.*, Amsterdam, pp. 357–360 (2012).

12. Mandal, S., Singh, H., Mandal, S.K., et al. "Design of a compact monopole on-chip antenna for 24 GHz automotive radar application", *International Workshop on Antenna Technology (iWAT)*, Miami, FL, USA, pp. 115–117 (2019).

13. Wegman, F. and Aarts, L. "Advancing sustainable safety: National road safety outlook for 2005–202", SWOV Institute for Road Safety Research, Leidschendam, pp. 1–215 (2006). ISBN-10: 90-807958-7-9 ISBN-13: 978-90-807958-7-7

14. 'European Environment Agency'. Available at: http://europa.eu.int/comm/energy_transport/library/lb_texte_complet_en.pdf, accessed 22 October (2003).

15. Technical requirements for vehicular radar systems. FCC, Washington, DC, FCC 47 CFR, Sec. 15.515, 2008.

16. Ju, Y., Jin, Y., and Lee, J. "Design and implementation of a 24 GHz FMCW radar system for automotive applications", *International Radar Conference*, Lille, pp. 1–4 (2014).

17. Kim, C., Kim, J., Baek, D., et al. "A circularly polarized balanced radar front-end with a single antenna for 24-GHz radar applications", *IEEE Transactions on Microwave Theory and Techniques*, **57**(2), pp. 293–297 (2009).

18. Kuo, C., Lin, C., and Sun, J. "Modified microstrip franklin array antenna for automotive short-range radar application in blind spot information system", *IEEE Antennas and Wireless Propagation Letters*, **16**, pp. 1731–1734 (2017).

19. Alsath, M.G.N., Lawrance, L., and Kanagasabai, M. "Bandwidth-enhanced grid array antenna for UWB automotive radar sensors", *IEEE Trans. Antennas Propag.*, **63**(11), pp. 5215–5219 (2015).

20. Gresham, I., Jenkins, A., Egri, R., et al. "Ultra-wideband radar sensors for short-range vehicular applications", *IEEE Trans. Microw. Theory Tech.*, **52**(9), pp. 2105–2122 (2004).

21. Gresham, I., Kinayman, N., Jenkins, A., et al. "A fully integrated 24 GHz SiGe receiver chip in a low-cost QFN plastic package", *Radio Freq. IEEE Radio Frequency Integrated Circuits (RFIC) Symposium.*, San Francisco, CA, p. 4 (2006).

22. Jain, V., Sundararaman, S., and Heydari, P. "A 22–29-GHz UWB pulse-radar receiver front-end in 0.18-μm CMOS", *IEEE Transactions on Microwave Theory and Techniques*, **57**(8), pp. 1903–1914 (2009).

23. Krishnaswamy, H. and Hashemi, H. "A 4-channel 24–27 GHz UWB phased array transmitter in 0.13 μm CMOS for vehicular radar", *Custom Integr. Circuits Conference.*, San Jose, CA, pp. 753–756 (2007).

24. Jain, V., Tzeng, F., Zhou, L., et al. "A single-chip dual-band 22-29-GHz/77-81-GHz BiCMOS transceiver for automotive radars", *IEEE Journal of Solid-State Circuits*, **44**(12), pp. 3469–3485 (2009).

25. Yu, C., Li, E.S., Jin, H., et al. "24-GHz horizontally-polarized automotive antenna arrays with wide fan beam and high gain", *IEEE Transactions on Antennas and Propagation*, **67**(2), pp. 892–904 (2019).

26. Suetsugu, S., Zhang, M., Hirokawa, J., et al. "Design of a 45-degree linearly-polarized slot array fed by a coaxial line in the millimeter-wave band", *International Workshop on Electromagnetics: Applications and Student Innovation Competition (iWEM)*, Hsinchu, pp. 1–2 (2015).

27. Hamberger, G.F., Siart, U., and Eibert, T.F. "A dual-linearly polarized receive antenna array for digital beamforming in automotive use", *IEEE Asia Pacific Microwave Conference (APMC)*, Kuala Lumpar, pp. 17–20 (2017).

28. Shamim, A., Roy, L., Fong, N., et al. "24 GHz on-chip antennas and balun on bulk Si for air transmission", *IEEE Transactions on Antennas and Propagation*, **56**(2), pp. 303–311 (2008).

29. Lin, C-Y., Lin, Y-S., Lu, H-C., et al. "Design and implementation of A 24-/60-GHz dual-band monopole meander-line planar CMOS antenna", **54**(7), pp. 1731–1737 (2012).

30. Cheema, H.M. and Shamim, A. "The last barrier: on-chip antennas", *IEEE Microwave Magazine*, **14**(1), pp. 79–91 (2013).

31. WU, T.T. "Theory of thin circular loop antennas", *Journal of Mathematical Physics*, **3**, pp. 1301–1304 (1962).

32. Rao, B.R. "Far field patterns of large circular loop antennas: Theoretical and experimental result", *IEEE Trans. Antennas Propagation*, **16**(2), pp. 269–270 (1968).

33. Elliott, R.S., *Antenna Theory and Design. Piscataway*, NJ: IEEE Press, pp. 71–73 (2003).

34. Nakano, H., Tsuchiya, N., Suzuki, T., et al. "Loop and spiral line antennas at microstrip substrate surface", *Proc. 6th Int. Conf. Antenna and Propagation (ICAP)*, Japan, pp. 196–200 (1989).

35. Altshuler, E.E. "The Traveling-wave linear antenna", *IRE Trans. Antennas Propagation*, **9**(4), pp. 324–329 (1961).

36. Okuba, S. and Tokumaru, S. "Reactively loaded loop antennas with reflectors for circular polarization", *Trans. IECE Jpn.*, **65**(8), pp. 56–64 (1982).

37. Iizuka, K. "The circular loop antenna multiloaded with positive and negative resistors", *IEEE Trans. Antennas Propag.*, **13**(1), pp. 7–20 (1965).

38. Lo, Y.T., Solomon, D., and Richards, W.F. "Theory and experiment on microstrip antennas", *IEEE Trans. Antennas Propagat.*, **AP-27**(2), pp. 137–145 (1979).

39. Milligan, T. "Polarization loss in a link budget when using measured circular-polarization gains of antennas", *IEEE Antennas and Propagation Magazine*, **38**(1), pp. 56–58 (1996).

40. Roy, S.K. "Study of the gain of circularly or elliptically polarized antennae", *Indian Journal of Pure and Applied Physics*, **39**(9), pp. 603–606 (2001). ISSN: 0975-1041 (Online); 0019-5596 (Print).

41. Toh, B.Y., Cahill, R., and Fusco, V.F. "Understanding and measuring circular polarization", *IEEE Transactions on Education*, **46**(3), pp. 313–318 (2003).

42. Jiang, L., Mao, J., and Leung, K.W. "A CMOS UWB on-chip antenna with a MIM capacitor loading AMC", *IEEE Transactions on Electron Devices*, **59**(6), pp. 1757–1764 (2012).

43. Watanabe, S., Harun-ur Rashid A.B.M., and Kikkawa, T. "Effect of high-resistivity Si substrate on antenna transmission gain for on-chip wireless interconnects", *Japanese Journal of Applied Physics*, **43**(45), pp. 2297–2301 (2004).

44. Shamim, A. and Zhang, H. "On-chip antenna: challenges and design considerations", *Antennas and Propagation for 5G and Beyond*, pp. 123–155 (2020).

Biographies

Sanjukta Mandal received her BTech degree in Electronics and Instrumentation Engineering and MTech degree in Communication Engineering from University of Kalyani in 2012 and 2014, respectively. After MTech, she worked as a Project Fellow in the project entitled "Design of Mobile Robot Technology for Security, Surveillance, Mining, Building Inspection and Planetary Exploration (ESC0112/RP-1)" in CSIR-CMERI, Durgapur, West Bengal, India. She is currently pursuing her PhD program at National Institute of Technology Durgapur, West Bengal, India under the prestigious Visvesvaraya PhD scheme of Ministry of Electronics and Information Technology (MeitY), Govt. of India. Her current research interests include on-chip antenna design for short range communication, gain enhancement of on-chip antenna, and equivalent circuit modelling of on-chip antenna. She has published 14 research papers in international journals and conferences.

Harshavardhan Singh received his BE degree in Electronics and Communication Engineering (ECE) from NRI-Institute of Information Science and Technology (NIIST), RGPV, Bhopal in 2010 and MTech degree in Electronics and Communication Engineering (Telecommunication Engineering) from National Institute of Technology Durgapur (NITD), West Bengal in 2014. He joined NITD as a research scholar in 2015 for completion of his PhD degree. He received scholarship from the Visvesvaraya PhD scheme, The Ministry of Electronics and Information Technology, Govt. of India during his research work. Currently, He is working as an Assistant Professor at the Department of Electronics and Communication Engineering, University of Engineering and Management, Kolkata, India. His primary areas of research include On-chip antennas, System on Chip (SoC) based architectures, Chip inductors, Antenna arrays, and RF circuits for wireless communication. He has been the reviewer of many international journal and conferences such as Progress in Electromagnetic Research (PIER), Springer Nature, etc. He has published 17 research papers in International Journals and Conferences.

Sujit Kumar Mandal received BSc degree in Physics Honours from University of Calcutta in 2001. He completed BTech and MTech in Radio Physics & Electronics from Institute of Radio Physics & Electronics, C. U. in the year 2004 and 2006, respectively. He received PhD degree from National Institute of Technology, Durgapur where he is presently an Assistant Professor at the Department of Electronics and Communication Engineering. He has published about 50 research papers in peer-reviewed international journals and conference proceedings. His present research areas include application of soft computing techniques in antenna array optimization, time-modulated antenna arrays, microstrip patch antenna, RF energy harvesting, and on-chip antenna design. Dr Mandal is a member of IEEE.

Ashis Kumar Mal received BSc degree in Electronics and (Tele)Communications Engineering from Bengal Engineering College (now IIEST) Shibpur and MSc degree from IIT Kanpur in 1989 and 1994, respectively. He obtained his PhD from IIT Kharagpur in 2009 in the field of Microelectronics and VLSI. He has around 25 years of teaching experience and currently, he is with NIT Durgapur as an Associate Professor serving the Department of Electronics and Communication Engineering. He has published more than 60 articles in refereed international journals and conferences. As a member of IEEE Solid-State Circuits Society (SSCS), his interest includes Analog/Mixed Signal VLSI (AMS) and Digital-Assisted Analog (DAA).

Rajat Mahapatra was born in Kolkata, India in 1972. He received his MTech and PhD degrees from the Indian Institute of Technology (IIT) Khargapur, India in 1999 and 2005, respectively. During 2005–2010, he was a Research Associate with the School of Electrical, Electronics and Communication Engineering, Newcastle University, Newcastle upon Tyne, UK. He is currently an Associate Professor at the Department of Electronics and Communication Engineering, National Institute of Technology (NIT), Durgapur, India. He

has around 80 publications in referred international journals and conference proceedings. His areas of interest include physics, technology and characterization of MOS devices, memory, and sensors.

Pamidiparthi Ravi Teja Naidu is currently working as a Scientist 'D' at Semi-Conductor Laboratory, Mohali at the Department of space, Government of India. He is a graduate in Avionics from Indian Institute of Space Science and Technology (IIST), Thiruvananthapuram, Kerala. He joined the Semi-Conductor Laboratory in 2015 and since then, he has been involved in various MEMS and RF Device fabrication, testing, and packaging processes. His specialized experience is in lithographic process and their equipment maintenance and up keeping. He has five years of experience in MEMS fabrication process. He is also a life time member of ISSS and ISSE Society of India. He has published 5 technical papers in national and international conferences to his credit.