Scientia Iranica D (2022) 29(5), 2437–2449

Sharif University of Technology
Scientia Iranica
Transactions D: Computer Science & Engineering and Electrical Engineering
http://scientiairanica.sharif.edu

Delayed least mean squares filters suppressing the radio frequency interference in cosmic rays radio detection

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Received 20 June 2018; received in revised form 8 September 2020; accepted 4 January 2021

KEYWORDS
Pierre auger observatory;
Auger engineering radio array;
FPGA;
FIR filter;
Least mean squares algorithm.

Abstract. Extensive Air Showers (EAS), initiated by Ultra-High-Energy Cosmic Rays (UHECRs), generate geo-synchrotron and geo-magnetic radiations and they are, also, the source of excess charge processes. In the frequency range of 10 to 100 MHz, coherent radiation is formed. Many experiments use the radio detection technique for studying EAS features. The Auger Engineering Radio Array (AERA), part of the Pierre Auger Observatory, uses hundreds of radio antennas working in the frequency range of 30 to 80 MHz to support the investigation of UHECRs together with the standard surface and fluorescence detectors. The AERA radio frequency range is significantly contaminated by the human-made and usually narrow-band Radio Frequency Interference (RFI), e.g., short-wave radio transmitters. The presence of RFIs in the detected signals increases the ratio of spurious triggers; in consequence, empty data inflate the databases. This study proposes replacing the currently used IIR-notch nonadaptive filter by the delayed version of the well-known Least Mean Squares (LMS) algorithm, which offers crucial advantage adjustment. The current study implemented 32/64-stage Delay Least Mean Squares (DLMS) filters on cost-effective Cyclone® IV and Cyclone® V as non-canonical Finite Input Response (FIR) with a sufficient safety margin for a global clock being at least 20% higher than 200 MHz, which equals the ADC sampling frequency.

1. Introduction

Ultra-High-Energy Cosmic Rays (UHECRs) penetrating the Earth atmosphere generate avalanches of charged and neutral particles, known as air showers. The origin of UHECRs remains a mystery to this day since their discovery in the late 1930s [1–5]. Many experiments, e.g., the Pierre Auger Observatory [6], detect Extensive Air Shower (EAS) to estimate the energy and arrival direction of UHECRs and to obtain cosmic ray composition.

Radio detection of air showers began in the 1960s [7,8]. In the last decades, the LOPES [9] and CODALEMA [10] collaborations refreshed and improved the performance of the radio detection technique. The Auger Engineering Radio Array (AERA) [11–14] is the third type of a UHECR detector at the Pierre Auger Observatory to study EAS with an energy rate larger than 10^{17} eV.

Crucial mechanisms responsible for radio-wave

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doi: 10.24200/sci.2021.51272.2092

generation are geomagnetic radiation [15] and Askaryan charge-excess [16]. A transverse electric current is generated by the magnetic field of the Earth in the shower front. Ionization of air molecules by high-energy photons in EAS generates a charge excess. Additionally, Cherenkov effect was observed in [17,18].

Detection of radio signals is possible only for coherent emission. The radio-band is limited by the analog bandpass filter for 30 to 80 MHz. The coherent emission even to the GHz region may be observed. The above range has been selected to avoid the FM radio band (88–108 MHz) and to eliminate signals reflecting many times in the atmosphere, e.g., coming from long-distance storms. In the 3080 MHz range, human-made Radio Frequency Interferences (RFIs) and Galactic noise are mainly observed.

In order to avoid spurious detection, input data must be cleared from RFI. Total removal is rather impossible and RFI should be at least suppressed significantly as in [19–24]. A self-triggered algorithm runs itself on ADC traces. It analyzes pulses based on the characteristics described in [25]. Crucial results were already obtained from the third Auger detector - the radio one [26,27]. New triggers were also proposed in [28,29].

2. The normalized LMS algorithm

The Normalized LMS (NLMS) filter proposed by the referenced studies [30,31] in the 1960s is rather complex due to variables division as part of its requirements (see Eq. (1)). It solves the normalization problem by the learning factor which is updated at every iteration:

$$\mu(i+1) = \frac{\mu}{\gamma + \sum_{j=0}^{M-1} X^2(i-j-DL)}, \qquad (1)$$

where $\gamma > 0$ eliminates a singularity related to a division by zero, M is the length of the Finite Input Response (FIR) filter, and DL denotes the Delay Line used for the introduction of a gap between the original and filtered signals. In this case, the distortion factor of the filtered signal was significantly reduced. $\boldsymbol{X}$ denotes the samples with $\boldsymbol{i}$ and $\boldsymbol{j}$ indices, respectively. The division operation in the Cyclone FPGAs requires a 24-stage pipeline LPM_DIVIDE Mega-function, which is slow as it is not supported by Digital Signal Processing (DSP) blocks but implemented only in logic cells. The canonical FIR implementation requires additionally five pipeline stages for a 32-stage length.

Practically, the NLMS filter [32] could be implemented at only 16 stages (NLMS16). Although Table 1 gives the convergence time ~ 2.6 μs for 32 stages, this is for a pure filter only (i.e., without any other data processing modules for radio-detection in the FPGA). Figure 1 shows the timing for the NLMS32. Although

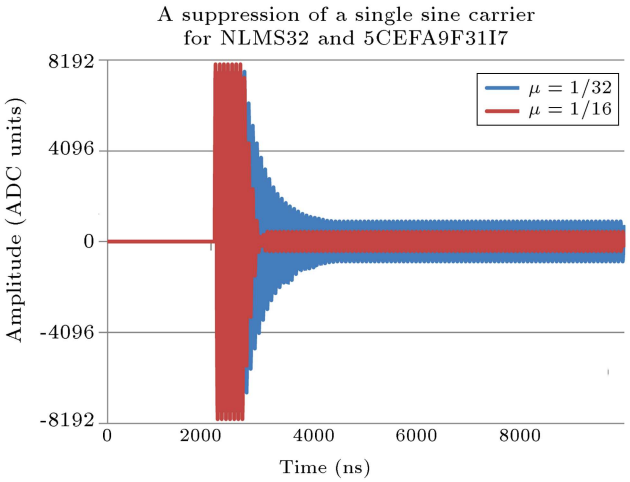


Figure 1. Timing for the NLMS32 suppression for 5CEFA9F31I7.

the convergence is extremely fast, the suppression factor is rather poor and the filter retains 5% or 10% of the RFI carrier. Additional algorithms implemented on 5CEFA9F31I7 dramatically decrease the registered performance and the filter fails.

As the implementation of a 32-stage NLMS with other Data Acquisition (DAQ) routines in the FPGA was problematic, the Altera Hardware Description Language (AHDL) code was simplified by using the direct LMS architecture, which could be pipelined and re-timed to give a functionally equivalent representation referred to as Delayed LMS (DLMS) [33,34]. This variant can be applied directly to the existing radio electronics in the EP4CE75F29C6 FPGA and tested in the field.

3. Previous DLMS implementations

The idea of the DLMS algorithm is not new. Many publications reported theoretical analyses and implementations. However, the present implementation requires a very high speed ($\geq$ 200 MHz) in cost-efficient FPGAs, providing simultaneously low-power consumption. Military Altera families, e.g., Stratix II or Stratix III, equipped with 6-input LUTs (Look Up Tables) allow more efficient synthesis than 4-input LUT cost-efficient families like Cyclone II-V [35]. Stratix families provide a very high registered performance (up to 500 MHz). However, they have two fundamental disadvantages: price (very expensive for mass production of several hundred detectors) and power consumption. Available exclusively in Stratix III FPGAs, Programmable Power Technology (PPT) theoretically enables every programmable logic to be configured either in high-speed or low-power modes, respectively. All other FPGAs contain blocks that are designed to run at only one speed, the highest possible speed, to support timing critical paths. Using the PPT in Stratix III FPGAs,

Table 1. A timing for various LMS variants. variants for FPGAS 5CEFA9F31I7 and for 5CSXFC6D6F31C6 were tested on the prototype front-end board for the Pierre auger surface detector [44,45] and on the Cyclone V SOC development kit(terasic), respectively. the others were simulated in the Modelsim (university program).

Type	FPGA	μ^{-1}	$Slack_{Fast}$ (ns)		$Fmax_{Slow}$ (MHz)		1-sine max
	Cyclone V		−40°C	100°C	−40°C	100°C	Supp. (μs)
	Cyclone IV		0°C	85°C	0°C	85°C	
NLMS16	5CEFA9F31I7 mea	64	1.544	0.992	**126.45**	**128.82**	∼ 5.0 (10%)
		32	1.555	1.131	**126.2**	**130.99**	∼ 2.6 (5%)
		16	1.544	0.992	**126.45**	**128.82**	∼ 1.6 (2.5%)
	EP4CE75F29C6 sim	64	1.339		**179.31**	**156.54**	*Failed*
		32	1.339		**179.31**	**156.54**	*Failed*
NLMS32	5CEFA9F31I7 mea	32	1.609	1.204	**128.14**	**132.26**	∼ 2.6 (10%)
		16	1.609	1.204	**128.14**	**132.26**	∼ 0.9 (5%)
DLMS32	5CEFA9F31I7 mea	256	2.369	1.703	**173.19**	**180.02**	∼ 2.2 (zero)
		128	2.397	1.723	**181.13**	**189.21**	∼ 5.0 (zero)
		64	2.319	1.8	**168.38**	**173.67**	*No CONV*
	5CEFA7F31C6 sim	256	1.856	1.341	202.06	**197.75**	∼ 2.2 (zero)
		128	2.063	1.585	**199.76**	202.43	∼ 5.0 (zero)
		64	2.15	1.675	211.1	208.64	*No CONV*
	5CSXFC6D6F31C6 mea	256	1.924	1.554	**180.77**	**183.28**	∼ 2.2 (zero)
		128	1.704	1.422	**174.25**	**174.19**	∼ 5.0 (zero)
		64	2.048	1.582	**186.99**	**188.5**	*No CONV*
	EP4CE75F29C6 sim	256	1.958		229.46	206.87	*No CONV*
		128	1.945		221.83	200.36	∼ 5.0 (zero)
		64	2.322		245.04	222.67	∼ 1.1 (−2..2)
		32	2.131		232.34	208.9	*No CONV*

all logic blocks in the array are set to low-power mode, except those designated as timing critical. With only the timing critical blocks set to the high-speed mode, power dissipation in Stratix III devices should theoretically be substantially reduced. Practically, we measured the 600 mW static power consumption in the Stratix III development kit in comparison to only 100 mW for Cyclone III. No optimization of the route for fast tracks reduced the power for Stratix below the Cyclone level.

Yi et al. [36] proposed a re-timed, DLMS architecture which allowed a 66.7% reduction in delays and 5 times faster convergence time, thereby yielding superior performance in terms of throughput rate, compared to previous work.

However, the Virtex-II FPGA technology yields a throughput rate of only 182 MSps. This is still not enough to meet the requirements (ADC sampling = 200 MHz + at least 20% of safety margin).

Dong et al. [37] considered "High-speed FPGA Implementation of an Improved LMS Algorithm", but for 60 or 120 MHz sampling. Again, it is too slow for our goal.

Several others use variants of the LMS algorithm for audio techniques (e.g., [38–40]). This is of course not helpful for our measurements. We need to meet contradictory attributes: very high speed, wide safety margin, low power consumption (due to its being supplied from solar panels), and cost efficient (due to volume production). For this reason, we must optimize the existing algorithms to reach an operational variant for cosmic ray detection.

4. Our DLMS implementation

Figure 2 shows our modified 32-stage DLMS algorithm, which is based on the algorithms described in [33,34]. In comparison to the original solution, our algorithm contains additional pipeline stages that improve the registered performance (a total speed). The block in

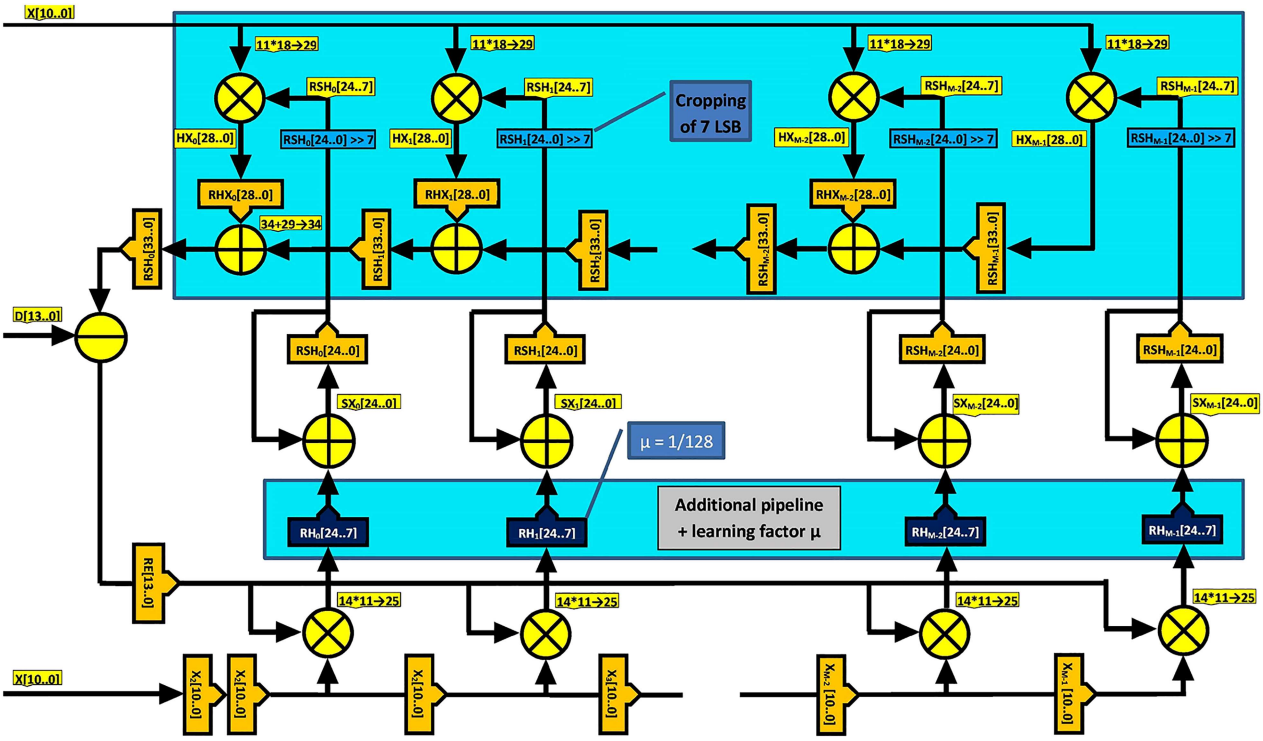


Figure 2. The structure of DLMS32. The input $D[13..0]$ corresponds to data to be filtered. Additional input $X[10..0]$ is a reference node derived from the original data but delayed for 64 clock cycles and with the 3 least significant bits neglected ($X[10..0] = (D[13..3] >> 3)$) delayed by LPM SHIFTREG with64 stages. Embedded multipliers are working in 11×18-bit mode giving 29-bit result data. These data summed in 32-stage chain give 34-bit data subtracted from the input 14-bit data. The graphs show where particular variables are cropped (the least significant bits are neglected). Such an operation keeps a reasonable width of processed variables. The block 'Additional pipeline + learning factor μ was inserted after several attempts to reach a sufficient register performance and a safety margin. The 25-bit sums $SX_k[24..0]$ are obtained from 25-bit $RSH_k[24..0]$ registers and 19-bit $RH_k[24..5]$ supported registers. Most significant bits in the sums are supplemented by the sign bit $RH_k[24]$ according to the rules for summation of two's-complement signed variables. The configuration shown in the graph corresponds to the learning factor $\mu = 1/32$. However, if the width of the supported register was to be shortened to, for example, $RH_k[24..9]$ with 4 higher bits replaced by the sign bit, the implementation would correspond to the learning factor $\mu = 1/512$ ($512 = 32 << 4$). This feature allows a dynamic change of the learning factor in a simple way by using a multiplexer (controlled from outside) instead of fixed RH_k registers. However, we should keep in mind that the cost of some additional comfort in filter control is a narrower safety margin.

Figure 2 denoted as "Additional pipeline + learning factor μ" contains a 3-bit multiplexer allowing dynamical modification of learning factors from $\mu = 1/8(2^{-3})$ to $\mu = 1/1024(2^{-10})$. A grid 2^{-n} for the learning factor, where n is an integer number, eliminates a division operation. A change in the learning factor from 2^{-n} to $2^{-n\pm1}$ corresponds simply to a change of the address in the multiplexer by one.

The algorithm provides a very short convergence time, especially for learning factors $\mu^{-1} = 512$, 256, and 128 for Cyclone®V 5CEFA9F31I7 and 5CEFA7F31C6 as well as for $\mu^{-1} = 128$ and 64 for Cyclone®IV EP4CE75F29C6 (the FPGA currently used in the AERA radio stations).

Figure 3 shows the simulation results of Cyclone® V FPGAs. The mono carrier is removed totally in a few μs for $\mu^{-1} = 512$ (3.92 μs), 256 (3.2 μs), and 128 (5.92 μs). However, for $\mu^{-1} = 1024$, the convergence is too slow and for $\mu^{-1} = 64$, the convergence totally fails. Nevertheless, this variant can be easily tested in a real field condition in Malargüe, Argentina in' Cyclone® IV EP4CE75F29C6.

In the ideal case as shown in Figure 3, which does not occur in practice, the mono-carrier is totally removed. However, four mono-carriers related to short-wave transmitters are observed in typical pampas conditions. At the frequencies of these four carriers, the IIR filter currently in use is tuned. Figure 4 shows the suppression of four mono-carriers, which seems to be completely different from that of a single RFI. A higher learning factor provides faster convergence. The behavior seems to be monotonic. Nevertheless, learning factors larger than $\mu^{-1} = 256$ do not provide a sufficient convergence speed.

The DLMS32 algorithm provides a sufficiently fast speed for the industrial version of FPGAs, which

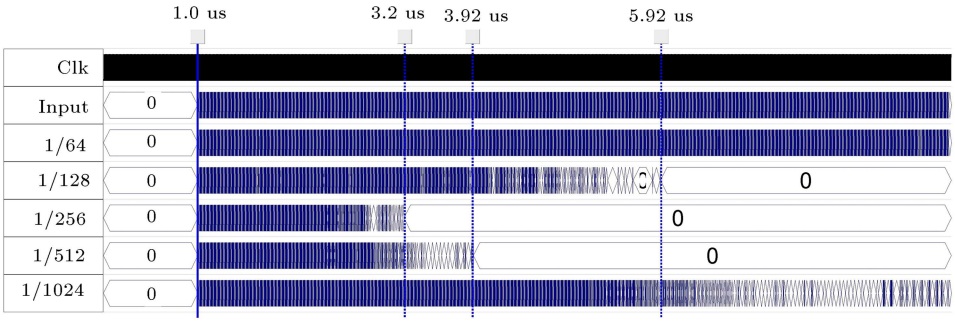


Figure 3. Timing for various DLMS32 variants with $\mu^{-1} = 64$, 128, 256, 512 and 1024, respectively, for Cyclone® V FPGA 5CEFA7F31C6. Only for $\mu^{-1} = 128$, 256, and 512, a convergence is fast enough.

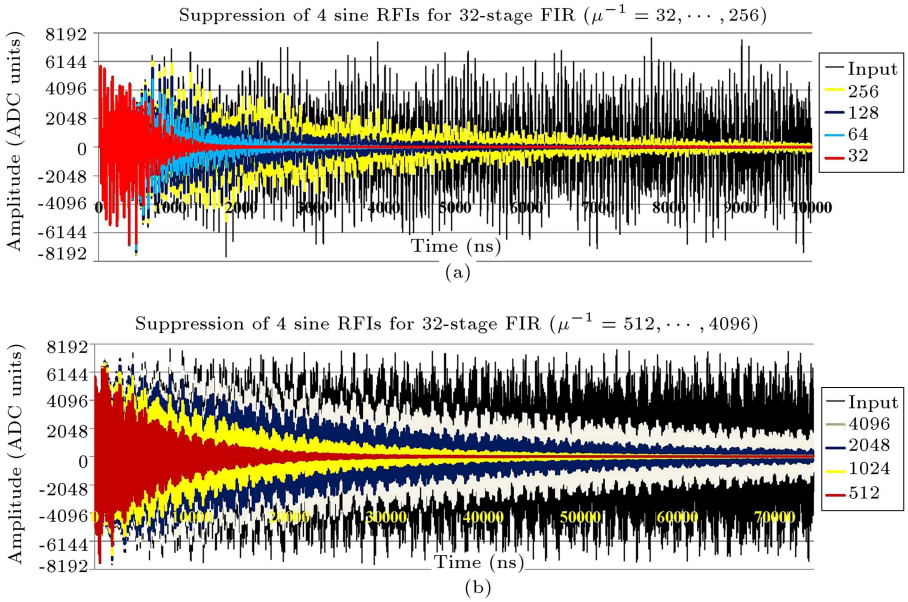


Figure 4. Timing for DLMS32 suppression for 5CEFA9F31I7. Each plot presents 5 signals: the input and filtered with the learning factors $\mu = 1/32$, 1/64, 1/128, and 1/256 (a) as well as with learning factors $\mu = 1/512$, 1/1024, 1/2048, and 1/4096 (b), respectively.

are produced only in a middle-speed grade (with a suffix "7"). The largest FPGA (e.g., 5CEFA9F31I7) is also produced only in a middle speed grade.

5. 32- vs. 64-stage FIR

A longer FIR filter provides more efficient RFI suppression, especially for lower frequencies, when a wave of a single period is on the edge of the filter length. For 200 MHz sampling ($T = 5$ ns), 32 stages correspond to 160 ns, equivalent to 6.25 MHz of RFI. Below this frequency, the filter efficiency dramatically declines. In this case, a 64-stage filter is recommended. Theoretically, this should not be the case in a real system due to the existence of an analog band-pass input filter with cut-off frequencies 30 and 80 MHz. However, we observed Fourier peaks (Figure 5) outside of this filter range [41,42]. A longer filter means higher power consumption. The final configuration is selected after tests in real pampas environmental conditions. Radio detectors are spread over a large area. The level of contamination varies from one place to another. Perhaps, an area suffering greater contamination would require a longer filter, while in relatively "quiet" regions, a 32-stage filter could be a sufficient option.

Figure 6 shows the suppression efficiency of a 64-stage FIR filter. For all learning factors, the convergence is fine, especially for $\mu^{-1} = 32$, 64, 128, and 256. Of note, the convergence for $\mu^{-1} = 32$ is worse than that for $\mu^{-1} = 64$. The optimization of the learning factor is a significant topic. Figure 7 shows the suppression of four carriers turning on sequentially. It is clearly visible that independent of the number of carriers, the suppression is perfect. The 64-stage FIR gives faster convergence at ~ 2 μs; however, this feature is not crucial for the contamination structure. Nevertheless, it may be useful for large environmental noise fluctuations.

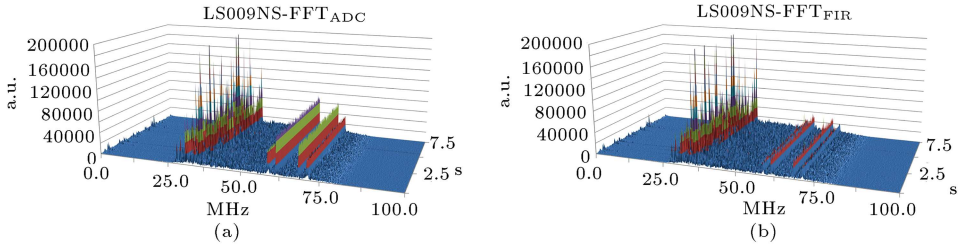


Figure 5. FFT for ADC and FIR filters with $D = 128$ for long-term (7.5 s) data from the radio station LS009 and NS polarization. We saw four mono-carriers, but with additional low-frequency non-stationary RFI. The presence of the variable in time RFI reduces the efficiency of the LP filter [41,42].

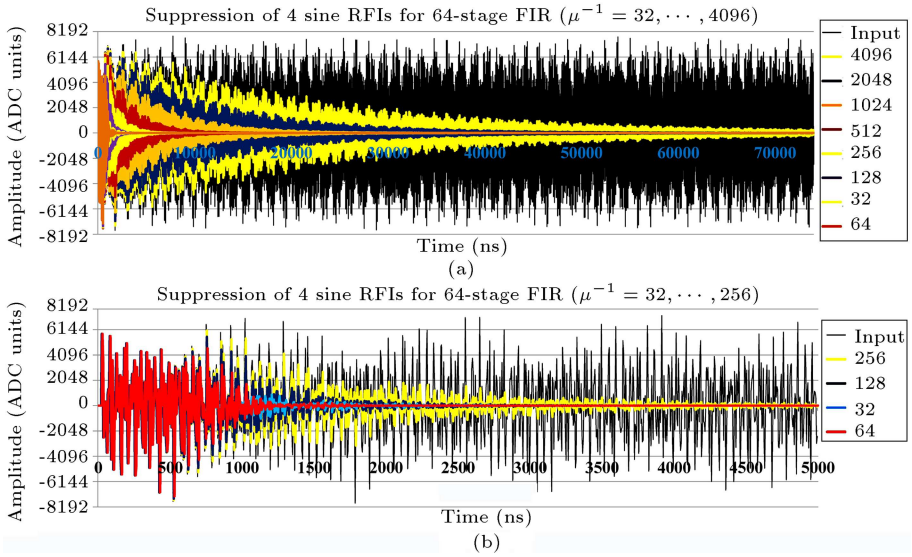


Figure 6. Timing for DLMS64 suppression for 5CEFA9F31I7. The description of the signals is the same as that in Figure 4: (a) Totally 9 signal along with the input and filtered signals for 8 various learning factors and (b) the zoom for $\mu = 1/32$, $1/64$, $1/128$, and $1/256$, respectively.

Figure 8 shows learning curves for the DLMS32 algorithm. It is explicitly visible that the curves reach a very low expected level for learning factors $\mu > 1/512$. The learning curves for the DLMS64 algorithm are practically very similar. Differences are negligible, as we can see in Figure 7.

6. Constant versus variable step LMS algorithm

The convergence of the LMS algorithm depends on the learning factor μ. The range of learning factors μ must be in the following range: $0 \leq \mu \leq 1/\lambda_{\max}$, where $\lambda_{\max}$ is the largest eigenvalue of the auto-correlation matrix of the input signal. The convergence time is $\tau_{mse} = 1/(4\mu\lambda_n)$. It is seen that the steady-state error and convergence rate are conflicting conditions, i.e., a small step size corresponds to a small offset and slow convergence rate; a large step size generates a fast convergence rate and a large offset. In order to avoid these bottlenecks, many algorithms with Variable Step Size (VSS) LMS were proposed to set dynamically the learning factors during the process of convergence [43]. However, the VSS approach usually requires more sophisticated mathematical algorithms and their implementation in the FPGA with 200 MHz speed is a challenge, especially in cost-efficient FPGAs.

7. Resources use

Table 2 summarizes the resources used by the various algorithms and FPGAs. The DLMS32 algorithm is economical in the use of resources in comparison to the NLMS16 and the NLMS32, in particular. The DLMS32 uses more embedded multipliers located in DSP blocks, but this is an advantage, as dedicated fast multipliers significantly speed up the calculations and reduce propagation time duration.

DLMS64 variant, since it consumes a lot of resources, is to be considered for seriously RFI-contaminated regions. Even in the case of tests in the Front-End currently used with EP4CE75F29C6, the DLMS64 could not be tested for both polarization channels due to the lack of DSP blocks (64% occupancy for a single channel). Even if we resigned from the DSP

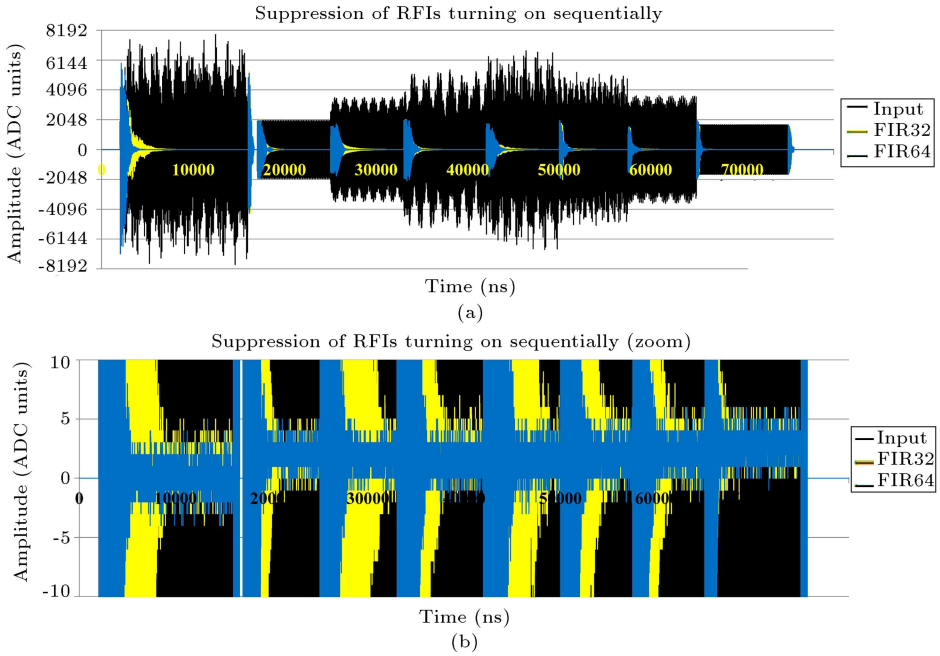


Figure 7. A timing for DLMS32/64 suppression for 5CEFA9F31I7. 4 carriers ($A_k = 2000 * \sin(\omega_k)$ turned on sequentially at $2 + 10 * k$ μs ($k = 0, 1, 2, 3$ and $\omega_0 = 41.11$ MHz, $\omega_1 = 59.37$ MHz, $\omega_2 = 71.11$ MHz, $\omega_3 = 19.0$ MHz). All mono-carriers are suppressed almost to zero. It is clearly visible that the amplitude of filtered signals is at the level of 1–2 ADC-units, while the input amplitude is at the level of $\sim$ 8000 ADC-units.

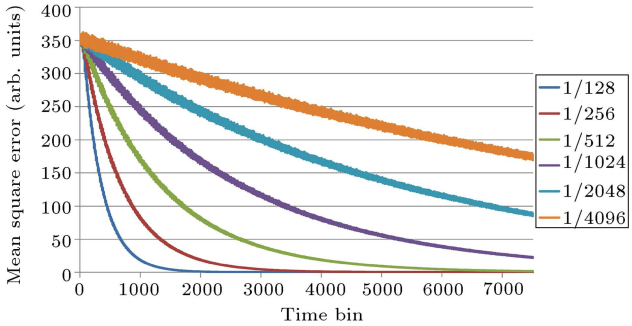


Figure 8. Learning curves for the 32-stage DLMS algorithm.

blocks, the use of logic elements is at an unacceptable level: 44% for a single channel.

8. Laboratory measurements

The DLMS32 filter was tested at the Łódź laboratory. Signals (sine waveforms or bursts) were emitted to the air by quarter-length dipoles and received by the original AERA antenna [46].

For tests, the prototype of the Front-End Board was used for the Auger surface detectors (Figure 9). The Pierre Auger Observatory has provided valuable data since 2004 using fluorescence and surface detectors for the UHECRs detection. The radio detector has been the third one developed since 2010. As the surface detector, it allows on 100% of duty while the fluorescence detector can work only during moonless nights. Its on-duty is estimated as 15%. The electronics for the surface detector designed in the 1990s became obsolete and statistically stopped working. Its replacement is impossible as some electronic components have not been produced for 15 years. The Pierre Auger Collaboration decided to upgrade the surface detector electronic which increases 3 times the sampling frequency and improves the analog resolution from 10 to 12-bits. The new surface front-end should also cooperate with the radio detectors. The prototype (Figure 9) developed for the surface and radio detectors is equipped with the largest Altera FPGA chip from the Cyclone® V family. Seven front-end boards successfully passed 9-month tests on Argentinean pampas [44,45].

The environment at the Łódź laboratory is significantly contaminated by the FM transmitters (Figure 10(a)). We must use band-reject filters in the range of 88–108 MHz to clean the signal. Figure 10(b) shows the spectrum already cleaned from FM contribution. The spectrum of test signals is shown in Figure 11. Figure 12 shows the spectra of test signals from Figure 11 after the standard IIR filter currently in use in radio stations for perfect adjustment and for slightly deflected frequencies.

If contamination frequencies do not match the optimal ones, the IIR filter is practically useless. The suppression is reduced at a factor of 30 or more.

Figure 13 shows that the suppression of the DLMS32 filter is at the same level as the IIR filter for optimal adjustment. Tests with short burst signals

Table 2. Resources utilization for various FPGAS and LMS variants.

FPGA	Variant	ALMs/LEs	Regs	DSP
5CEFA9F31I7	NLMS16	1,854/113,560 (2%)	3,642	26/342 (8%)
	NLMS32	3,097/113,560 (3%)	6,099	50/342 (15%)
	DLMS32	**1,118/113,560 (<1%)**	**2,818**	**63/342 (18%)**
	DLMS64	2,085/113,560 (2%)	4,872	127/342 (37%)
5CEFA7F31C6	DLMS32	1,126/56,480 (2%)	2822	63/156 (40%)
EP4CE75F29C6	NLMS16	6,046/75,408 (8%)	3,964	100/400 (25%)
	DLMS32	**2,999/75,408 (4%)**	**2,916**	**128/400 (32%)**
	DLMS64	6,482/75,408 (9%)	6,489	256/400 (64%)
		33,176/75,408 (44%)	16,937	0/400 (0%)
5CSXFC6D6F31C6	DLMS32	1,126/41,910 (3%)	2,802	63/112 (56%)

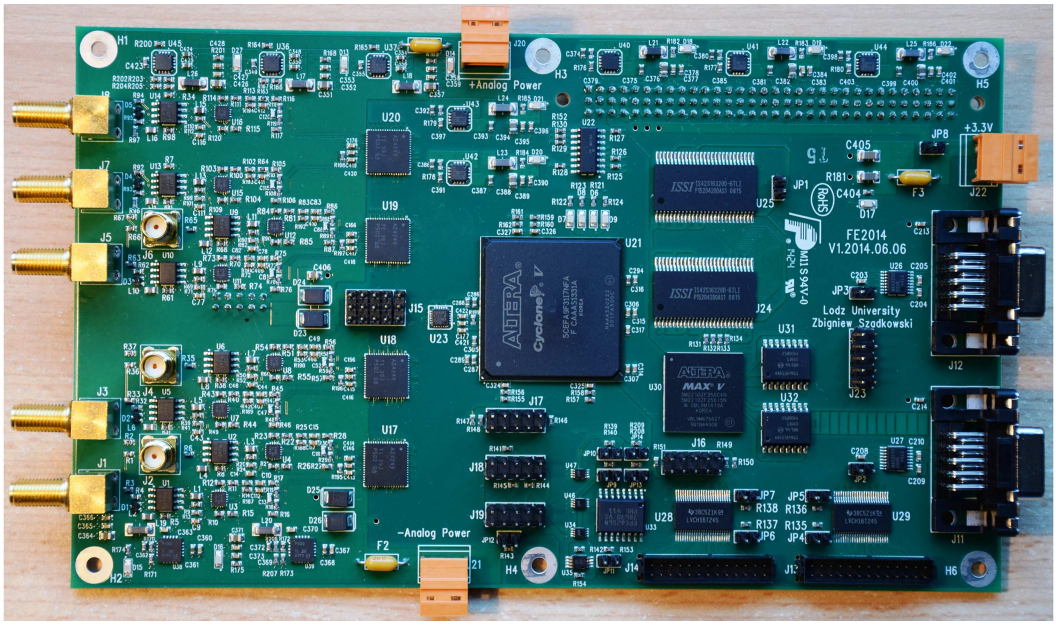
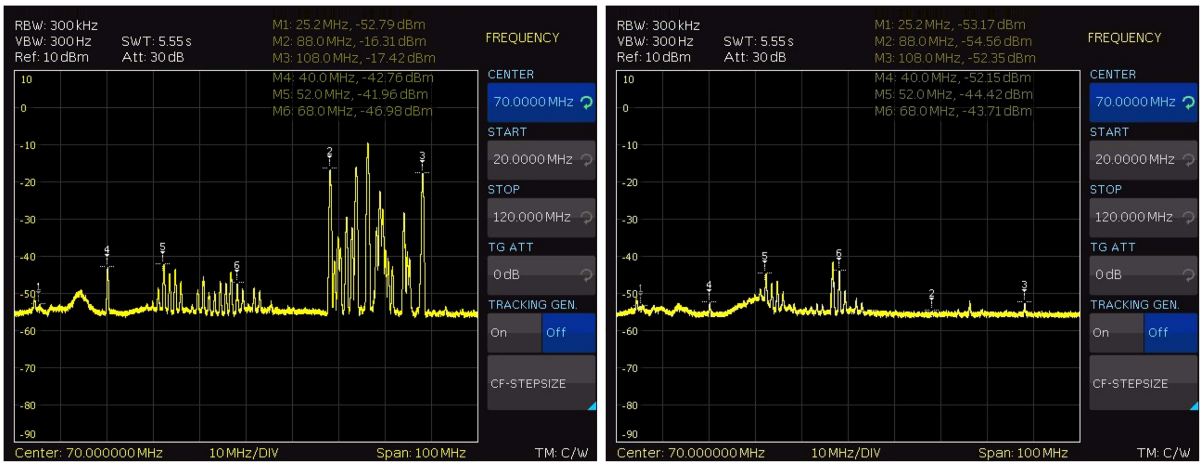


Figure 9. The prototype front-end board for the surface and radio detectors of the Pierre Auger Observatory [44,45].



(a) (b)

Figure 10. The spectrum at the Łódź laboratory without the FM (88–108 MHz) Chebyshev filter measured by the spectrum analyzer HAMEG (a) and with FM (88–108 MHz) Chebyshev filter measured by the spectrum analyzer HAMEG. The FM band has been totally removed (b).

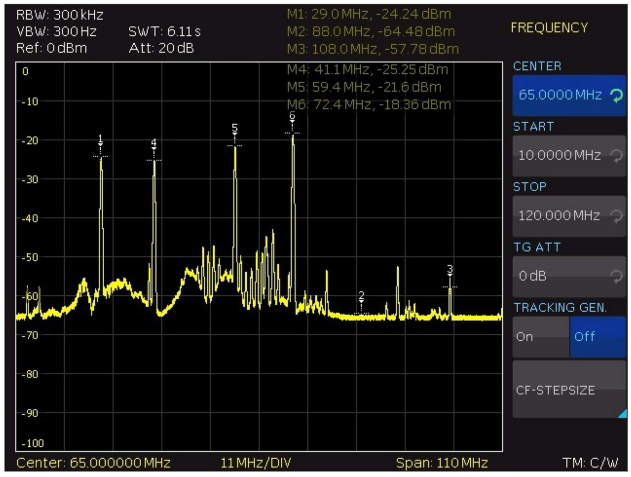


Figure 11. The spectrum of a test signal: 4 mono-carriers corresponding to IIR notch filter frequencies.

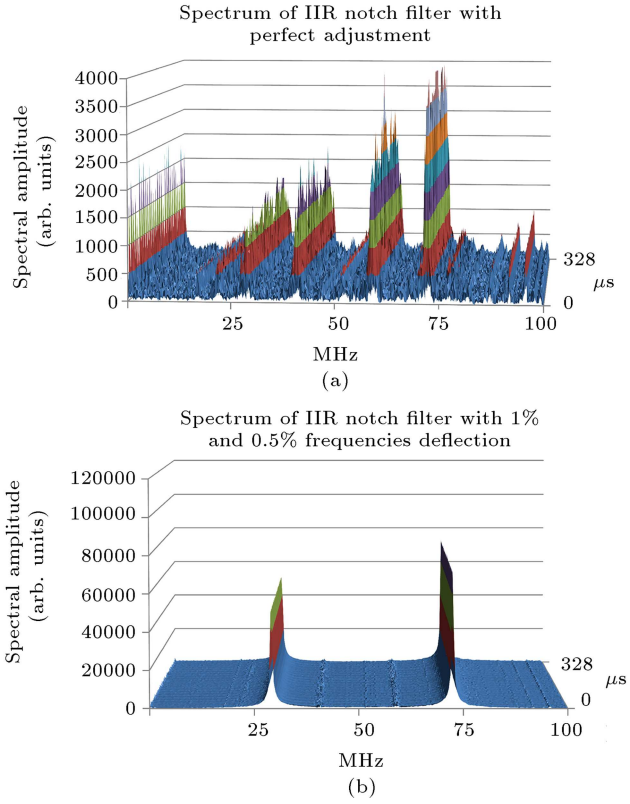


Figure 12. Spectra of the filtered signals by the IIR filter for 4 mono-carriers from Figure 11 (a) and for two slightly deflected frequencies f_2 and f_3 at 1% and 0.5%, respectively (b).

show the response speed of the filters. Figure 14 shows the spectra of original and filtered signals. For both IIR and DLMS32 filters, the spectra are similar. A response is fast enough not to cause additional distortion. In this sense, the DLMS algorithm is prepared better in case of short peak cancellation visible in measurements in Figure 5.

Figure 15 shows suppression factors for 4 mono-

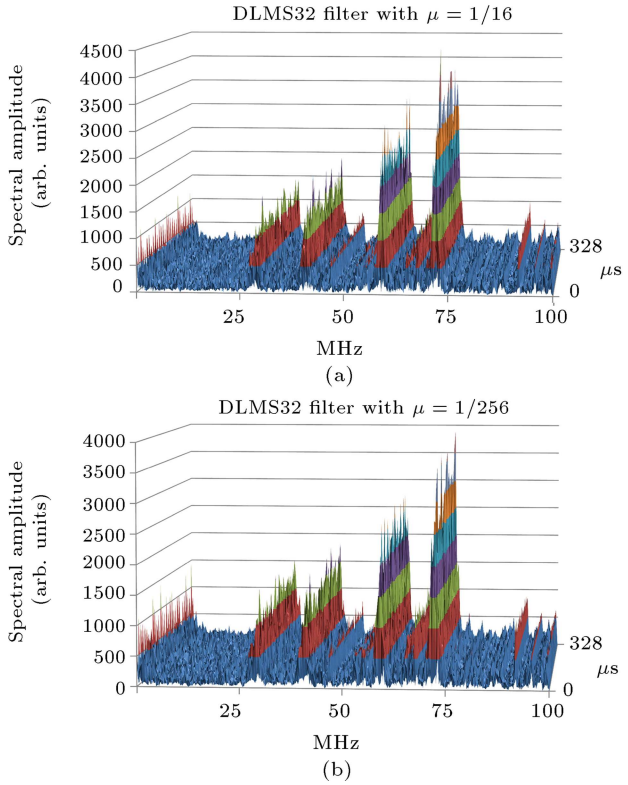


Figure 13. A spectrum of filtered signals by the DLMS32 algorithm with the learning factors $\mu = 1/16$ and $\mu = 1/256$.

carriers with frequencies perfectly tuned for the IIR filter. It is seen that the DLMS32 algorithm offers practically the same RFI suppression in a wide range of learning factors as the IIR filter. However, the DLMS32 algorithm enjoys one crucial advantage, that is, adaptivity. In the case of additional RFI sources, the nonadaptive algorithm is useless. For future challenges, we need to be ready to resolve the issue of sources that are unpredictable at present.

9. DLMS vs. LMS algorithm

Figure 2 shows a graphical representation of the DLMS/LMS algorithm. A difference between the DLMS and LMS algorithms is in X[10.0] inputs:

- With 64 time-bin delays (the DLMS algorithm);
- Without any delay (the LMS algorithm).

The entire structure of both algorithms shown in Figure 2 is the same.

In the case of comparing both algorithms, the learning curves are calculated for a particular configuration potentially appearing in the AERA experiment. Figure 16 shows learning curves calculated for 4 sine signals (spread in the frequency range shown in Figure 11). It is clearly visible that the convergence speed is faster for the DLMS algorithm.

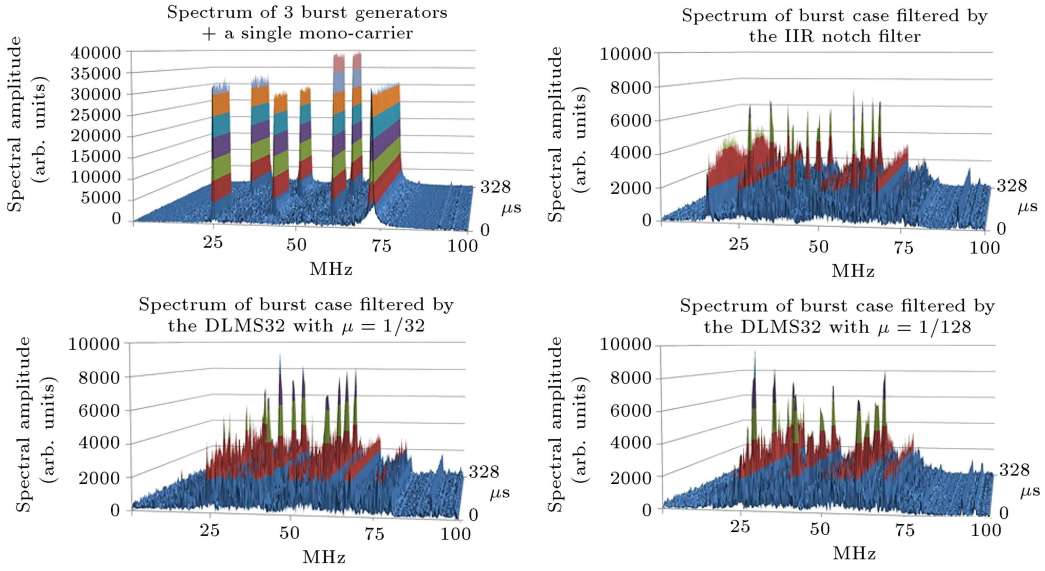


Figure 14. A spectrum of tested burst signals. For the DLMS32 filter, we observe some peaks as residua from the original signals when the filter did not obtain sufficient convergence. For the IIR filter, similar peaks are observed due to the necessity of time for the filter stabilization.

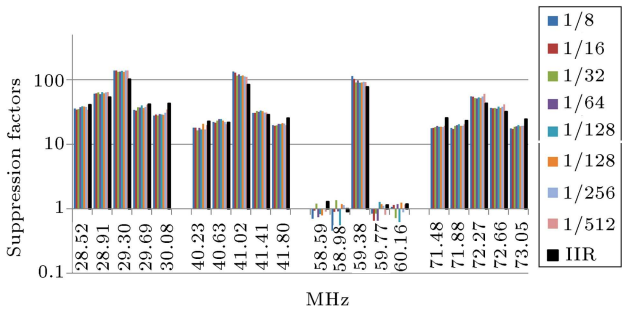


Figure 15. Suppression factors of filtered signals by the DLMS32 algorithm with the learning factors $\mu = 1/8$ till $\mu = 1/512$ for 4 mono carriers. Black columns indicate the suppression factors of the IIR filter.

10. Limitations

We checked the algorithms for mono-carriers with relatively widely separated frequencies. For "beacons" distances (e.g. 65.434, 68.364, 76.175, and 79.103 MHz), the suppression of the DLMS algorithm is very efficient (Figure 17). However, when the frequency distance is small (Figure 17(b) or 18(a)), the suppression is rather poor. Nevertheless, the DLMS32 algorithm is relatively efficient for FM-modulated signals with a relatively large deviation (75 kHz) and modulation frequency (100 kHz), which can be characteristic of FMCW radars (Figure 18(b)).

11. Conclusion

This study successfully implemented the DLMS32 algorithm on cost-efficient FPGAs from Cyclone® IV E and Cyclone® V E families with 200 MHz global clock (Figure 7). The DLMS32 algorithm was found to be much faster algorithm than the NLMS32 one. The Delay LMS (DLMS) variant offers a wider safety margin and uses less resources than the Normalized LMS (NLMS). Moreover, it is less complicated and does not require any division operation for normalizing the learning factors. In ideal conditions, the DLMS32

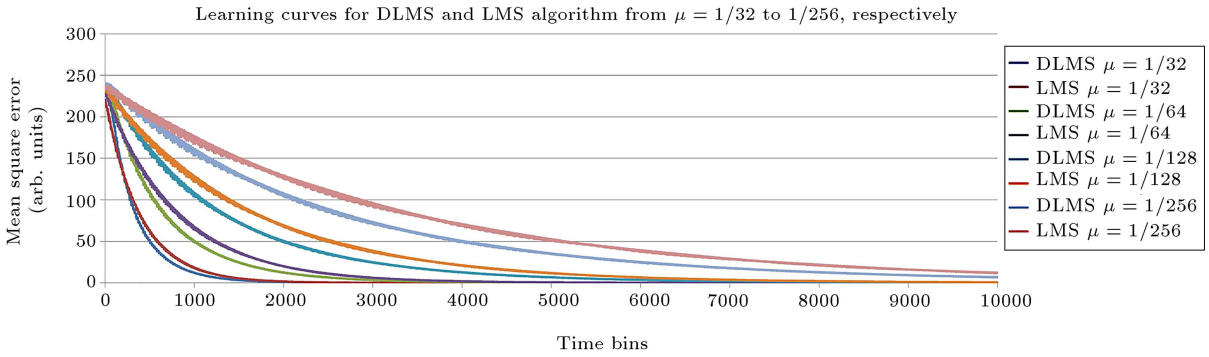


Figure 16. Learning curves for the 32-stage DLMS and LMS algorithms.

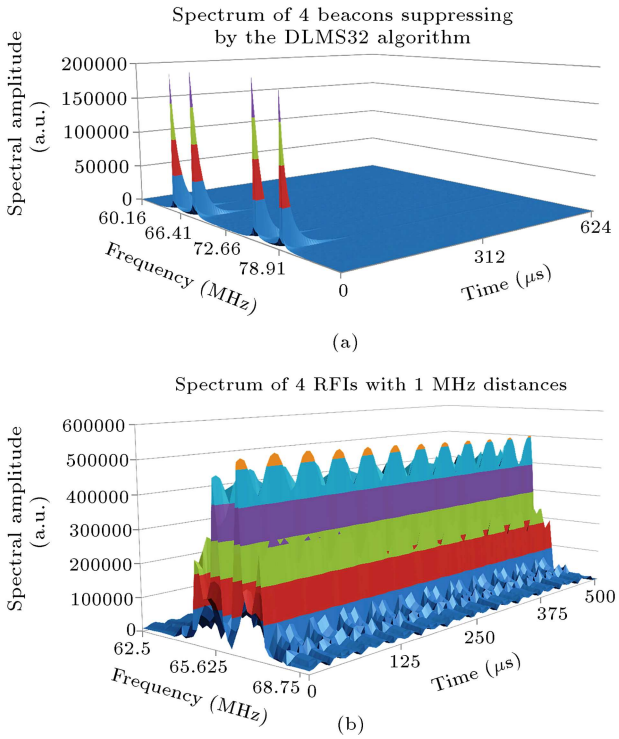


Figure 17. The spectrum of 4 AERA beacon generators suppressing by the DLMS32 algorithm (a) and the spectrum of 4 RFIs with a frequency distance of 1 MHz (b).

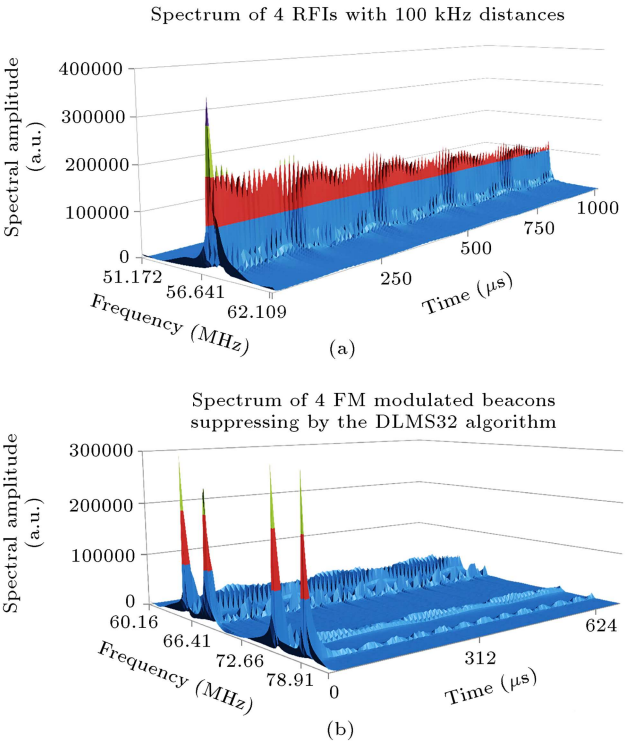


Figure 18. Spectrum of 4 RFIs generators with a frequency distance of 100 kHz suppressing by the DLMS32 algorithm (a) and the spectrum of 4 beacon frequencies FM modulated with 75 kHz and 25 kHz deviation and 100 and 10 kHz modulation frequencies (b).

suppresses the RFI totally (to zero), while the NLMS retains some fraction of contamination (see Figure 1).

The DLMS32 variant can be tested easily in the field (Malargue, Argentina) in the existing radio stations' in the same Cyclone® IV E FPGAs. Some selected learning factors offer perfect performance. However, we should remember that the simulations are performed for rather ideal conditions (without noise and temporary fluctuations). The analysis presented above is only the first step. Only pampas measurements allow for final verification and confirmation of very promising features, especially for the upgraded Front-End Boards.

Acknowledgment

This work is supported by the National Science Centre (Poland) under NCN Grant HARMONIA-8 No. 2016/22/M/ST9/00198.

References

1. Rossi, B. "Misure sulla distribuzione angolare di intensita dellaradiazione penetrante all' Asmara", *La Ricerca Scientifica Supplemento*, **1**(9–10), pp. 579–589 (1934).
2. Schmeiser, K. and Bothe, W. "Die harten ultrastrahlschauer", *Annals of Physics*, **424**, p. 161 (1938).
3. Kolhörster, W., Matthes, I., and Weber, E. "Gekoppelte Höhenstrahlen", *Naturwissenschaften*, **26**, p. 576 (1938).
4. Auger, P., Maze, R., and Robley, A.F. "Extension et pouvoir pénétrant des grandes grebes de rayons cosmiques", *Comptes Rendus*, **208**, p. 1641 (1939).
5. Auger, P., Ehrenfest, P., Maze, R., et al. "Extensive cosmic ray showers", *Reviews of Modern Physics*, **11**, pp. 288–291 (1939).
6. Pierre Auger Collaboration "The Pierre Auger cosmic ray observatory", *Nucl. Instrum. Meth.*, **A798**, pp. 172–213 (2015).
7. Allan, H.R. "Cosmic ray physics", In *Progress in Particle and Nuclear Physics*, North-Holland Publishing Company, Amsterdam, **10**, p. 169 (1971)
8. Fegan, D.J. "Detection of elusive radio and optical emission from cosmic-ray showers in the 1960s", *Nucl. Instrum. Meth.*, **A662**, pp. S2–S11 (2012).
9. Falcke, H., Apel, W.D., Badea, A.F., et al. "Detection and imaging of atmospheric radio flashes from cosmic ray air showers", *Nature (London)*, **435**, pp. 313–316 (2005).
10. Ardouin, D., Belletoile, A., Charrier, D., et al. "Radioelectric field features of extensive air showers observed with CODALEMA", *Astropart. Phys.*, **26**, pp. 341–350 (2006).

11. Fliescher, S. (Pierre Auger Collaboration), "Radio detection of cosmic ray induced air showers at the Pierre Auger observatory", *Nucl. Instrum. Meth.*, **A662**, pp. S124–S129 (2012).
12. Dallier, R. (Pierre Auger Collaboration), "Measuring cosmic ray radio signals at the Pierre Auger Observatory", *Nucl. Instrum. Meth.*, **A630**, pp. 218–221 (2011).
13. Huege, T. (Pierre Auger Collaboration), "Radio detection of cosmic rays in the Pierre Auger Observatory", *Nucl. Instrum. Meth.*, **A617**, pp. 484–487 (2010).
14. van den Berg, A.M., (Pierre Auger Collaboration), "Results from and prospects for the Auger Engineering Radio Array ", *Eur. Phys. J. Web Conf.*, **53**, p. 080060 (2013).
15. Kahn, F.D. and Lerche, I. In *Proceedings of the Royal Society of London Series A-Mathematical and Physical Sciences*, **289**, p. 206 (1966).
16. Askaryan, G.A. "Excess negative charge of an electron-photon shower and its coherent radio emission", *Sov. Phys. JETP*, **14**, pp. 441–443 (1962).
17. Werner, K., de Vries, K.D., and Scholten, O. "A realistic treatment of geomagnetic Cherenkov radiation from cosmic ray air showers", *Astropart. Phys.*, **37**, pp. 5–16 (2012).
18. James, C.W., Falcke, H., Huege, T., et al. "General description of electromagnetic radiation processes based on instantaneous charge acceleration in "endpoints"", *Phys. Rev.*, **E84**, p. 056602 (2011).
19. Szadkowski, Z. and Głas, D. "Adaptive linear predictor FIR filter based on the cyclone V FPGA with HPS to reduce narrow band RFI in radio detection of cosmic rays", *IEEE Trans. Nucl. Science*, **63**(3), pp. 1455–1462 (2016).
20. Szadkowski, Z. "Adaptive IIR-Notch filter for RFI suppression in a radio detection of cosmic rays", *IEEE Trans. Nucl. Science*, **64**(6), pp. 1292–1303 (2017).
21. Szadkowski, Z. "RFI filtering in AERA radio-detection of cosmic rays", *Progress in Electromagnetics Research Symposium - Spring (PIERS)*, St. Petersburg, Russia (May 22-25, 2017).
22. Szadkowski, Z. and Szadkowska, A. "Two-dimensional multiplier-less wavelet trigger for a radio-detection of cosmic rays", *Progress in Electromagnetics Research Symposium - Spring (PIERS)*, St. Petersburg, Russia (May 22-25, 2017).
23. Szadkowski, Z. "A hardware implementation of the Levinson routine in a radio detector of cosmic rays to improve a suppression of the nonstationary RFI", *IEEE Trans. Nucl. Science*, **64**(11), pp. 2895–2903 (2017).
24. Jafari, S., Hashemi Golpayegani, S.M.R., and Jafari, H. "A novel noise reduction method based on geometrical properties of continuous chaotic signals", *Scientia Iranica*, **19**(6), pp. 1837–1842 (2012).
25. Kelley, J.L. for Pierre Auger Collaboration "Data acquisition, triggering, and filtering at the Auger engineering radio array", *Nucl. Instrum. Meth.*, **A725**, pp. 133–136 (2013).
26. Pierre Auger Collaboration "Nano- second-level time synchronization of autonomous radio detector stations for extensive air showers", *JINST*, **11**, p. 01018 (2016).
27. Pierre Auger Collaboration "Measurement of the radiation energy in the radio signal of extensive air showers as a universal estimator of cosmic-ray energy", *Phys. Rev. Lett*, **116**(24), p. 241101 (2016).
28. Szadkowski, Z. "An optimization of the FPGA based wavelet trigger in radio detection of cosmic rays", *IEEE Trans. Nucl. Science*, **62**(3), pp. 993–1001 (2015).
29. Szadkowski, Z. and Pytel, K. "Artificial neural network as a FPGA trigger for a detection of very inclined air showers", *IEEE Trans. Nucl. Science*, **62**(3), pp. 1002–1009 (2015).
30. Nagumo, J. and Noda, A. "A learning method for system identification", *IEEE Trans. on Automatic Control*, **12**(3), p. 282 (1967).
31. Albert, A.E. and Gardner, L.S., *Stochastic Approximation and Nonlinear Regression*, MIT Press, Cambridge, MA. (1967).
32. Szadkowski, Z. and Głas, D. "The least mean squares adaptive FIR filter for narrow-band RFI suppression in radio detection of cosmic rays", *IEEE Trans. Nucl. Science*, **64**(6), pp. 1304–1315 (2017).
33. Bahoura, M. and Ezzaidi, H. "FPGA implementation of sequential adaptive noise canceller using Xilinx system generator", *Proc. Conf. on Microelectronics*, Marrakesh, pp. 213–216 (2009).
34. Papadhimitri, E., Testoni, N., and Maseti, G. "A filtering technique based on a DLMS algorithm for ultrasonography video", *1st International Symposium on Computing in Informatics and Mathematics* (ISCIM 2011).
35. Mullins, S. and Heneghan, S. "Alternative least mean square adaptive filter architectures for implementation on field programmable gate arrays", *11th European Signal Processing Conference* (2001).
36. Yi, Y., Woods, R., and Cowan, C.F.N. "High speed FPGA-based implementations of delayed-LMS filters", *The Journal of VLSI Signal Processing*, **39**, p. 113 (2005).
37. Dong, X., Li, H., and Wang, Y. "High-speed FPGA implementation of an improved LMS algorithm", *International Conference on Computational Problem-Solving (ICCP)* (2013).
38. Elhossini, A., Areibi, S., and Dony, R. "An FPGA Implementation of the LMS Adaptive Filter for Audio Processing", *2006 IEEE International Conference on Reconfigurable Computing and FPGAs (ReConFig)* (2006).

39. Nagendra, S.K. and Vinay Kumar. S.B. "Echo cancellation in audio signal using LMS algorithm", *National Conference on Recent Trends in Engineering & Technology*, Gujarat, India (2011).
40. Elamaran, V., Aswini, A., Niraimathi, V., et al. "FPGA implementation of audio enhancement using adaptive LMS filters", *Journal of Artificial Intelligence*, **5**, pp. 221–226 (2012).
41. Szadkowski, Z., Fraenkel, E.D., and van den Berg Ad, M. "FPGA/NIOS implementation of an adaptive FIR filter using linear prediction to reduce narrow-band RFI for radio detection of cosmic rays", *IEEE Trans. Nucl. Science*, **60**(5), pp. 3483–3490 (2013).
42. Szadkowski, Z., Głas D., Timmermans, C., at al. (Pierre Auger Collaboration) "First results from the FPGA/NIOS adaptive FIR filter using linear prediction implemented in the AERA radio stations to reduce narrow band RFI for radio detection of cosmic rays", *IEEE Trans. Nucl. Science*, **62**(3), pp. 977–984 (2015).
43. Shams Esfand Abadi, M., Moussavi, S.Z., and Mahlooji Far, A. "Variable, step-size, block normalized, least mean, square adaptive filter: A unified framework", *Scientia Iranica*, **15**, pp. 195–202 (2008).
44. Szadkowski, Z. "Front-end board with cyclone V as a test high-resolution platform for the Auger_Beyond_2015 front end electronics", *IEEE Trans. Nucl. Science*, **62**(3), pp. 985–1001 (2015).
45. Szadkowski, Z. "First results from high-resolution front end electronics for water Cherenkov air shower detectors equipped with cyclone V FPGA", *IEEE Trans. Nucl. Science*, **63**(3), pp. 1446–1454 (2016).
46. Pierre Auger Collaboration "Calibration of the logarithmic-periodic dipole antenna (LPDA) radio stations at the Pierre Auger Observatory using an octocopter", *JINST*, **12**, p. T10005 (2017).

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