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Research Note

A low power 10-bit flash analog-to-digital converter with divide and collate subranging conversion scheme

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Abstract. Sampling rate plays a key role in wireless applications in a very high-frequency range. Flash Analog-to-Digital Converter (ADC) outperforms slow converters in this regard, but is bulky at high resolutions. A state-of-the-art Divide and Collate (DnC) algorithm is proposed to design the flash ADC at subranging levels. The offset voltage is kept at a minimum through the comparators used for novel coarse and fine conversions, separately. The kick-back noise is also reduced using sample and hold switches at the input. The 10 bit ADC architecture is designed with 45 nm CMOS technology and analyzed in the SPECTRE environment. A minor variation in the transconductance with temperature is observed and, consequently, the offset drift with temperature is found to be 0.015 mV/°C. The design improves the Integrated Non-Linearity (INL) by 0.42 LSB and Differential Non-Linearity (DNL) by 0.3 LSB. Signal-to-Noise-and-Distortion Ratio (SNDR) and Spurious-Free-Dynamic-Range (SFDR) are 51.8 dB and 62 dB, respectively, in the frequency range at the Nyquist rate with a supply voltage of 1 V and input frequency of 500 MHz. The subranging scheme minimizes the comparator requirements, which is reflected in the 44% reduction of the power dissipation.

1. Introduction

Exponential growth in the applications of battery-operated devices like cell phones, laptops, and portable medical instruments has made power consumption and speed prominent design issues. The modules commonly used in a system on a chip process all the data within the chip. However, when the system needs to interact with the outer world, an Analog-to-Digital Converter (ADC) is used [1]. The ADC stands as a fundamental interfacing device to communicate with real-world applications. Good synchronization with the digital sub-modules is of primary consideration while operating an ADC. Therefore, high sampling rate is taken as a major architectural constraint by many designers [2,3].

Successive-Approximation-Register (SAR) ADCs [4] are characterized by several circuitries such as digital-to-analog circuits, control circuitries, and comparators. High-resolution ADCs can be implemented with lower complexity using sigma-delta ($\Sigma\Delta$) [5] counterparts, but maintaining good power efficiency is a challenging task [6]. $\Sigma\Delta$ ADCs produce an average

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output from a stream of bandlimited inputs. Mapping between the output and input thus becomes decisive and can cause conversion error. Time-interleaved, pipelined and flash ADCs are used for carrying out high-speed conversions, which provide high sampling frequency (f_s) in excess of 2 GHz [7,8]. Effective Number Of Bits (ENOB) is dependent on noise components present in a signal. The primary design strategy is to maintain ENOB of 95% for input frequencies up to ($\frac{f_s}{4}$) and better than 90% with Nyquist frequency ($\frac{f_s}{2}$). Time-interleaved ADC architecture is also used widely nowadays to make the circuit functionally faster with lower power dissipation. One major advantage of time-interleaving is its integrity with all ADC types. Time-interleaved ADC [7] can operate at high speeds; however, it imposes stringent gain-bandwidth requirements. Any synchronization mismatch between these interleaved channels would cause malfunctioning of the entire architecture. Another alternative is the usage of pipelining [8] that allows for the evaluation of Least Significant Bits (LSBs) during determination of Most Significant Bits (MSBs).

Flash converter stands as one of the most viable options for high-speed medium-resolution conversion suitable for wireless communications [8]. The number of comparators increases exponentially in the order of 2^N-1, as depicted in Figure 1. Subranging architecture can reduce the excessive number of comparators as requirement. Additional strategies such as assisted low power ADCs and partial switching are used to improve energy efficiency [9–14]. In [9], time interleaved architectures using capacitor-based Digital-to-Analog Converters (DAC) were used. A temperature non-varying subranging ADC through switching algorithm was also proposed in [10]. Both algorithmic and architectural developments were carried out in integrating flash ADCs. A reference voltage-based calibration was presented in [15], while an optimized comparator

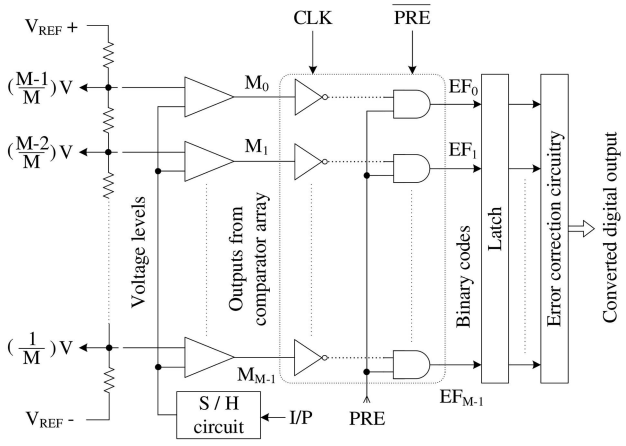


Figure 1. Flash Analog-to-Digital Converter (ADC) architecture with sing-stage coarse conversion.

offset combination to achieve the highest ENOB was proposed in [16]. An adjustment scheme was incorporated between differential and common-mode reference voltages for improving the ADC linearity. Using an excessive number of comparators in flash ADCs [17–20] with higher resolutions leads to high power requirement and space integration.

Studies have shown that all reference levels are not necessary for determining the MSBs. In the design of subranging architecture, initial levels are termed as coarse levels, while sub-divisions of the coarse levels are termed as fine levels [21–24]. A two-step time-interleaved ADC was introduced by Figueiredo et al. to reduce the number of comparators [21]. Two fine ADCs of the same size were connected after the MSB generation with a time gap of 1 phase required for settling. It reduces power dissipation to a great extent, but additional delay limits the resolution limit. An additional offset calibration scheme was employed in [22] to correct non-linearity and gain error generated by the residue amplifier used. Offset calibration eliminates the coarse ADC errors which are normally passed to the vulnerable fine ADCs. Digital subranging technique is proposed to speed up the ADC operation using the selected voltage levels generated after coarse comparisons [23]. Above 50% of total power is dissipated in Sample and Hold (S/H) and fine converters. Thus, efforts have been made to reduce the height (number of comparators per stage) of fine comparators to reduce power consumption. These design considerations certainly improve subranging architecture performance, but organizing fine comparators in terms of both height and width still remains a challenging task.

Many algorithms for sub-ranging architectures have also been defined which are broadly categorized as the binary search and frequency scaling algorithm [24]. In the binary search algorithm, input voltage level is sought after using divide and search mechanism. Another sub-ranging methodology is Dynamic Architecture and Frequency Scaling (DAFS) based algorithm. In this method, the same resolution of binary search scheme is used. Improvement of the binary searching is made to achieve a performance which is in between traditional flash and binary search. It evaluates Excess Delay (EXD) which takes both the cycle delay and reset margin into consideration. The binary search versus Bright Flash (BF) is also determined so as to cancel the EXD generated in the algorithmic-based subranging architectures [25]. Given that coarse and fine levels are basic steps in the design of subranging ADC, two different comparators for coarse and fine levels are proposed. Arrangement of coarse and fine level comparators using the algorithmic approaches is explored in this paper. Power optimization with a short additional conversion delay is targeted through the

proposition of the state-of-the-art Divide and Collate (DnC) subranging conversion algorithm.

The remainder of the paper is structured as follows: The proposed subranging level (coarse and fine) designed with different comparators (dynamic charge sharing based) is discussed in Section 2. Conversion scheme using the proposed DnC algorithm is elaborated in Section 3 with a comparison among algorithmic-based subranging architectures followed by an in-depth analysis and performance comparison for proving the efficacy of the architecture. Section 4 comprises results and discussions and Section 5 concludes the paper.

2. Design proposition of comparator for coarse and fine levels

Comparators constitute a basic portion of ADC structure as they occupy approximately 70% of the sectional area of the ADC. The offsets present in comparators often affect the non-linearity performance of ADC, namely the Integral Non-Linearity (INL) and Differential Non-Linearity (DNL). Designs of two comparators using charge-sharing-based mechanism, as shown in Figure 2, are used in this work such that changes in the offset characteristics remain minimal with PVT (Process, Voltage, and Temperature) variations. However, this increases the kick-back noise as the gain of the comparator increases to a large extent. Thus, sampling and hold switches are connected at the input terminals. At first, the coarse comparator (CCMP), described in Figure 2(b), has a large offset, but does not affect the comparison process given that the MSB bits are determined only using this comparator. Subsequently, the fine conversion comparator (FCMP) is discussed, as shown in Figure 2(a), which is necessary to keep the comparator offset to LSB/4 and therefore, a calibration step of 0.07 mV is required.

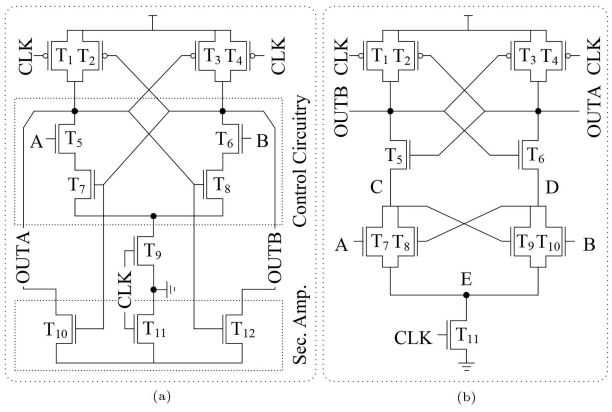


Figure 2. Proposed comparators for subranging Analog-to-Digital Converter (ADC) design: (a) Fine level comparator and (b) coarse level comparator.

Designs of many comparators were presented in [26–32] existing in the literature. The authors lucidly propose designs with low power, but with an excessive delay that affects the circuits' functionality of working at low voltage. A single tail transistor [29] allows the passage of current through both the differential pairs and the latch pairs which draw a large amount of current through a single gate transistor, thereby requiring a large gate area.

Another attempt to nullify the effect of a single transistor carrying both the current through the latch and differential stage is the usage of double tail comparator [30], but in the presence of an inverted clock. However, at any stage, if the driven clock and the driving clock have a mismatch in timing, there will be a delay in the regeneration of the process and the circuit will malfunction in that scenario. Reference voltages necessary for comparison purposes are generated using a resistor-based array as they are subject to the slightest variation with respect to temperature rather than the reference voltage generation using the offset variation of comparators, whereby there are large variations with temperature.

2.1. Subranging comparator design

To increase the latch regeneration speed, Babayan-Mashhadi and Lotfi [32] proposed a design that uses a charge-sharing mechanism wherein the node immediately discharges onto ground instead of creeping in through an inverter stage, but in the presence of an inverted clock. However, this design is subject to a major drawback of clock slew.

In case there is no proper synchronization between the driven and driving clocks, there will be a delay in the precharge phase and regeneration process malfunction in this scenario. Two charge-sharing-based comparators are used in the entire process. The comparators used for designing the subranging ADC are depicted in Figure 2. LSBs [28] for the conversion are determined from the comparator design portrayed in Figure 2(a) due to their wide applicability in the subranging structure compared to the number of CCMPs. The operation of the used charge-sharing circuits of higher resolution, depicted in Figure 2(a), involves two phases: precharge and evaluation. The functionality of this process is laid out below:

1. *Precharge phase*: During this phase, CLK is in reset state; the transistors T_1 and T_4 are pulled up to V_{DD};
2. *Evaluation phase*: This phase starts the mark of the evaluation phase with CLK value "1". At the evaluation phase, the applied voltage goes to the input transistors, namely T_5 and T_6 in Figure 2(a). Depending on the applied voltage input, the transistors T_5 and T_6 discharge. When the path gets

discharged, the voltage is sufficient to turn on the transistors T_{10} and T_{12} and the nodes OUTA and OUTB get immediately charged to V_{DD}.

Subsequently, for coarse level comparisons, an energy-efficient back-feeding based comparator is presented in Figure 2(b). The precharge phase is similar to the previous comparator with the exception of the decoupling of evaluation transistors T_7 and T_{10}. During the evaluation phase, the nodes OUTA or OUTB discharge depending on the rate of input voltage applied to the sensing input transistors, T_7 and T_{10}, respectively. The charge difference between back feed nodes C and D does not contribute to the operation speed of the evaluation process. A delay in the circuitry function is reduced by adding a back feeding discharge circuitry formed by C-T_9-E or D-T_8-E, which provides an immediate bypass for the discharge path. The T_7-T_8 paves a low-resistant path to the tail current during the evaluation phase. This mechanism of back feed nodes discharging enhances the regeneration and amplification process by minimizing the element of parasite in the transistor. Unlike the conventional latch storage where T_2-T_5 and T_3-T_6 inverters carry the evaluation result, output nodes (OUTA and OUTB) hold the result through strong pass transistors T_2-T_6 and T_3-T_5.

However, when a voltage difference of less than 0.01 mV is applied between the input nodes A and B, the difference between output nodes OUTA and OUTB is not sufficient enough to latch on to the value in Figure 2(b); therefore, the circuit in Figure 2(a) is used. The secondary amplifier comes into effect and the value then immediately turns on either of the transistors T_{10} and T_{12}, thereby providing an immediate path for discharge. This process improves the regeneration time as the control circuitry comprises a charge-sharing circuitry with transistors T_1-T_4. As soon as the charge-sharing circuit turns on, the value is latched on to the supply voltage. This makes the process faster as the charging and discharging time duration becomes shorter.

2.2. Analysis of subranging level comparators

Current through the input transistors is pulled down due to the presence of the extra circuitry, thereby a low-resistant path through the input is formed that results in the high gain of the comparators, hence yielding high kick-back noise. The modeled comparators maintain a constant current to transconductance ratio $\frac{I_{d5}}{g_{m5}}$ (fine conversion comparator) and $\frac{I_{d7}}{g_{m7}}$ (CCMPs) with variation in temperature, as depicted in results, and is discussed later. The mismatch between a comparator and input offset voltage may cause conversion errors. The conversion error results from the inability to make a difference in comparator input resolution. The error can be in any limits for any design. However, certain tolerance level can be neglected. The design here uses a tolerance limit of 0.5 LSB to −0.5 LSB.

The non-linearity performance is a prime metric in the design of ADC and it affects the performance of ADC. The problem degrades if the comparator offset is not removed. Therefore, several attempts are made to eliminate the offset based on the design topology. The input referred offset voltage before calibration [33] is given by:

$$V_{os} = \delta V_{5,6} - \frac{I_{d5}}{g_{m5}} \left(\delta \frac{\beta M_{5,6}}{\beta M_5} \right), \tag{1}$$

where $\delta V_{5,6}$ and $\beta M_{5,6}$ are the threshold and current mismatches, respectively, in the differential pair transistors T_5 and T_6. The transistors T_7 and T_8 are in the strong inversion region. As a result, the ratio is determined as $\frac{I_{d7}}{g_{m7}}$ in [33] as follows:

$$\frac{I_{D7}}{g_{m7}} = \frac{V_{gs7} - V_{T7}}{2}. \tag{2}$$

The threshold voltage is independent of temperature because the body effect is completely eliminated as the source and substrate are connected together. The transistors T_5 and T_6 are in weak inversion during the regeneration phase. Since the transistor T_5 is in weak inversion, the current through T_5 is given by:

$$I_{d5} = \frac{W_5}{L_5} I_t e^{\frac{(V_{GS5}) - V_{T5}}{\frac{nk_t}{q}}}. \tag{3}$$

k_t and q are the Boltzmann constant and the elementary charge, respectively. Therefore, we have:

$$V_{GS5} = V_{T5} + \frac{nk_T}{q} \ln \frac{\frac{I_{d5}}{I_t}}{\frac{W_5}{L_5}}. \tag{4}$$

3. Proposed DnC conversion algorithm

Flash ADCs are widely used for high-speed conversion, although they do represent a viable option in terms of power. As discussed earlier, the traditional binary search conversion scheme performs with substandard EXD which is almost non-feasible at a higher sampling frequency. This scheme was later explored by Yoshioka et al. [25] to reduce the EXD. Subranging ADCs are subject to a major limitation attached to the requirement of higher fine levels. The conversion delay is given as follows:

$$t_{FL} = 2t - comp\ delay. \tag{5}$$

Therefore, improvement of the conversion algorithm plays a pivotal role in reducing the architecture latency. A DnC conversion scheme is proposed to reduce EXD and achieve a low level comparator requirement compared to traditional flash ADCs. All the comparators

$(2^N - 1)$ are activated at an instant in a flash ADC (e.g., 15 comparators are activated in the first cycle of a 4 bit flash ADC). The conversion process goes through several operating cycles. The power in flash ADC is given by:

$$P_{FL} = (2^N - 1)P_{comp}. \tag{6}$$

The energy per conversion for flash ADC is significant as more comparators are used for the conversion stage.

3.1. Binary search algorithm

The discussion begins with the binary search algorithm followed by the improved dynamic architecture. Thereafter, the proposed DnC is introduced and compared with respect to EXD and conversion energy. The schematic of the binary search algorithm is shown in Figure 3. In binary conversion, all the comparators are connected in a divide (voltage levels) and search (selection) mechanism. A sampled signal is denoted by V_{IN} which goes through a decisive circuit that activates the mid-level voltage to select the upper or lower set of reference voltages. In this way, the conversion is carried out in multiple cycles unless the LSB is determined. A 4 bit flash architecture is given in Figure 3 wherein an input voltage of 630 mV is selected at the clock sampling instant with the resistive reference ladder voltage difference of 1 V ($V_{REF}+ = 1$, $V_{REF}- = 0$).

Each level has a voltage of 62.5 mV. Therefore, V_{IN} of 630 mV will activate the set of decisive circuits highlighted in Figure 3 ($\frac{8}{16}$, $\frac{12}{16}$, $\frac{10}{16}$, and $\frac{9}{16}$), resulting in encoded digital output of '1010'. This means that not all the comparators are selected within one cycle of comparison; hence, flash conversion is optimized. The Figure-of-Merit (FoM) is given by:

$$FoM = \frac{P_{FL}}{f_s \times 2^{ENOB}} \; per \; cycle, \tag{7}$$

where f_s is the sampling rate.

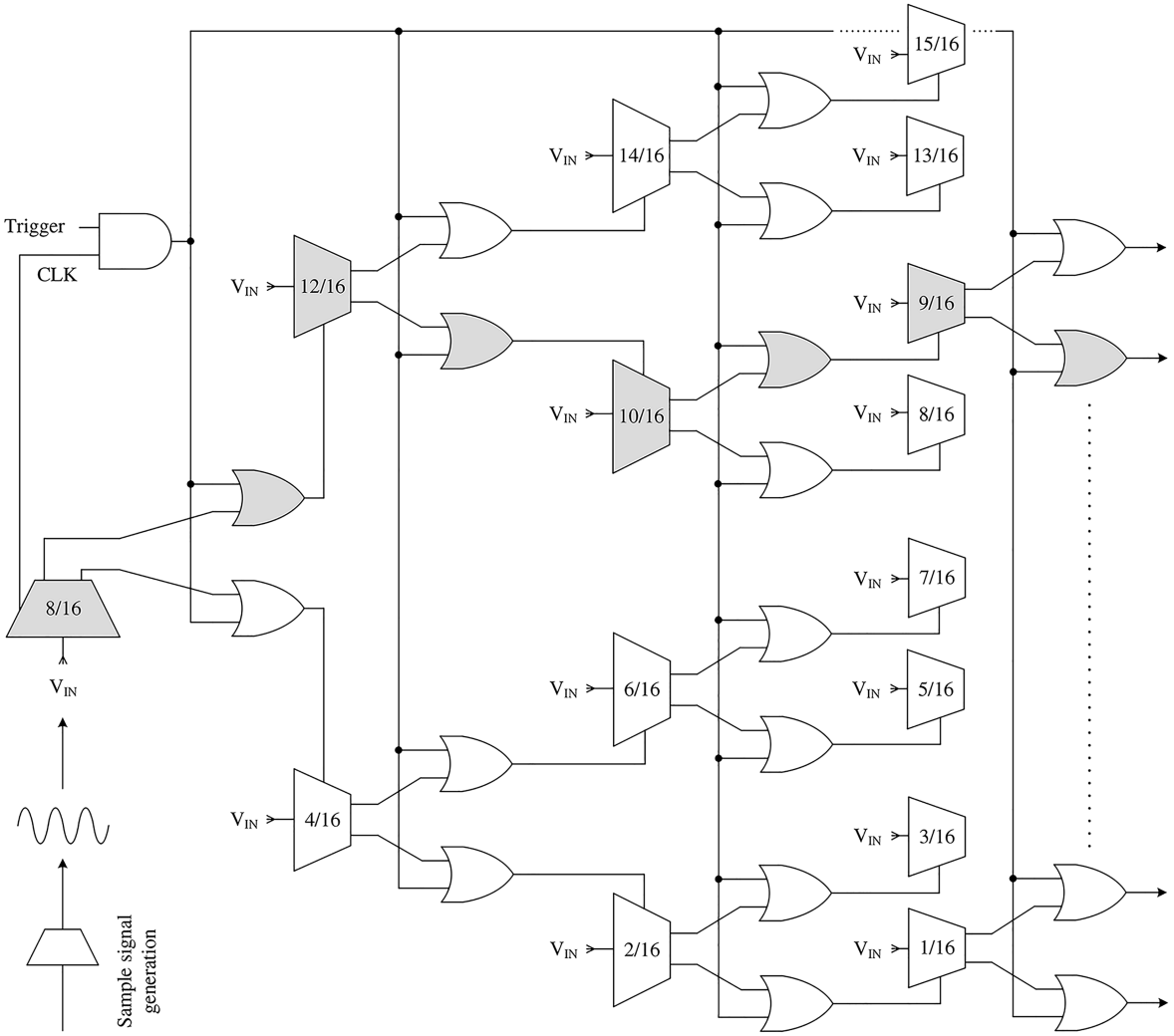


Figure 3. Binary search-based flash A/D converter: (a 4-bit flash architecture is designed with decision circuits composed of comparators and selectors).

Thus, the FoM using this scheme is lower than the flash-type, yet with a higher conversion delay.

3.2. DnC conversion scheme

Despite the higher sampling rate, flash ADCs irrespective of the subranging scheme suffer from two major performance issues:

1. Higher energy per conversion stage;
2. Requirement of excessive number of comparators at higher resolutions.

The attempt to combat the trade-off between power and delay discussed in the previous section is directed towards the development of DnC conversion algorithm. The proposed subranging 10 bit flash-ADC is shown in Figure 4 and it comprises a set of reference voltages, an array of comparators, and multiplexers. The concept of subranging stems from the identification of a set of reference voltages around the sampled input for the next step of fine mode conversion. The two intermediate fine mode reference voltages are determined using a selector (MUX), which is controlled by the preceding coarse/fine mode output. The presence of fan-out of the MUX thereby increases, creating large capacitance at the output that limits the speed of optimization. This issue can be minimized by placing a moderate number of comparators (8 or 4 as elaborated later) to provide the best energy delay trade-off. These levels have been chosen after analyzing other subranging schemes [34–37] that provide limits per stage conversion/switching to maintain a good power-delay trade-off. In the proposed architecture, the concepts of voltage divisions and distribution are used. A set of resistors is well equally spaced with the nodes carrying voltages. However, the voltage is not given to the comparator directly, but is rather distributed to each comparator in a novel way through the DnC conversion shown in Algorithm 1.

The algorithm is elaborated for a 10 bit ADC. The scheme goes through one level of coarse conversion and multiple levels of fine conversions. A 10 bit ADC has 1024 conversion levels in number, out of which 8 coarse comparisons are performed at the first stage. Then, the fine conversion starts with at most 8 levels at each stage. The minimum number of comparisons is limited to 4 for avoiding large loading at the previous stage. It may be noted that only 2×1 MUX for most levels and 4×1 MUX for final and/or pre-final stages are used irrespective of the ADC resolution. Therefore, the distribution was measured to be $8 \times 8 \times 4 \times 4$ for this design. Hence, a 48 $\times$ reduction was achieved with only 3 more conversion stages. The comparator regeneration time plays a significant role in deciding on the ADC performance in the subranging scheme due to more existing stages. Use of a modified inverter-based comparator to reduce the power and area was demonstrated, compared to the op-amp based comparators. A secondary amplifier was introduced for the proposed comparator to be performed within a short regeneration time, as shown in Figure 2(a). The design worked well with a small input voltage difference, but at a cost of extra power. The coarse comparison is common at all ADC resolutions. Therefore, for power optimization, an energy efficient dynamic comparator was used for higher input voltage comparison.

1: Resolution = N;
2: Coarse comparator = A;
3: Fine comparators = B_1, B_2;
4: Assign A, S, B_1= 8;
5: Assign B_2 = 4;
6: Assign C_1 = 1;
7: Assign C_2 = 0;
8: **Ensure**: $M = 2^N$
9: **while** $A \times S < M$ **do**
10: $S = S \times 8$;
11: $C_1 = C_1 + 1$;
12: **end while**
13: **if** $A \times S = M$ **then**
14: Assign stages = [A] [C_1 times B_1];
15: end of conversion (*exit*);
16: **end if**
17: Assign T = S;
18: **while** $A \times T > M$ **do**
19: $T = T / 2$;
20: $C_2 = C_2 + 1$;
21: **end while**
22: Assign stages = [A] [(C_1-C_2) times B_1] [C_2 times B_2];
23: end of conversion (*exit*);

Algorithm. Divide and collate subranging conversion scheme.

4. Results and discussions

A subranging ADC was designed with the proposed DnC algorithm. Furthermore, the ADC was structured with two proposed comparators separately for both the coarse and fine levels. Performance analysis of the proposed comparators exhibited robustness over environment variations and mismatches. A faster fine comparator was selected to reduce the architecture latency as it is responsible for LSB determination. The proposed DnC conversion scheme improved the FoM at low additional EXD. It required a smaller number of fine conversion stages and facilitated an optimized comparator array distribution to provide the best power delay trade-off.

4.1. Performance analysis of subranging level comparators

The comparators used for conversion were designed using the Generic Process Design Kit (GPDK) 45 nm technology. The referred designs [29–32] were rescaled using 45 nm design technology and their performances were compared in the same environment as a feasible platform was found that worked well in terms of power,

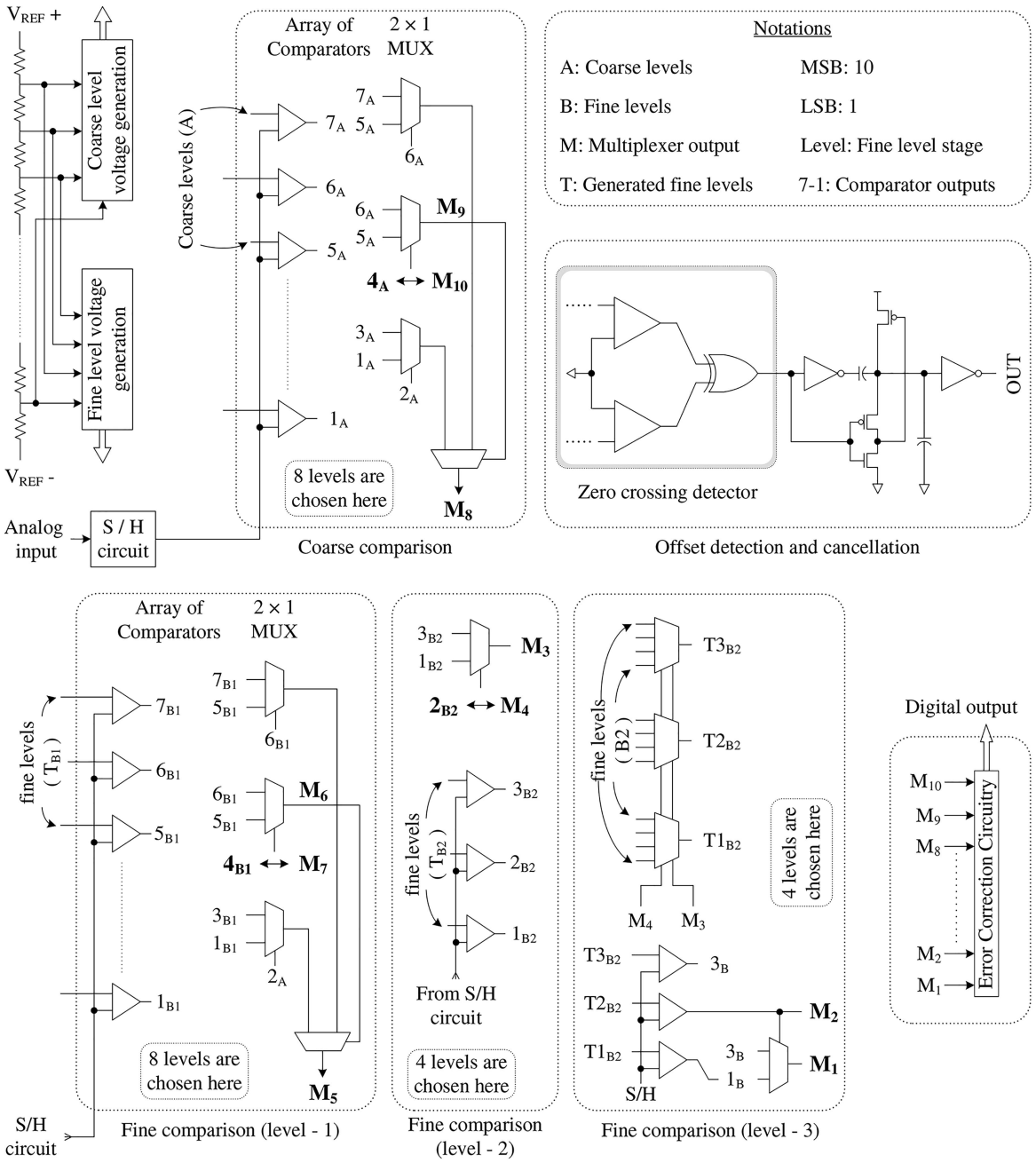


Figure 4. The proposed 10-bit subranging Analog-to-Digital Converter (ADC) design with divide and collate conversion scheme.

delay, and subtle kick-back noise parameters. Table 1 depicts the discussed comparators.

The maximum operating frequency of the proposed comparator (Figure 2(a)) is higher than that [29–32] shown in Table 1. The regeneration speed affects the output settling time; the lower value of the proposed comparators thereby improves the operating frequency. The number of transistors, power consumption, and energy consumption is less than those in [30–32], while being more than the former in [29]. The kick-back noise is higher than that found in [29–32]; however, it is managed and reduced with the sampling switch connected. The kick-back noise is high without the sampling switch (worst case) and is around 0.84 mV; it is reduced to 0.12 mV after using the sampling switch (best case) as it isolates the regeneration nodes during the evaluation phase of the comparison for the FCMP. However, the kick-back noise remains quantitatively high for the best case with 0.07 mV and 0.91 mV in the worst case, respectively. The process corner variation performance for the two proposed comparators is noted in Table 2.

Table 1. Performance comparison summary with referred comparators.

Parameter	[29]	[30]	[31]	[32]	FCMP	CCMP
Max. freq. (MHz)	900	1000	2000	2500	2500	2500
Delay (ps./dec)	54	24	110	27	16	21
Power (nW)	27	2061	4060	317	68	27
Supply vol. (V)	1	1	1.2	1	0.5	0.6
Energy/ conv. (fJ/conv)	3.03	17.07	19.07	38	5.8	4.13
No. of trans.	9	14	15	14	12	11
Kick-back noise (worst-case(mV)) ($\delta V_{in} = 0.1$ mV)	0.78	0.4	0.3	0.72	0.84	0.91
Kick-back noise (best-case(mV)) ($\delta V_{in} = 10$ mV)	0.64	0.23	0.3	0.43	0.12	0.07

Table 2. Energy-delay analysis of subranging comparators under process variation.

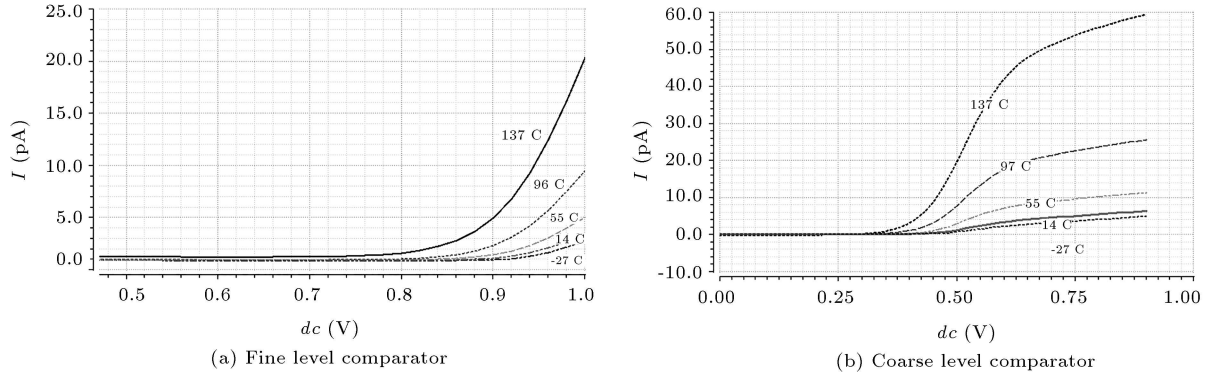
Comparator	Parameter	SS	SF	FS	FF
Coarse level	Energy (fJ/convstep)	0.065	0.079	0.078	0.087
	Delay (ps)	16.6	16.9	6.3	4.9
Fine level	Energy (fJ/convstep)	0.077	0.099	0.098	0.107
	Delay (ps)	16	15.4	6.7	5

The design is moderately sensitive to delay with a mean deviation of 38% in the conversion of both coarse and fine level comparators and is the least sensitive to energy dissipation with variations of 14.5% and 21.7% respectively.

Table 3 presents a description of various state-of-the-art ADCs. The sampling frequency was seen to be higher than that for other architectures. The design could also function at a low supply voltage of 0.5 V. The FoM was seen to be the best amongst all the compared architectures. Figure 5(a) and (b) show the temperature dependence of offset voltage with varying temperatures. It shows that the offset does not drift much with respect to temperature. The ratio of current to transconductance is almost constant. I_{d5} is generated by the band gap and the temperature coefficient where the comparators are calibrated at 27°C. The diffusion capacitance of the transistor, therefore, minimizes the operating frequency. Figure 5(a) shows the change of I_{d5} with temperature changes. Putting this value in Eq. (1), the temperature dependence was found to be very small 0.015 mV/°C and could be neglected. Thus, the addition of the secondary amplifier circuitry changes $\frac{I_{d5}}{g_{m5}}$ slightly and does not depend on temperature. However, the second-order effects at high temperatures affect the offset of the comparator which in turn effects the ADC performance. Thus, offset voltage is reduced at high temperatures.

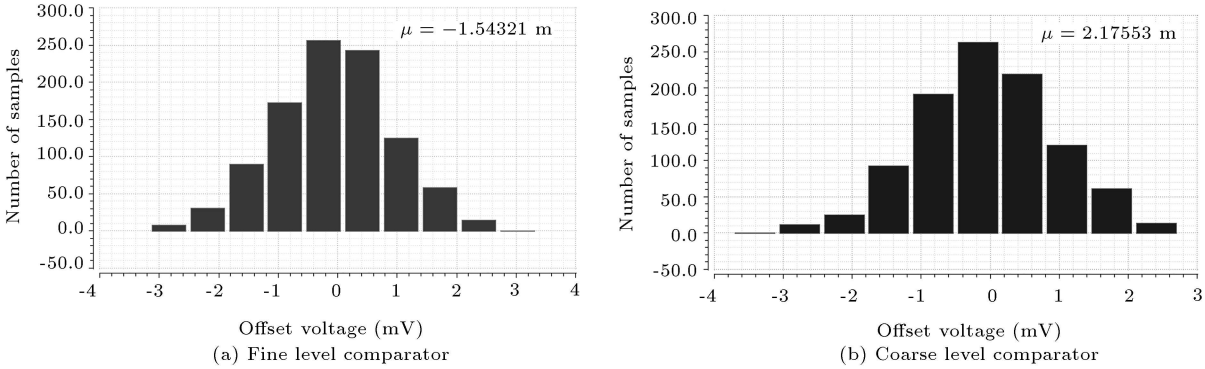
Table 3. Comparison with state of art.

Feature	[1]	[8]	[21]	[22]	[23]	[20]	[25]	Proposed
Technology	90-nm	28-nm	90-nm	90-nm	55-nm	65-nm	65-nm	45-nm
Resolution	10	11	6	10	8	8	7	10
Sampling freq. (GS/s)	0.1	0.02	1	0.1	1	1.5	1.22	2.5
Min. supply voltage (V)	1.2	1.8	1.2	1	1.2	1	1	0.5
Input range (mV)	1600	280	—	2	800	—	—	300
INL (LSB)	0.95	1.2	—	0.9/–0.9	-1.2/1.2	0.5/–0.5	—	0.25/–0.3
DNL (LSB)	0.83	0.7	—	0.6/–0.5	–0.8/0.8	0.28/–0.25	—	0.28/–0.21
SNDR (dB)	56.4	61.8	33.8	58	43.5	38	36.2	51.8
SFDR (dB)	—	—	—	75	55	47	—	62
Power (mW)	68.3	2.24	55	6	16	35	8.11	10.5
FoM (pJ/conv)	—	0.111	—	0.092	0.125	0.42	0.125	0.014
ENOB (Bits)	9.08	—	5.3	9.34	7	6	—	8.3



(a) Fine level comparator (b) Coarse level comparator

Figure 5. Decision transistor current performance variation over temperature.



(a) Fine level comparator (b) Coarse level comparator

Figure 6. Comparator offset variation over 1000 runs of Monte Carlo sampling method.

Figure 5(b) shows the temperature dependence on the bias point of transistor T_5. Current I_{d5} is slightly dependent on temperature at low temperatures. The offset voltage is seen to be high at lower temperatures while being low at high temperatures with a secondary amplifier. Second-order channel effects appear at high temperatures. It comprises the channel length modulation effect and the buffer size. In this work, the temperature dependence for the proposed comparator and conventional comparator is shown.

The comparator design such that the offset is zero for a common mode voltage below 100 mV. To improve the calibration accuracy, the voltage converter is added that acts like a buffer. Voltage is transferred to the input and the capacitor builds up the voltage and then, sends it to the capacitor. The capacitor charges and sends it to the drain of the N-channel Metal Oxide Semiconductor (NMOS). The voltage is either low or high at this point. Now, this voltage is applied to the transistor ends [29]. For example, when the common mode voltage is 100 mV, the output of the comparator is 10 mV. The multiplexer input will take this voltage to be high and yield a high output. Then, as soon as the output from the inverter goes high or low, the NMOS turns on and the voltage from the buffer gets transmitted to the output. This will yield a low output. Thus, the introduction of the down voltage converter improves the non-linearity performance by 0.42 LSB. However, the addition of this converter increases the overall power consumption by 10%. The DNL deviation was found to be 0.28 LSB. The standard deviation of the input-referred offset noise is less than 0.24 LSB, but the error is around 3.5 LSBs from Monte Carlo simulation results, as shown in Figure 6. Few designs are used in which the differential and latch stages are separated from each other [24–26]. This separation introduces less delay and the circuit can function better with an offset variation of 0.52 LSBs [26], but at the cost of high power dissipation.

The Monte Carlo simulation in Figure 6(a) shows the mean offset deviation of 3.5 LSBs for fine comparator and 5.6 LSBs for CCMPs with 1000 trials, as shown in Figure 6(b).

EXD for subranging ADC is illustrated in Figure 7 which can be defined as follows:

$$EXD = \text{Reset margin} + \text{conversion delay}. \tag{8}$$

The scheme works fine for an ADC even at a higher resolution, provided that the comparative delay is within an acceptable limit since EXD is proportional to it and ultimately affects the sampling rate. The EXD is greatly suppressed due to the faster discharge rate of comparators. The EXD primarily results from the searching of fine voltage levels. ADC conversion consists of S/H circuit, coarse conversion, and fine conversion steps. The operation is assigned to a 4 bit

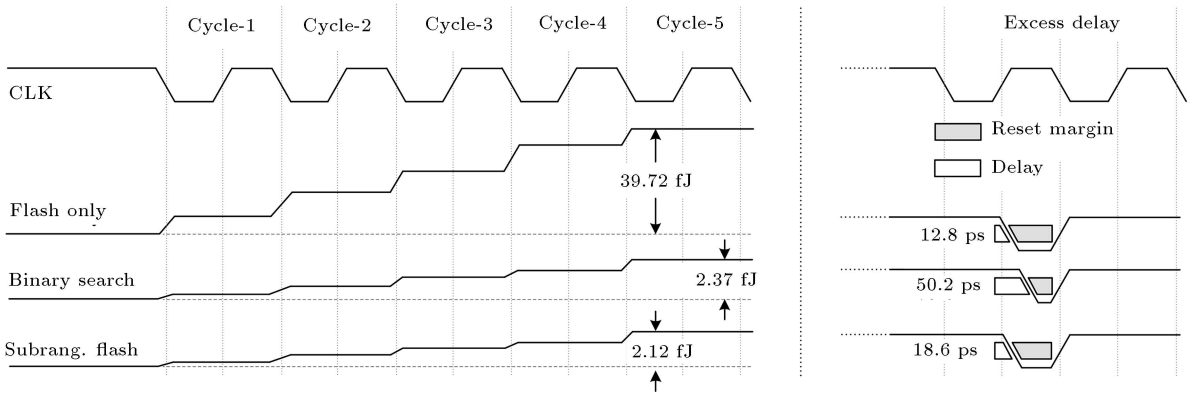


Figure 7. Energy-delay performance of various A/D conversion algorithms.

ADC. Each cycle consists of three phases (P): S/H, coarse, and fine stages. The sampling switch is closed and the applied input signal is sampled to capacitance and the switch opens at the beginning of the cycle $P[N]$. At the next phase of operation, $P[N+1]$, MSB is determined using coarse conversion. The remaining bits are evaluated in the subsequent fine conversion. The cycle $P[N+2]$ determines the next two fine modes of bits and, in this way, the process goes on [32–37].

Since the output is greatly dependent on the number of voltage levels, flash operation continues for another cycle when the conversion at the phase $P[N+2]$ is prolonged. Flash ADC converts fully at the coarse level ($P[N+1]$ phase) which allows it to cancel the EXD for the other subsequent stages. A higher reset margin is, however, set to be synchronized with the sampling frequency. Timing diagram (Figure 7) presents energy per conversion step over various operational cycles in EXD of different flash architectures. Number of subranging stages is estimated as follows:

Subranging stages (Flash)

$$= \frac{\text{Number of Flash conversions } (M)}{\text{Number of searches}} \left[\frac{\mathbf{16}}{\mathbf{16}} = \mathbf{1}\right], \quad (9)$$

Subranging stages (Binary)

$$= \frac{\text{Number of Flash conversions } (M)}{\log_2\left(\frac{M}{2}\right) + 1}$$

$$\left[\frac{\mathbf{16}}{\mathbf{3+1}} = \mathbf{4}\right], \quad (10)$$

Subranging stages (Prop. subranging)

$$= \log_2 M - Y (Y \text{ is calculated from DnC algorithm})$$

$$[\mathbf{4 - 2 = 2}]. \quad (11)$$

Eqs. (9)–(11) show the stage requirements (coarse + fine) of the compared flash architectures. As a design demonstration, 4 bit flash ADCs are discussed and the performances are summarized in Figure 7. The larger number of fine levels using binary search scheme degrades the conversion speed, which may dither the conversion at a higher sampling frequency. Subranging flash, on the other hand, has two stages and can perform with the low EXD of 5.8 ps. Faster flash ADC dissipates higher cycle energy (FoM of 39.72 fJ in just 5 cycles) which makes it less efficient for higher resolution converters. The proposed subranging flash ADC provides the best energy-delay trade-off at medium-to-high resolutions.

The ADC converts a 500 MHz input signal at a sampling rate of 2.5 GS/s with a power supply of 1 V. A resistor-based reference ladder, depicted in Figure 4, is used due to its stability despite temperature mismatches in the input range of 300 mV. There are 8 coarse levels which indicates the levels as 7A, 6A,...,1A as others will be the same. Since the DnC scheme assigns three fine comparison stages, 8-4-4 number of comparators are used at levels 1, 2, and 3, respectively. During the test cycle, input was at 75.5 mV at the beginning of evaluation phase (CLK = 1). Thus, the lower voltage limits were selected to be 75 mV (level 1), 77.34375 mV (level 2), and 75.5859 mV (level 3). In addition, 290 μV was assigned to 1 LSB representation.

The behavioral characteristics of the compared designs were tested at various process corners, as depicted in Figure 8. The flash ADC has the highest power dissipation over all corners. The consumed power is the least for all flash and binary search-based ADC at the slowest (SS) process corner. The consumed power is greater than binary search for the proposed design, but lower than the flash-based ADC. However, owing to the higher EXD that contributes to the overall delay in the binary search scheme, the resolution must be limited to the moderate range. Figure 9 depicts the average power variation with variations of frequency and supply voltage. The average power increases by 2.36 mW/GHz over the 2.5 GHz bandwidth. The average power increment over the supply voltage variation

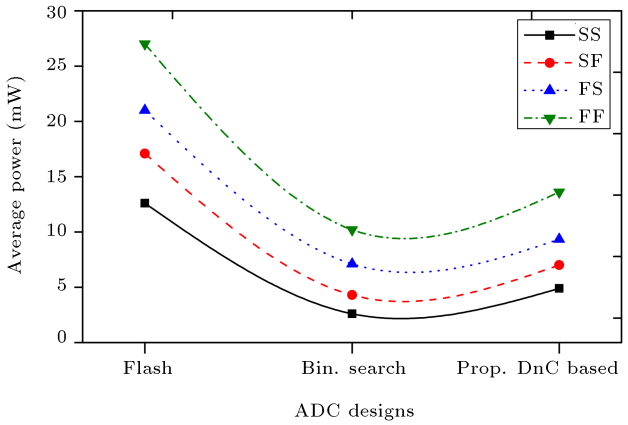


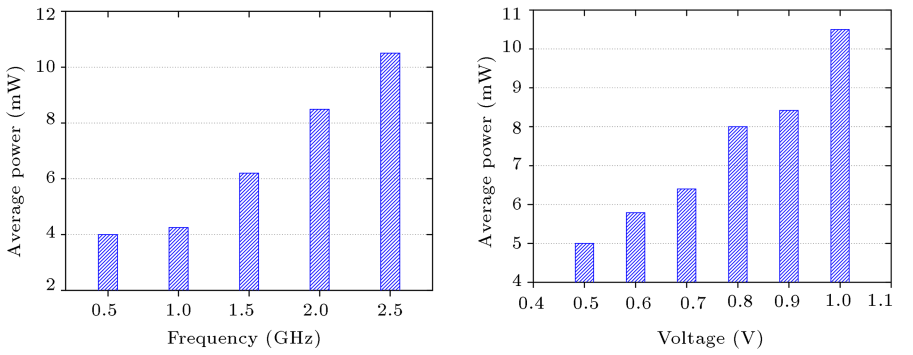
Figure 8. System variation comparison with process corners.

was found as 0.10 mW/V. Figure 10(a) depicts the power consumption of the system with temperature variation. The average power dissipation increases with increase in temperature. The power also increases for the proposed DnC-based ADC, except for a drop at 60°C. The delay variation with respect to frequency is depicted in Figure 10(b). The average delay is seen to be decreasing with an increase in the supply voltage. The rate of decrease in delay with respect to the supply voltage is 3 ps/V.

4.2. Static errors

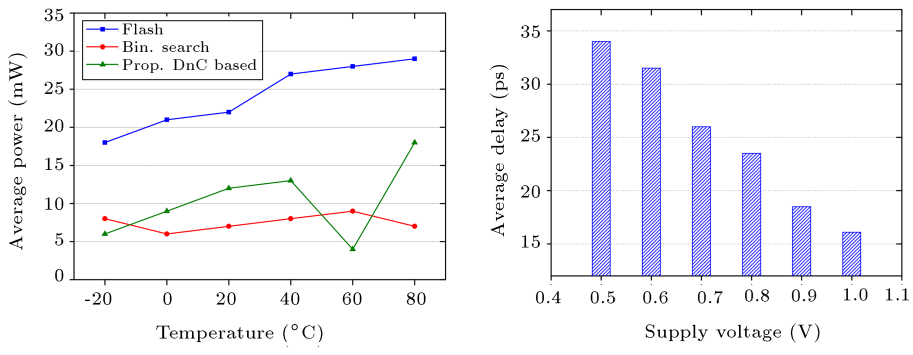
The primary static errors in ADC are INL and DNL that arise due to the comparators' difficulty in estimation below a certain voltage limit level. The input referred offset voltage is low, but the common mode offset voltage is high, which is removed through the use of down voltage converters, as shown in Figure 4. This leads to the lower value of non-linearity errors. Even the kick-back noise is also compensated using a sample and hold switch. The input referred offset deviation is noted to be around 72.5 μV which yields DNL of 0.24 LSB. INL and DNL deviations in the subranging ADC were found to be 0.3/–0.22 LSB and 0.24/–0.32 LSB with an input frequency of 500 MHz and a sampling frequency of 2.5 GS/s, as noted in Figures 11 and 12, respectively.

Monte Carlo simulations were carried out over 1000 trials. The mean value determined from the plot is set as the reference point for further calculations. The non-linearity variations are then plotted in Figures 11 and 12. The results were collected after using offset compensation in the circuits. The kick-back noise is high; yet, as discussed previously, it is compensated using the sample and hold switches. The kick-back noise in the worst case detected in comparator inputs



(a) Average power with a variation of frequency (b) Average power with variation of voltage

Figure 9. Average power responses over variation.



(a) Average power with a variation of temperature (b) Delay variation with frequency

Figure 10. Power-delay response over temperature-voltage.

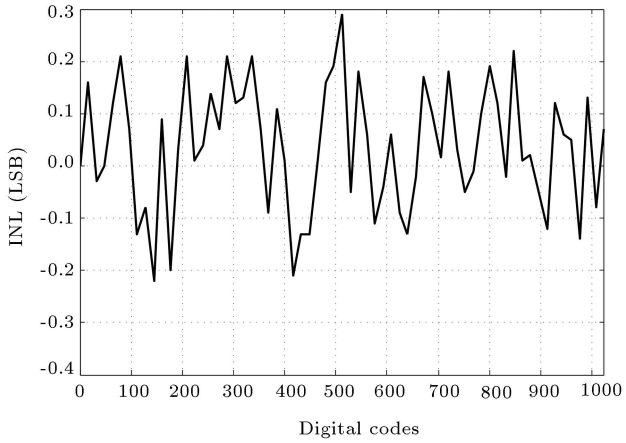


Figure 11. Integrated-Non-Linearity (INL).

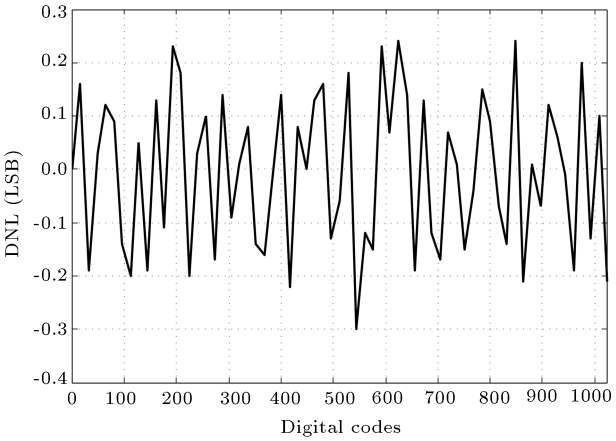


Figure 12. Differential-Non-Linearity (DNL).

of $\delta V_{in} = 0.1$ mV is 0.84 mV and for the best case is 0.12 mV, keeping $\delta V_{in} = 10$ mV for FCMP.

4.3. Power dissipation analysis

One of the limitations of flash ADC is its high power dissipation owing to high-resolution bits. It arises from the fact that $2^N - 1$ number of comparators are used. The DnC, on the other hand, requires only 20 comparators (1023 in traditional flash) at one coarse and three fine levels. Subranging flash with a binary search conversion scheme entails 510 low power digital comparators. However, the binary search requires 10 stages that increase the conversion latency excessively.

Figure 13 shows the distribution of power. Resistor-based ladder requires 58.7% amounting to a large section of power distribution. Subsequently, the comparators (CCMP and FCMP) utilize a sparse amount of 18.4% only.

4.4. Dynamic analysis

Fast Fourier Transform (FFT) is an important attribute to determine the signal characteristics. The frequency response is seen with variation in input frequency at a sampling frequency of 2.5 GHz. The

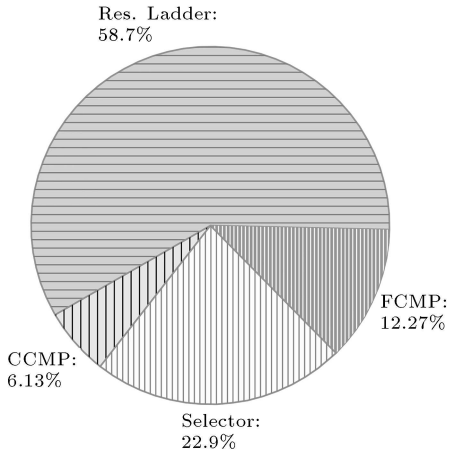


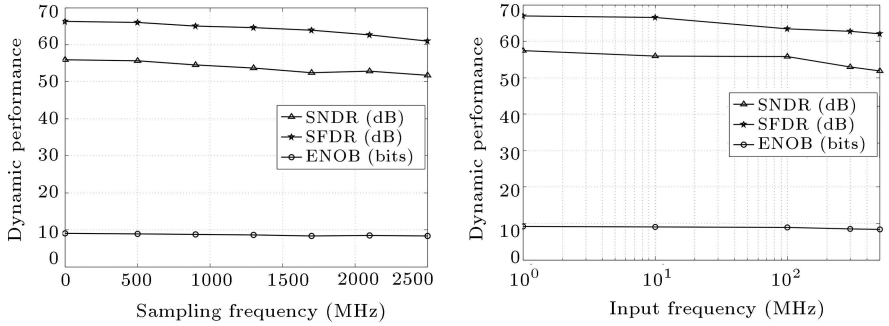
Figure 13. Power distribution among various operational modules.

digitized signal obtained for each sampled analog value is reconstructed as an analog signal by passing it through a DAC whose FFT is then obtained. The dynamic response plots determine the Signal-to-Noise-Distortion Ratio (SNDR), Spurious-Free-Dynamic Range (SFDR), ENOB with 51.8 dB, 62 dB, and 8.3, respectively, at an input frequency of 500 MHz, and a sampling frequency of 2.5 GS/s, as shown in Figure 14(a). The simulated SNDR is seen to be 51.8 equivalent to ENOB and SFDR is 62 dB. Spurs due to the harmonic components increase close to the Nyquist rate and, therefore, SFDR decreases near the Nyquist rate while the spurs are not close to the DC frequency, thus exhibiting an increase in SFDR amounting to 56 dB close to 500 MHz.

ENOB is found to be 9.1 at a low frequency of 500 MHz and at a Nyquist rate of 8.3, as seen in Figure 14(a). SNDR also declines by 4.5 dB due to spurs near the Nyquist frequency following the proximity of DC frequency to the Nyquist range. As observed from Figure 14(b), the dynamic parameters (SNDR and SFDR) decline in value by a small amount of 7 dB while increasing the input frequency. A stable ENOB of approximately 8.3 is seen in this range. The FoM is a prime metric that measures the ADC performance. The dynamic performance with varying supply voltages is presented in Figure 15, which is discussed in the following subsection. It is found to be 14 fJ/conv, which is 44% more than that in [18] and comparable to those in [19,24], as seen in Figure 16. Deguchi et al. [17] designed a faster flash ADC involving a pre-amplifier that allows the ADC to operate at a higher sampling rate; however, the resolution is limited to moderate range.

4.5. Low voltage considerations

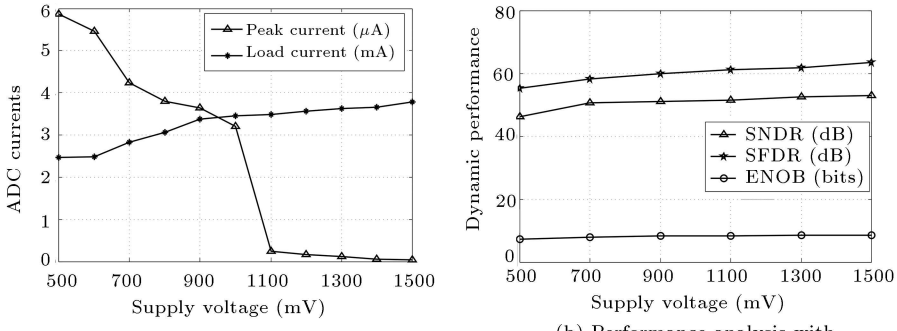
Modern ADCs are integrated into the System on Chips (SoCs) with wireless power supply. The designs are expected to operate at lower supply voltages with-



(a) Dynamic performance versus sampling frequency

(b) Dynamic performance versus input frequency at 2.5 GS/s

Figure 14. Dynamic responses with varying system responses.



(a) ADC currents at varying supply voltage

(b) Performance analysis with supply voltage variation

Figure 15. Analog-to-Digital Converter (ADC) performance analysis with supply voltage variation.

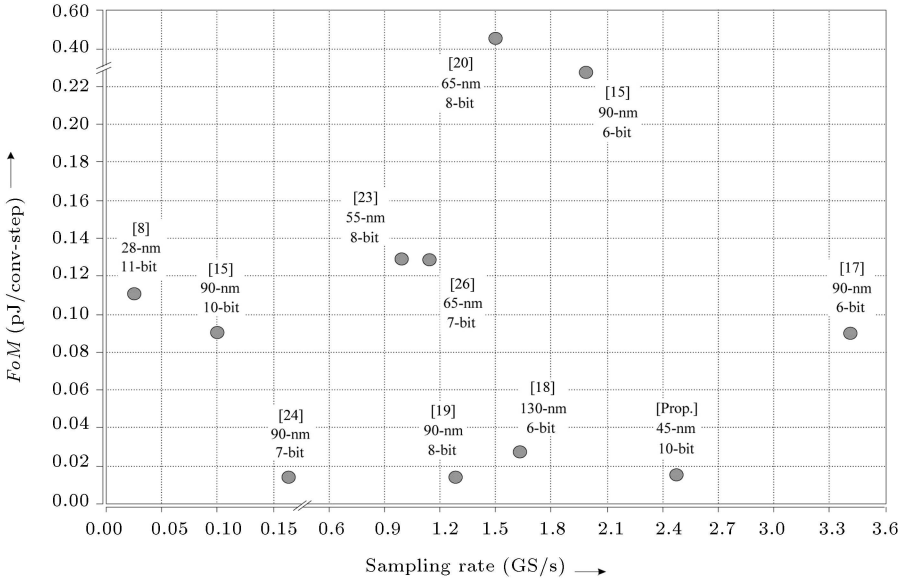


Figure 16. Energy-delay performance of various A/D conversion schemes.

out significant performance degradation. Transistor threshold and the differential input level of the comparator become significant at a lower supply. The proposed subranging ADC is simulated over a range of 500 mV to 1500 mV. The performance of load current shows a sharp decrease with increase in the supply voltages. This occurs because of the presence of the comparator. The load current depends on the fan-out of the comparator and increases with an increase in the fan-out. With increase in supply voltage, the fan-out of the comparator increases and thereby, the load current decreases, as plotted in

Figure 15. However, the peak current response reverses with respect to the supply voltage with low to average changes. This is evident as the comparator power and driving current are proportional to the supply voltage. Dynamic performance (SNDR and SFDR) illustrated in Figure 15(b) exhibits a decrement while scaling the supply voltage down. The behavior is primarily due to the use of comparators. The glitch and kick back noise of the proposed comparator increases with increase in supply voltage. The kick-back noise is attributed to the spurious noise, which is associated with comparators too. The ENOB is also proportional to the noise. As the noise increases with increase in supply voltage, the ENOB decreases. However, this circuit is capable of functioning at a low voltage less than 600 mV as it does not have any transmission gates or pre-amplifiers. The excellent performance of the design at a low supply voltage makes it feasible for practical applications.

5. Conclusion

Flash Analog-to-Digital Converter (ADC) has gained popularity among ADC designers owing to its vast applicability in SoC design platforms. Designing at the subranging level is a must in spite of its lower conversion speed than the traditional flash counterparts. This work presented a 10-bit subranging scheme for flash ADC with an optimized Divide and Collate (DnC) conversion scheme, which yielded better performance than binary search and flash ADC. The constituent components of the module were enhanced with the use of low power charge shared Coarse Comparator (CCMP) and faster Fine Conversion Comparator (FCMP), thereby making it better than the conventional designs. Performance analyses of these subranging comparators exhibited stable offset across environment variations. The DnC algorithm assigned the optimized number of comparators, even at higher resolutions. It reduced Figure-of-Merit (FoM) to a great extent without notable degradation in the excess delay. The design is successful in achieving power consumption of 10.5 mW with an FoM of seemingly good value. Estimation of subranging stages was performed with emphasis on the resolution and conversion algorithm. It showed a moderate number of stage assignments in the proposed DnC. Low power subranging comparators yielded only 18% of the ADC dissipation. Furthermore, the design was functional at a low supply voltage though with degradation of Signal-to-Noise-and-Distoration (SNDR), subsequently affecting the ADC dynamic performance. The design entailed the utility of an ADC with a sampling rate of 2.5 GS/s, which is on average 60% more than the conventional subranging ADC topologies. The time-interleaved and pipelined ADC seemingly provided a better sampling rate, but at the cost of higher computational complexity. This ADC succumbs to low complexity, although the loading effect notably increases with an increase in the number of MUXes. The smaller number of comparators in combination with good static and dynamic performances certainly fits the DnC subranging flash ADC into the modern electronic systems.

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