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Performance improvement of AC-DC power converters under unbalanced conditions

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Abstract. In this paper, a single synchronous reference-frame based control method is proposed to improve the performance of AC-DC interlink converters feeding DC loads under unbalanced AC grid conditions. Unbalanced grid voltages cause undesirable double frequency ($2\omega_0$) oscillations on the DC link voltage in AC-DC converters. In the medium/high power applications, low switching frequency and the oscillatory power of the input filter considerably degrade the functionality of the existing methods for removing $2\omega_0$ ripples from DC link voltage. In this paper, an analytical equation for the terminal active power is derived considering the input filter inductance. Accordingly, suitable current references for the control are proposed to eliminate the undesirable $2\omega_0$ ripples from DC-link voltage considering low switching frequency. It is shown that the filter inductance adds a non-linear term to the active power equation, which complicates the current reference calculation. Also, a real-time recursive method is proposed to solve the equations and find the current references. To evaluate the performance of the proposed method, different grid unbalanced conditions, including asymmetrical short circuit faults, are applied to a test system in the PSCAD/EMTDC environment. Furthermore, the functionality of the proposed method is compared with that of the existing method for unbalanced conditions.

1. Introduction

Voltage Source Converters (VSC) provide efficient and controllable power conversion from AC power to DC, and vice versa. DC power has been used in industrial plants [1–3] and High-Voltage Direct Current (HVDC) systems [4–6]. However, in recent years, trends to use DC power in the DC grid and DC microgrid have been on the rise. DC grids represent a future alternative to AC grids, which benefit from high efficiency, lower weight structure, and less footprint [7–10]. Specifically, medium-voltage DC grids are mainly preferred in the high power industry applications.

A VSC is responsible for regulating the DC voltage and controlling the exchanged power with the AC grid [11,12]. Therefore, any AC grid short circuit fault or disturbance directly affects the DC voltage. This becomes a more challenging issue considering the unbalanced nature of distribution systems and various asymmetrical temporary short-circuit faults in AC systems [13–15]. This problem is intensified in

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high power applications where the DC-link voltage control-loop bandwidth (BW) is limited due to the low switching frequency [16]. A low control BW deteriorates the disturbance rejection capability of the converter [17]. Also, under unbalanced conditions, the effect of the power absorbed by the input filter inductor cannot be ignored. In this condition, the sum of the instantaneous active powers of the three phases is not zero anymore, which results in ripples with the frequency of $2\omega_0$ (ω_0: fundamental frequency) on the instantaneous active power injected into the DC side and DC link capacitor. Furthermore, the filter inductance introduces a right-side zero in the linearized dynamic equation of the system, which can affect the stable operation of the converter [18]. To avoid this problem, the bandwidth of the DC link voltage control loop must be lowered, which again decreases the disturbance rejection capability of the converter. As a result, the conventional control of the DC link could not work properly under unbalanced conditions [18].

Under an unbalanced condition and during asymmetrical short circuit faults, due to the unbalanced grid voltages, the absorbed power from the grid has a pulsating component with the frequency of $2\omega_0$. This pulsating component flows through the DC link capacitor and causes the same frequency components on the DC link voltage. These components degrade the converter functionality and impose greater stress on the capacitor, converter switches, and the DC loads (in DC microgrids application). The power converter control methods under unbalanced conditions can be divided into five categories as follows [19–24]:

1. *Instantaneous Active Reactive Control (IARC)*: In this method, the converter behaves like symmetric resistance at all three phases and absorbs instantaneous constant active power from the grid. Also, the reactive power ripple is considered to be zero under unbalanced conditions. Although this approach provides ripple-free instantaneous active power, the output currents are highly distorted;
2. *Instantaneously Controlled Positive-Sequence (ICPS)*: In this method, the converter instantaneously controls the positive-sequence current in order to control the active power by forcing the negative sequence to zero. This method does not limit the reactive power ripples and less distorted currents are drawn. However, power quality of the currents is not satisfactory yet;
3. *Positive-Negative-Sequence Compensation (PNSC)*: This method takes an active power from the grid by producing positive- and negative-sequence sinusoidal currents. In this scheme, sequence current components are selected such that active power $2\omega_0$ ripples are forced to zero;
4. *Average Active-Reactive Control (AARC)*: In this method, the converter controls the average of the instantaneous active power. Since this method filters the active power ripples in the control system, the ripples still exist in the actual instantaneous active power;
5. *Balanced Positive-Sequence Control (BPSC)*: In this method, the converter only absorbs a positive sequence current from the grid. Absorbing balanced currents from unbalanced grid results in instantaneous active power with relatively large ripples.

Among the five approaches, the first three ones (IARC, ICPS, and PNSC) provide a flow of ripple-free instantaneous active power from the grid at the point of connection. However, the first two ones result in harmonic polluted currents taken from the grid, which is not permitted due to the power quality limits. The absorbed currents are sinusoidal if the Positive-Negative Sequence Compensation (PNSC) method is employed. In this method, the positive and negative sequence components are selected to force the active power $2\omega_0$ ripples to zero.

Following a comparison of the different strategies, the PNSC method is the widely used method in the literature to control the power converter under unbalanced conditions [19–24]. The PNSC scheme is implemented in the Double Synchronous Reference Frame (DSRF) scheme proposed by [25–27]. A DSRF simultaneously employs two clockwise and counterclockwise synchronous reference frames to control the positive and negative sequence currents. Song and Nam [26] and Suh et al. [28] derive an instantaneous power expression at the grid connection point to calculate the current references to remove the pulsating components of the active power. They enhanced the converter performance under unbalanced conditions, but they did not consider the input AC filter effect. Having used the same method, Yazdani and Irvani [16] introduced a unified dynamic model and control strategy for the power converter. Nevertheless, because of using band trap filters in the control structure, the bandwidth of the system inherently is low. To overcome this, Hu and He [29] employed an approach based on the $\alpha\beta$ frame. Changing the frame from the grid voltage oriented synchronous dq frame to the stationary $\alpha\beta$ frame loses the inherent benefit of the synchronous dq frame, which is the decoupling between d and q axes and, also, complicates the control of the converter. Furthermore, upon improving the current controller in [30], the DC voltage regulation for asymmetric wind power Permanent Magnet Synchronous Generator (PMSG) systems in [31], instantaneous power control for suppressing the second-harmonic DC-Bus voltage in [32], power control of three-phase rectifiers under non-ideal grid conditions in [33], and direct power control of Pulse

Width Modulation (PWM) rectifier in [34,35] were also mentioned in assuming PNSC method. However, none of these methods consider the input filter inductance. Yongsug and Lipo [27], Hu and He [29], Roiu et al. [36] proposed control methods that controlled the instantaneous active power at the converter terminals using the terminal voltages instead of the grid voltages. Using the terminal voltages, the filter inductance is considered, and the power equations are linearized. However, the proposed controllers are non-linear. Researchers Almedia et al. [37], Zarei et al. [38], and Al-Akayshee and Yuan [39] proposed methods based on single grid voltage oriented synchronous dq frame. They proposed using a resonant compensator in the voltage control loop to mitigate the $2\omega_0$ DC link voltage oscillations. This remedy requires high bandwidth for the voltage control loop, resulting in a high switching frequency. Furthermore, this method is presented for only the inverter mode of operation and the rectifying mode of operation has not been considered.

In this paper, first, the problem is analytically formulated in a grid voltage-oriented single synchronous "dq" reference frame, which reduces the number of transformations and gives a better insight into the problem. Then, the inverter current references are calculated to remove the undesirable ripples from the active power. It is shown that the filter inductance adds a non-linear term to the instantaneous active power equation, which complicates the current reference calculation. Then, a recursive real-time strategy is proposed to find the current reference considering the filter inductance, which avoids undesirable ripples in the DC link voltage during unbalanced input voltage conditions. Furthermore, the current controller is modified in order to track the proposed current references.

The rest of the paper is organized as follows. The conventional control of the converters including the DC link voltage control strategy is introduced in Section 2. Section 3 describes the effects of the unbalanced AC grid on the DC link voltage quality. In Section 4, the proposed current references calculation and the current control strategy are presented. Finally, simulation results and the conclusion of the study are provided in Sections 5 and 6, respectively.

2. Conventional control of the power converters in normal balanced grid condition

Figure 1 shows the converter power circuit with its control loops and elements. In this structure, a grid voltage-oriented control strategy is used, which aligns the d-axis of the reference frame with the grid voltage space vector. Then, the working frame in this study is based on the grid voltage-oriented synchronous "dq" reference frame. Based on Figure 1, the dynamic equations of the converter input filter in the grid voltage oriented synchronous "dq" frame are:

$$L_f.\frac{di_{td}}{dt} = -R_f.i_{td} + L_f.\omega.i_{tq} + m_d.\frac{V_{DC}}{2} - v_{gd}, \quad (1)$$

$$L_f.\frac{di_{tq}}{dt} = -R_f.i_{tq} - L_f.\omega.i_{td} + m_q.\frac{V_{DC}}{2} - v_{gq}. \quad (2)$$

In these equations, there are couplings between the d and q axis frames ($+L_f.\omega.i_{tq}$ and $-L_f.\omega.i_{td}$). To obtain independent dynamics, decoupling signals are fed

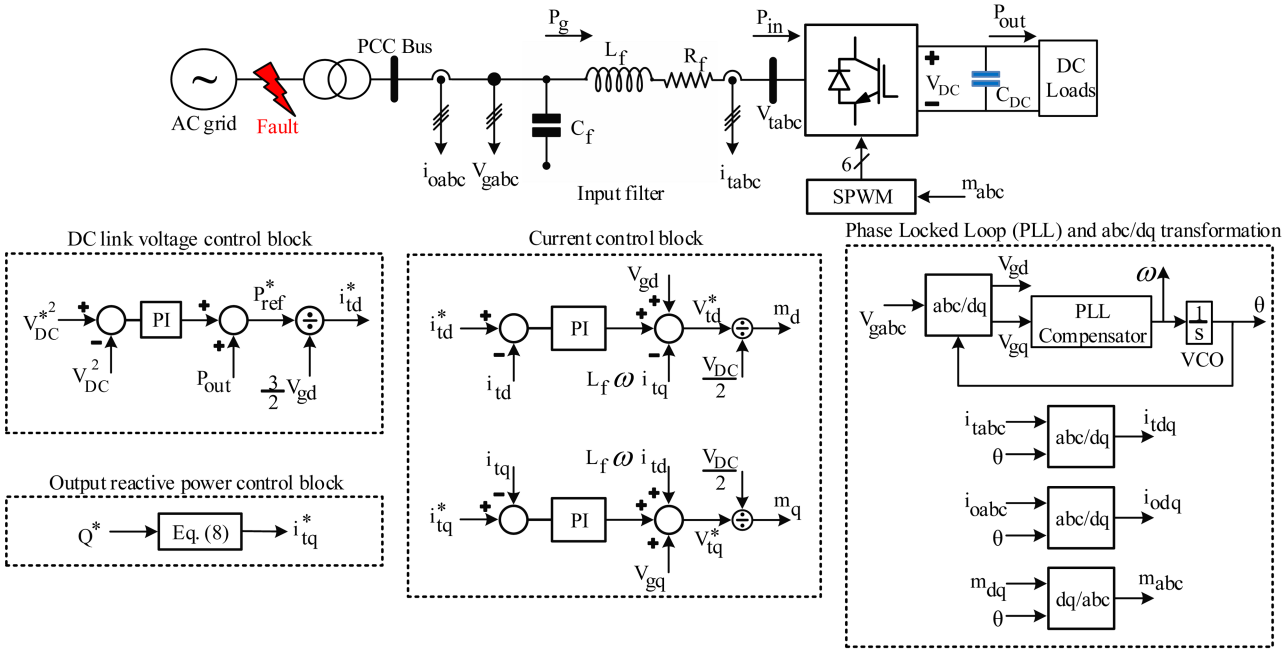

Figure 1. AC-DC power converter circuit with its control loops.

to the current control block. Also, to compensate the load dynamics, a feed-forward from the grid voltages (v_{gd}, v_{gq}) is used (see the current control block in Figure 1) [40].

A PI compensator is a commonly used controller in the literature for the current control block. The optimum PI coefficients are computed using the *amplitude optimization* method [41]. Based on [41], an optimum current control PI compensator is as follows:

$$PI = \frac{1}{\tau}.\frac{L_f s + R_f}{s}, \tag{3}$$

where τ^{-1} is the bandwidth of the current control loop, which is limited by the converter switching frequency.

Considering Eq. (3) along with Eqs. (1)–(2) and the current control block in Figure 1, the closed-loop transfer function of the current control loops, which is of first-order dynamic, is obtained in the following after applying the feed-forward and decoupling signals cancellation [18]:

$$\frac{i_{td}}{{i_{td}}^*} = \frac{i_{tq}}{{i_{tq}}^*} = \frac{1}{1+\tau.s}, \tag{4}$$

where ${i_{td}}^*$ and ${i_{tq}}^*$ are the current references in the d and q axis frames in the Laplace domain, respectively. The other blocks in Figure 1 are described in the following subsections.

2.1. Phase locked loop

Converters can control the DC link voltage and inject a predefined reactive power only when they are properly synchronized with the AC grid. Therefore, a proper synchronization algorithm must be utilized. A Phase-Locked Loop (PLL) is a commonly used method for synchronization purposes that estimates the angle of the grid voltage space vector. In three-phase systems, a PLL processes v_{gq} with a compensator and creates a synchronous phase angle, θ, using a resettable integrator, whose output is reset to zero whenever it exceeds 2π, as shown in Figure 1. This integrator is implemented by means of a Voltage-Controlled Oscillator (VCO) [41]. It is worth noting that a PLL compensator has an integrator, which guarantees a zero steady-state error in extracting the phase angle. Then, considering the grid voltage oriented control scheme, v_{gq} is settled at zero by the correct operation of the PLL [25].

2.2. Reactive power control block

As shown in Figure 1, the current reference in the q axis is computed from the reactive power set-point. The converter apparent power can be calculated in the grid voltage-oriented synchronous "dq" frame as:

$$P_g + jQ_g = \frac{3}{2}.(v_{gd} + jv_{gq}).(i_{td} + ji_{tq})^*. \tag{5}$$

Upon employing the grid voltage-oriented control scheme and considering the PLL operation, v_{gq} will be reduced to zero and the input active and reactive power equations can be simplified as:

$$P_g = \frac{3}{2}.v_{gd}.i_{td}, \tag{6}$$

$$Q_g = -\frac{3}{2}.v_{gd}.i_{tq}. \tag{7}$$

Using Eq. (7) and considering the reactive power injected by the AC filter capacitance, the current reference in the q axis will be obtained from the reactive power set point as:

$${i_{tq}}^{ref} = \frac{Q_g^*}{-3/2.v_{gd}} + \frac{3}{2}.C_f.\omega.v_{gd}, \tag{8}$$

where Q_g^* is the converter reactive power.

2.3. DC link voltage control block

As mentioned earlier, control of the DC link voltage is the main duty of the converter to provide DC loads with a reliable power. The dynamic equation of the DC link capacitor can be rewritten as follows:

$$P_{in} = P_{out} + \frac{1}{2}.C_{DC}.\frac{d}{dt}({V_{DC}}^2). \tag{9}$$

The conventional control scheme assumes that P_{in} can be replaced by P_g which is the absorbed power by the converter at the grid connection point [18]. Therefore, using Eqs. (6) and (9), one can write:

$$\frac{3}{2}.v_{gd}.i_{td} = P_{out} + \frac{1}{2}.C_{DC}.\frac{d}{dt}({V_{DC}}^2). \tag{10}$$

In Eq. (10), P_{out} can be considered as a disturbance that can be compensated by a feed-forward signal, as shown in the DC link voltage control block in Figure 1. The second term on the right-hand side of Eq. (10) contains a nonlinear term that complicates the DC link voltage controller design. To remove this nonlinearity and simplify the controller design, the energy stored in the DC link capacitor W_{DC} (α V_{DC}^2) is defined as a new control variable instead of the DC link voltage [42,43]. This remedy converts the nonlinear equation (10) to a linear one as:

$$\frac{3}{2}.v_{gd}.i_{td} = P_{out} + \frac{d}{dt}(W_{DC}). \tag{11}$$

Eq. (11) shows that i_{td} is the single control input by which W_{DC} settles at its set-point. Hence, the reference value of i_{td} must be obtained from the DC link voltage control loop as given in Eq. (12) [42] and it is shown in Figure 1 (see DC link voltage control block):

$${i_{td}}^* = \frac{P_{out}}{(3/2).v_{gd}} + PI.({W_{DC}}^* - W_{DC}). \tag{12}$$

As mentioned earlier, the first term on the right-hand side of Eq. (12) is a feed-forward signal to compensate the effect of P_{out}. Also, the PI compensator with

proper tuning ensures that W_{DC} will reach its reference value with a zero steady state error.

3. Effects of AC grid asymmetrical faults and imbalances on the converter operation and the DC link voltage control

The interlink converter regulates its DC side voltage and reactive power. Also, it is mentioned that asymmetrical faults and imbalances in the AC grid can disturb the DC side voltage control functionality. To discuss this challenge, assume that the AC grid voltages and currents in the stationary "*abc*" reference frame are unbalanced as follows:

$$\begin{cases} v_{ga} = V_1.\cos(\theta) + V_2.\cos(\theta+\delta) \\ v_{gb} = V_1.\cos(\theta-\frac{2\pi}{3}) + V_2.\cos(\theta+\delta+\frac{2\pi}{3}) \\ v_{gc} = V_1.\cos(\theta+\frac{2\pi}{3}) + V_2.\cos(\theta+\delta-\frac{2\pi}{3}) \end{cases} \quad (13)$$

$$\begin{cases} i_{ta} = I_1.\cos(\theta-\alpha_1) + I_2.\cos(\theta-\alpha_2) \\ i_{tb} = I_1.\cos(\theta-\alpha_1-\frac{2\pi}{3}) + I_2.\cos(\theta-\alpha_2+\frac{2\pi}{3}) \\ i_{tc} = I_1.\cos(\theta-\alpha_1+\frac{2\pi}{3}) + I_2.\cos(\theta-\alpha_2-\frac{2\pi}{3}) \end{cases} \quad (14)$$

where subscripts 1 and 2 indicate positive and negative sequence components, respectively. Also, α_1, α_2, and δ are the corresponding phase angles.

Substituting Eqs. (13) and (14) into Eq. (15) along with some simplification results in Eq. (16), which is the total instantaneous active power flowing from the AC grid to the converter:

$$P_g = v_{ga}.i_{ta} + v_{gb}.i_{tb} + v_{gc}.i_{tc}, \quad (15)$$

$$\begin{aligned} P_g =& \frac{3}{2}.[V_1.I_1.\cos(\alpha_1) + V_2.I_2.\cos(\alpha_2+\delta)] \\ &+ \frac{3}{2}.\big[V_2.I_1.\cos(2\theta+\delta-\alpha_1) \\ &+ V_1.I_2.\cos(2\theta-\alpha_2)\big]. \end{aligned} \quad (16)$$

The second part on the right-hand side of Eq. (16) is of pulsating nature with a frequency of $2\omega_0$.

Besides, the instantaneous power absorbed by the AC filter is also important in this regard. To clarify the subject even more, the instantaneous power of the input filter is:

$$P_{L_f} = L_f.\left[\frac{di_{ta}}{dt}.i_{ta} + \frac{di_{tb}}{dt}.i_{tb} + \frac{di_{tc}}{dt}.i_{tc}\right]. \quad (17)$$

Using Eq. (14) and after some simplifications, Eq. (17) changes to:

$$P_{L_f} = -3.L_f.\omega.I_1.I_2.\sin(2\theta+\alpha_1+\alpha_2). \quad (18)$$

As shown in Eq. (18), the instantaneous power of L_f has a zero average value and an oscillating component with the frequency of $2\omega_0$ in the unbalanced current condition ($I_2 \neq 0$). This oscillating component affects the DC side voltage, specifically when there are severe faults and imbalances in the AC grid. In other words, flowing of an oscillating power into the DC side as well as the DC link capacitor based on Eq. (9) causes the DC link voltage to have an undesirable ripple with the same frequency.

It is worth noting that the instantaneous power of P_{L_f} can be forced to zero by the flow of the balanced currents ($I_2 = 0$) through the input filter. This control strategy is called BPSC scheme, as described in Section 2, which only absorbs a positive sequence current from the grid. As mentioned earlier, absorbing balanced currents from unbalanced grid results in instantaneous active power with relatively large ripples. For this reason, the studies in the literature have widely used PNSC scheme which absorbs both positive and negative sequence currents under unbalanced conditions. However, the impact of filter instantaneous power P_{L_f} should be considered in the current reference calculation, which has been considered and covered in this paper.

In the next section, the proposed control methods are presented to overcome the above challenges.

4. Proposed control scheme for AC-DC converter under unbalanced AC grid condition

In high power-consuming applications, the switching frequency of converters is limited to a few kHz and therefore, the bandwidth of the current and DC link voltage control loops is rather low. This means that the DC link voltage control loop cannot compensate the pulsating components of the voltage ripples. Also, the ripples with a frequency of $2\omega_0$ in the converter input filter are important in this case since they affect the pulsating power delivered to the DC side of the converter.

Considering the limited BW and the input filter inductance effect, this paper proposes the current references in the grid voltage-oriented synchronous "*dq*" reference frame to remove the ripples from the instantaneous active power and the DC link voltage. Also, the current controller ($C_i(s)$) is modified to ensure accurate reference tracking.

4.1. Proposed current references and their calculation approach

In this part, the current references in the grid-voltage oriented synchronous "*dq*" reference frame are calculated such that the ripples with a frequency of $2\omega_0$ in the instantaneous active power are removed. Eq. (19) shows the power balance at the converter terminal:

$$P_{in} = P_g - P_{L_f}, \quad (19)$$

where P_g and P_{L_f} are given in Eqs. (16) and (18), respectively. Substituting Eqs. (16) and (18) into Eq. (19) along with doing some simplification yields:

$$\begin{aligned} P_{in} =& \frac{3}{2}.V_1.x_1 + \frac{3}{2}.V_2.[x_3.\cos(\delta) + x_4.\sin(\delta)] \\ &+ \frac{3}{2}.[V_2.x_1.\cos(\delta) - V_2.x_2.\sin(\delta) + V_1.x_3 \\ &+ 2.L_f.\omega.(x_2.x_3 + x_1.x_4)].\cos(2\theta) \\ &- \frac{3}{2}.[V_2.x_1.\sin(\delta) + V_2.x_2.\cos(\delta) + V_1.x_4 \\ &- 2.L_f.\omega.(x_1.x_3 - x_2.x_4)].\sin(2\theta), \end{aligned} \tag{20}$$

where x_1, x_2, x_3, and x_4 are $I_1.\cos(\alpha_1)$, $I_1.\sin(\alpha_1)$, $I_2.\cos(\alpha_2)$, $I_2.\sin(\alpha_2)$, respectively.

This equation in comparison with Eq. (6) shows the instantaneous active power at the terminal of the converter (P_{in}) and not at the grid connection point (P_g). As it is expected, P_{in} has a DC and a pulsating component. The DC component is equal to the constant active power reference of ${P_{ref}}^*$ in Figure 1, which comes from the DC link voltage control loop, and the pulsating part should be settled to zero. In doing so, proper values of x_1, x_2, x_3, and x_4 can be obtained by solving Eqs. (21)–(23):

$${P_{ref}}^* = \frac{3}{2}.V_1.x_1 + \frac{3}{2}.V_2.[x_3.\cos(\delta) + x_4.\sin(\delta)], \tag{21}$$

$$\begin{aligned} &V_2.x_1.\cos(\delta) - V_2.x_2.\sin(\delta) + V_1.x_3 \\ &\quad + 2.L_f.\omega.(x_2.x_3 + x_1.x_4) = 0, \end{aligned} \tag{22}$$

$$\begin{aligned} &V_2.x_1.\sin(\delta) + V_2.x_2.\cos(\delta) + V_1.x_4 \\ &\quad + 2.L_f.\omega.(x_2.x_4 - x_1.x_3) = 0. \end{aligned} \tag{23}$$

Eqs. (22) and (23) ensure that the terminal power will not have a pulsating component, thereby removing the pulsating component from the DC link voltage. To find the unknown four variables in Eqs. (21)–(23), another equation is needed. By computing the grid voltage-oriented synchronous "dq" frame components of the currents in Eq. (14) and substituting them into Eq. (7), the DC component of the reactive power gives the fourth equation as follows:

$$Q_{ref} = -\frac{3}{2}.V_1.x_2. \tag{24}$$

Solving Eqs. (21)–(24) gives the unknown variables x_1, x_2, x_3, and x_4, which are equal to $I_1.\cos(\alpha_1)$, $I_1.\sin(\alpha_1)$, $I_2.\cos(\alpha_2)$, and $I_2.\sin(\alpha_2)$, respectively. Then, substituting these variables into Eq. (14) and calculating the grid voltage oriented synchronous dq frame equivalents of the currents give the current control references as:

$$\begin{aligned} {I_d}^{ref} &= x_1 + x_3.\cos(2\theta) - x_4.\sin(2\theta), \\ {I_q}^{ref} &= x_2 - x_3.\sin(2\theta) - x_4.\cos(2\theta). \end{aligned} \tag{25}$$

These current references ensure that the undesirable oscillations on the DC link voltage will be removed.

It is worth noting that the grid voltage parameters of V_1, V_2, and δ are needed to solve the above equations. They can be obtained by measuring the grid voltage, transferring them to the grid-voltage oriented synchronous "dq" reference frame, and using a method based on a virtual quadrature signal generator as described in [44]. Using this method ensures a minimum interference over the control loop with a fast response and a smooth overshoot [44].

As shown in Eqs. (21)–(24), the equations for calculating the current references are nonlinear and cannot be solved by routine methods. To solve them, the following real-time recursive method is proposed:

Step 1. Eq. (26) is the first equation, which is used in the first step of calculation obtained from Eq. (21), where superscripts "k" and "$k-1$" represent the values at "k" and "$k-1$" time steps. Using this equation, ${x_1}^k$ can be obtained by substituting previous step values of x_3 and x_4 into Eq. (26). It should be mentioned that initial values of x_3 and x_4 (x_3^0 and x_4^0) are considered zero in the first step of simulation when running the system.

$$\begin{aligned} \frac{3}{2}.V_1.{x_1}^k =& {P_{ref}}^* - \frac{3}{2}.V_2.[{x_3}^{k-1}.\cos(\delta) \\ &+ {x_4}^{k-1}.\sin(\delta)]. \end{aligned} \tag{26}$$

Step 2. Using ${x_1}^k$ obtained by the previous step and considering ${x_2}^k$ from Eq. (24), ${x_3}^k$ and ${x_4}^k$ are given in Eq. (27) as shown in Box I.

Step 3. In this step, the values ${x_3}^k$ and ${x_4}^k$ obtained from Step 2 are used in Step 1 to determine ${x_1}^{k+1}$. By calculating ${x_1}^{k+1}$, ${x_3}^{k+1}$ and ${x_4}^{k+1}$ values are

$$\begin{bmatrix} {x_3}^k \\ {x_4}^k \end{bmatrix} = \frac{V_2}{(V_1 + 2.L_f.\omega.x_2)^2 + (2.L_f.\omega.x_1)^2} \times \begin{bmatrix} V_1.(-{x_1}^k.\cos(\delta) + {x_2}^k.\sin(\delta)) + 2.L_f.\omega.\sin(\delta).({x_1}^{k^2} + {x_2}^{k^2}) \\ -V_1.({x_1}^k.\sin(\delta) + {x_2}^k.\cos(\delta)) - 2.L_f.\omega.\cos(\delta).({x_1}^{k^2} + {x_2}^{k^2}) \end{bmatrix}. \tag{27}$$

Box I

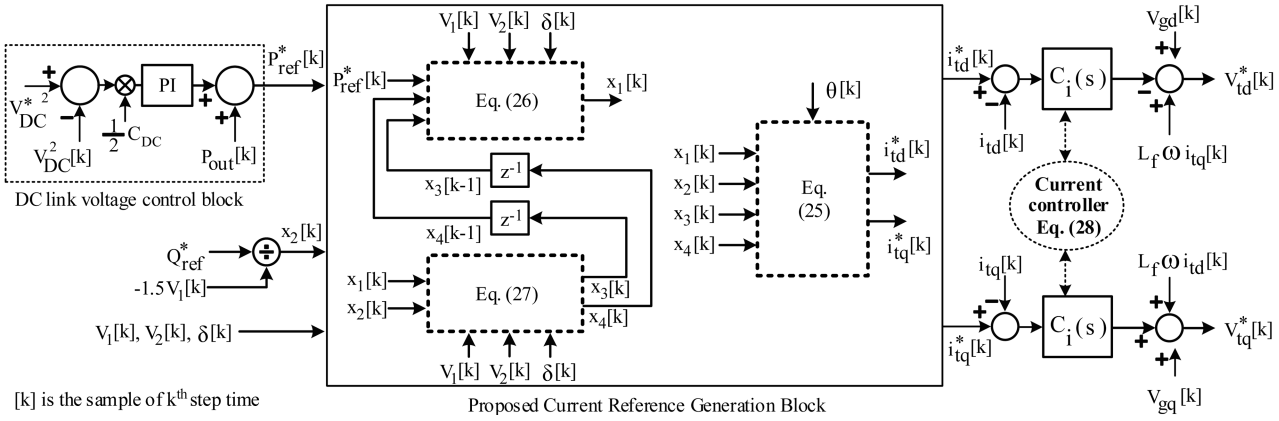

Figure 2. The converter control structure considering the proposed current references for the removal of double frequency ripples from DC-link voltage.

computed using Eq. (27) according to Step 2. This recursive process is continuously performed in each step, and the current references of Eq. (25) are updated correspondingly.

It is worth noting that the proposed current reference generation method works in real time, which takes the inputs and accordingly produces proper current references under both balanced and unbalanced conditions. Under the balanced condition, according to Eq. (27), the resulting current references are also balanced since $V_2 = 0$. Following the occurrence of an unbalanced condition, V_2 will take a non-zero value and then, the proposed method automatically updates the current references in a real-time scheme. Figure 2 graphically represents the proposed procedure for obtaining the proposed current references.

4.2. Modified current controller

As Eq. (25) shows, the derived current references have pulsating components in addition to a constant component. Then, the controller should have a large gain for this pulsating component as well as for the constant component. To ensure this, the following modified compensator is suggested:

$$C_i(s) = \frac{1}{\tau}.\frac{L_f.s + R_f}{s}.\frac{s^2 + 2\xi.(2\omega_0).s + (2\omega_0)^2}{s^2 + (2\omega_0)^2}, \qquad (28)$$

where the gain $1/\tau$ demonstrates the bandwidth of the current controller.

This compensator has an integrator, which ensures a zero steady-state error in tracking the constant component of the current references. Also, another resonant term is employed to ensure a zero steady-state error for the components with the frequency of $2\omega_0$. Finally, to improve the transient behavior of the current control loop, zero as the value of the input filter pole $s = -(R_f + r_{on})/L_f)$ is also added to this compensator.

Under unbalanced conditions, the input signal of the PLL (v_{gq}) has $2\omega_0$ term ripples, which may degrade the PLL operation and the synchronization process. In order to solve this problem, a modified PLL compensator is used as follows [18]:

$$C_{PLL} = k_1.\frac{s+z}{s}.\frac{s^2 + (2\omega_0)^2}{s^2 + 2\xi.(2\omega_0).s + (2\omega_0)^2}, \qquad (29)$$

where k_1 and z are the compensator gain and zero, respectively.

This compensator has a mid-reject characteristic in the frequency of $2\omega_0$. Therefore, the negative sequence components characterized by pulsating nature at a frequency of $2\omega_0$ will be removed. A pole at $s = 0$ is also added to ensure a zero steady-state error in finding the synchronous angle. Moreover, to improve the frequency and time-domain characteristics of the PLL loop, zero to $s = -z$ has also been added.

5. Simulation result

This section examines the functionality of the proposed method. The test system in Figure 1 is simulated, which consists of a 20 kV AC grid with its Thevenin equivalent, a 20/5 kV 16 MVA transformer ($\Delta - \Delta$ connection) with 5% leakage reactance, and a 16 MVA converter that regulates the DC link voltage. The DC link voltage is selected as 10 kV and the total load of the DC grid is 10 MW (two 5 MW loads). It is further assumed that the AC grid is an unbalanced network with V^-/V^+ ratio of 6%. The modified and conventional PLL compensators are given in Eqs. (30) and (31), respectively.

$$C_{PLL} = \frac{0.06 \times s + 2.21}{s} \cdot \frac{s^2 + (2\pi \times 100)^2}{s^2 + 1538 \times s + (2\pi \times 100)^2}, \qquad (30)$$

$$C_{PLL} = \frac{0.07 \times s + 5.17}{s}. \qquad (31)$$

The converter parameters are shown in Table 1.

Table 1. converter parameters.

Parameter	Value	Parameter	Value
R_f	0.01 Ω	C_{DC}	1000 μF
L_f	3.5 mH	f_{sw}	2 kHz
C_f	250 μF	DC load	10 MW

Also, the current controller and the DC link voltage controllers are:

$$C_i = \frac{2.19\times s+6.25}{s}.\frac{s^2+620\times s+(2\pi\times 100)^2}{s^2+(2\pi\times 100)^2}, \quad (32)$$

$$C_v = \frac{96\times s+3000}{s}. \quad (33)$$

The AC grid is simulated with its Thevenin model with an equivalent impedance of 0.8 Ω and the voltage values of (in kV):

$$V_a = 11.55\angle 0, V_b = 10.43\angle -118, V_c = 12.36\angle 122.$$

To show the performance of the proposed scheme, different scenarios are considered for the test system of Figure 1, and it is compared with that of the existing method in the literature. The compared existing method works based on removing double frequency oscillations from instantaneous active power at the grid connection point. This method improves the converter's performance under unbalanced conditions compared to the conventional method described in Section 2. However, the input filter inductance effect has not been included.

5.1. Evaluation of the PLL response

In this part, the operations of the conventional and modified PLL compensators are compared. Assume that the converter has been connected to the AC grid and the grid voltages are unbalanced at the imbalance ratio of 6%. A temporary Single Line to Ground (SLG) fault in the location shown in Figure 1 with $R_{fault} = 1\ \Omega$ occurs at $t = 1.5$ sec. The stationary "*abc*" and the grid-voltage oriented synchronous "*dq*" reference frames voltage waveforms on the converter side of the transformer are depicted in Figure 3(a) and (b), respectively. As shown in the figure, due to the delta connection of the transformer, the effect of an SLG fault in the grid side of the transformer appears at other two phases on the converter side of the transformer. The output frequencies of the conventional and modified PLLs are depicted in Figure 4. As shown in the figure, the conventional PLL finds the frequency of the AC grid with 5% ripple when the grid is unbalanced. However, during the fault, the frequency oscillates in a larger range, and then it

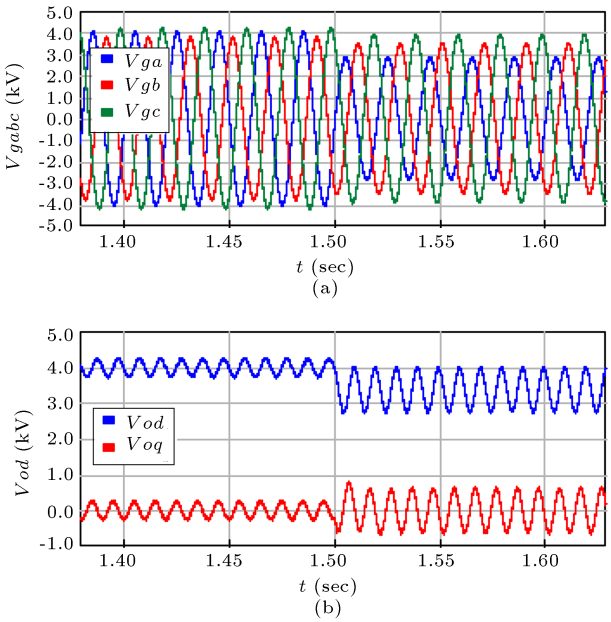

Figure 3. AC grid voltages on the converter side of the transformer which has 6% imbalance ratio for $t < 1.5$ s and an Single Line to Ground (SLG) fault with $R_{fault} = 1\ \Omega$ occurs on the grid side of the transformer at $t = 1.5$ sec: (a) abc frame and (b) grid voltage-oriented synchronous *dq* frame (*dq* components are calculated by the modified Phase-Locked Loop (PLL)).

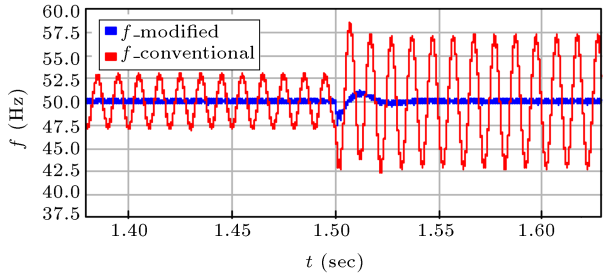

Figure 4. Comparison of the conventional and proposed modified Phase-Locked Loop (PLL) compensator behaviors (estimated frequency) when the short-circuit fault of Figure 3 occurs.

adversely affects the power converter functionality. On the other hand, the modified PLL tracks the frequency of the AC grid with negligible ripple in both normal and faulty conditions. To provide a fair comparison in the following subsections, the modified PLL is employed for both proposed and existing methods.

5.2. Operation under unbalanced condition

To investigate the steady-state operation of the proposed method, two 5 MW load step changes at times 0.75 sec and 1 sec are applied on the DC side of the power converter. The grid voltages are unbalanced at the imbalance ratio of 6%, which are shown in Figure 5(a). The DC link voltage waveforms for both the existing and proposed methods are depicted

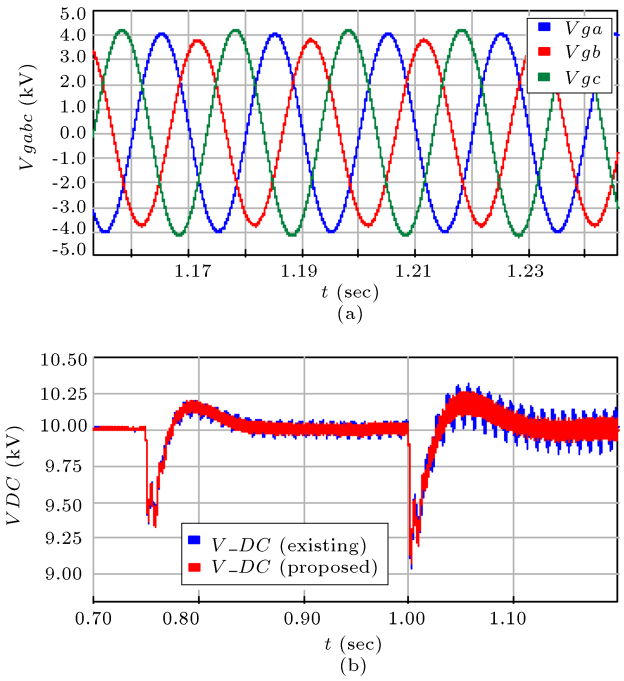

Figure 5. Comparison in the functionality of the existing and proposed DC link voltage control methods when two 5 MW load step changes occur at 0.75 sec and 1 sec under unbalanced grid conditions with an imbalance ratio of 6%: (a) grid voltage waveforms and (b) DC link voltage.

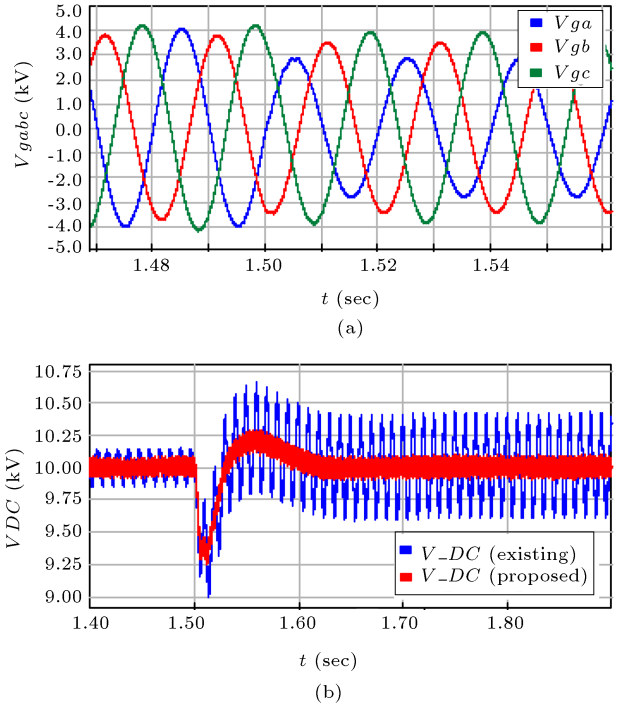

Figure 6. Comparison in the functionality of the existing and the proposed DC link voltage control methods when a single-line-to-ground fault with $R_{fault} = 1\ \Omega$ occurs on the grid side of the transformer at $t = 1.5$ sec: (a) grid voltage waveforms and (b) DC link voltage.

in Figure 5(b). As shown in this figure, there are oscillations ($2\omega_0$ components) with a small amplitude (2.5%) in the response of the existing method, which is allowed in terms of standard limits. On the other hand, the proposed method has effectively eliminated these ripples.

5.3. Operation under moderate short circuit faults

An SLG fault with $R_{fault} = 1\ \Omega$ occurs on the grid side of the transformer at $t = 1.5$ sec. Figure 6(a) shows the power converter input voltages in which two phases "a" and "b" are affected by the fault due to the delta connection of the transformer. Figure 6(b) demonstrates the response of the proposed and existing methods. As expected, the ripples on the DC side voltage increase if the existing method is used, but it is eliminated by the proposed method.

5.4. Operation under severe short circuit fault

In this part, a severe SLG fault with $R_{fault} = 1\ \Omega$ is applied to the system at 1.5 sec. This fault extremely decreases the phase voltage on the grid side of the transformer. The converter-side voltage of the transformer and the DC link voltages with the existing and proposed methods are presented in Figure 7(a) and (b), respectively. As can be seen from this figure, there are pulsating voltage ripples with a large amplitude when the existing control is employed, while the proposed method effectively eliminates these ripples. This large value of oscillation creates over-voltage on the DC link voltage, which may unnecessarily trigger the DC side over-voltage protection even under temporary short-circuit faults with a small duration (of few hundreds of milliseconds).

The input currents are depicted in Figure 7(c) and (d) for the proposed and existing schemes, respectively. As shown in Figure 7(d), ignoring the impact of the filter inductance in the control scheme of the existing method results in current references with a large amplitude. However, considering the filter inductance in the proposed control scheme considerably improves the current references and correspondingly the actual currents, as shown in Figure 7(c). This is also an important subject in terms of power converter over-current protection. Power converters are protected against over-currents by means of current limiter incorporated into the current control scheme. The current limiter instantaneously applies a limit to output current and in the case of an overload or a short-circuit fault, the output current amplitude is limited. In such circumstances, the DC link controller cannot maintain the control task, and the power converter should be tripped. According to the results in Figure 7(c) and (d), using the existing control scheme may result in activation of the current limiter, which is avoided by employing the proposed

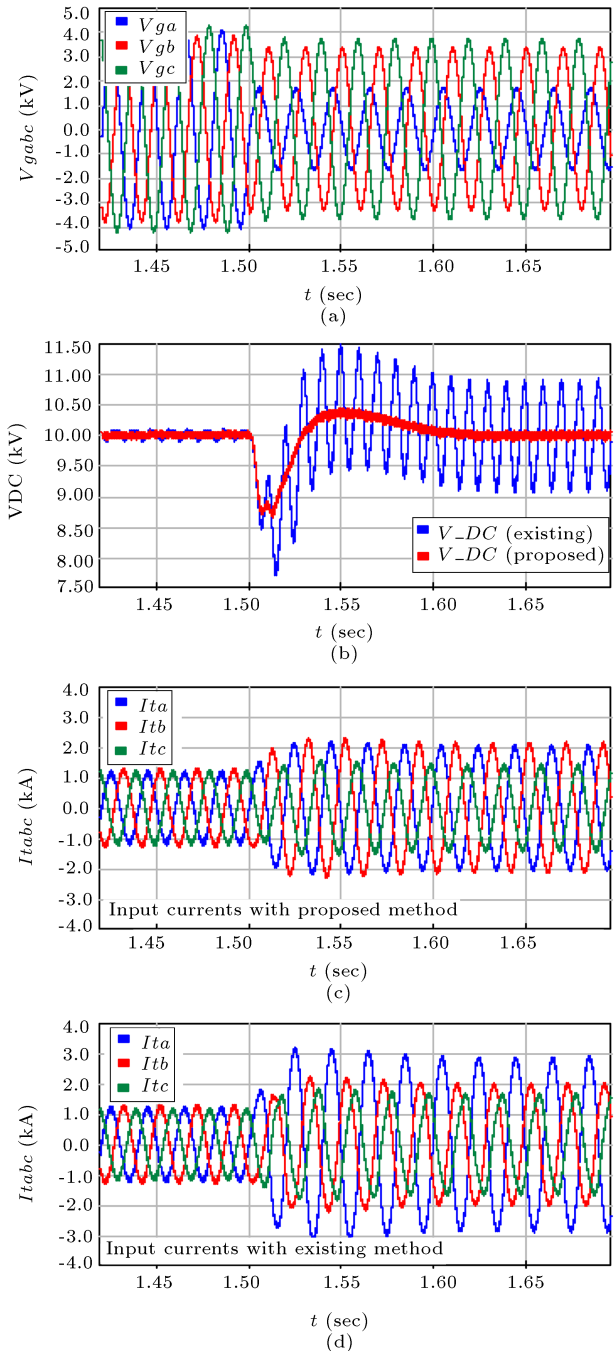

Figure 7. Comparison in the functionality of the existing and the proposed DC link voltage control methods when a severe single-line-to-ground fault with $R_{fault} = 1\ \Omega$ occurs on the grid side of the transformer at $t = 1.5$ sec: (a) grid voltage waveforms, (b) DC link voltage, (c) power converter input currents with the proposed method, and (d) power converter input currents with existing method under unbalanced conditions.

scheme. Therefore, using the proposed method not only avoids any unnecessary disconnection of the power converter due to the double frequency ripples in DC link voltage, but also improves the power quality of the input currents drawn from the grid.

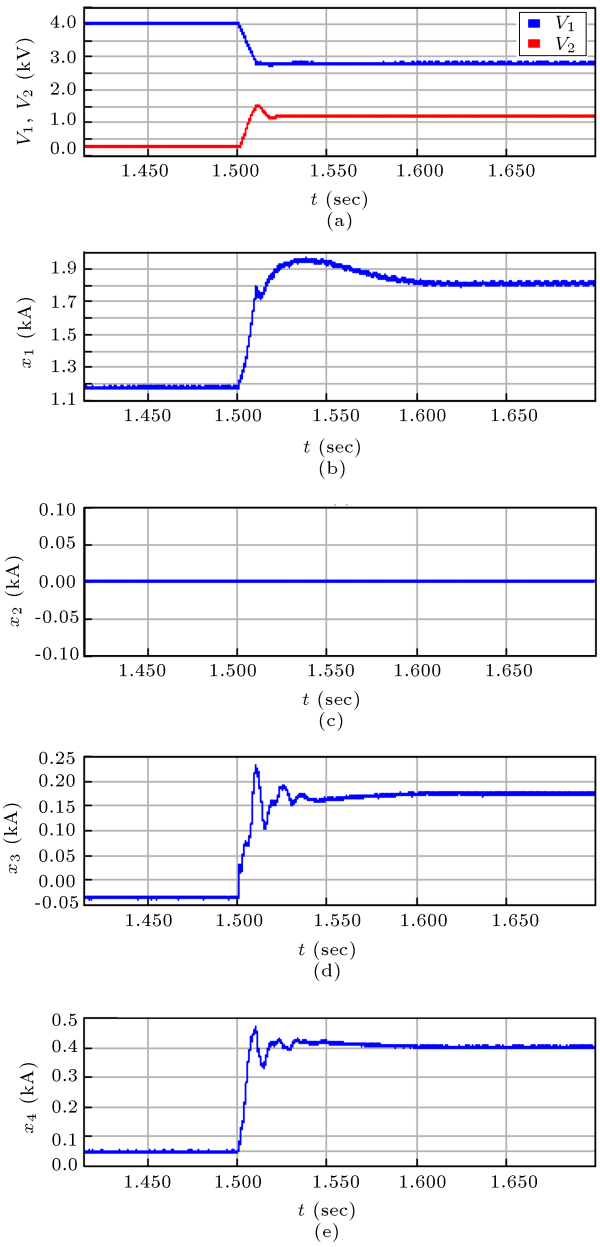

Figure 8. The variations on the waveforms of V_1 and V_2 and calculated values of x_1, x_2, x_3, and x_4 when a severe single-line-to-ground fault with $R_{fault} = 1\ \Omega$ occurs on the grid side of the transformer at $t = 1.5$ sec: (a) V_1 and V_2 variations, (b) x_1 variation, (c) x_2 variation, (d) x_3 variation, and (e) x_4 variation.

To further analyze the proposed real-time recursive method, the variations of the variables x_1, x_2, x_3, and x_4 are depicted in Figure 8. As shown in Figure 8 (a), by applying the fault at $t = 1.5$ sec, the positive sequence voltage decreases from 4 kV to 2.78 kV, and the negative sequence voltage increases from 0.25 kV to 1.17 kV, which shows a severe unbalanced condition. As mentioned earlier, before fault occurrence, the grid is unbalanced at the imbalance ratio of 6% (i.e., 0.25/4=0.06) and it increases to 42%

(1.17/2.78=0.42) when the fault occurs. By occurring the fault, the proposed method automatically updates x_1, x_2, x_3, and x_4 values to find the proper current references as it works in real time with a closed-loop manner. The variations of x_1, x_2, x_3, and x_4 are depicted in figures 8(b)–(e), respectively. As shown in these figures, when the fault occurs, the values are changed from previous steady-state values (unbalanced condition) to the new steady-state values (short circuit condition). As can be seen from the results, the proposed method does not need any fault occurrence detection strategy, since the values are updated in real time in a closed-loop system, as described in Figure 2.

6. Conclusion

This paper enhanced the performance of the power converters by reducing the pulsating ($2\omega_0$) ripples in the DC link voltage under unbalanced input voltage conditions. This performance improvement becomes more essential in medium/high power applications in which the switching frequency is low, and the effect of the input filter cannot be neglected. In this paper, the problem was analytically formulated considering the input filter inductance. Then, a recursive approach was proposed for solving the related nonlinear equations to determine the proper current references. Also, in order to ensure current reference tracking with a sinusoidal reference, the compensator performance was improved upon adding a resonant transfer function with a mid-pass filter characteristic. The performance of the proposed method was examined using different time domain simulations in the PSCAD/EMTDC environment. The results indicated that with the changes made to the control system and by determining proper current references, the performance of the overall system in removing the pulsating terms from the DC-link and the instantaneous output power was enhanced compared to the results of existing approach as in the literature.

Nomenclature

m_{abc}	Modulation indices in "*abc*" frame
m_d, m_q	Modulation indices in grid voltage oriented synchronous "*dq*" frame
V_{gabc}	Grid voltages in "*abc*" frame
i_{tabc}	Terminal currents in "*abc*" frame
i_{oabc}	Output currents in "*abc*" frame
V_{gdq}	Grid voltages in grid voltage oriented synchronous "*dq*" frame
i_{tdq}	Terminal currents in grid voltage oriented synchronous "*dq*" frame
i_{odq}	Output currents in grid voltage oriented synchronous "*dq*" frame
i^*_{td}, i^*_{tq}	Terminal current references in grid voltage oriented synchronous "*dq*" frame
V^*_{td}, V^*_{tq}	Terminal voltage references in grid voltage oriented synchronous "*dq*" frame produced by current controller
V_{DC}	DC link voltage
P_g	Instantaneous active power in the grid connection point
P_{in}	Instantaneous active power in converter terminal point
P_{out}	Instantaneous active power in DC loads side
ω, θ	Frequency and angular frequency produced by phase locked loop
R_f	Equivalent for input filter resistance and conduction and switching losses of the converter
L_f, C_f	Converter filter inductance, and capacitance
P^*_{ref}	Active power reference produced by DC-link voltage control loop
$Q*$	Reactive power reference
C_{DC}	DC link capacitor capacitance
abc/dq	"*abc*" to "*dq*" transformation

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