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 $Research \ Note$

Combination of Marx generator and capacitor diode voltage multiplier for pulsed power applications

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KEYWORDS

Pulsed power system; Pulsed electric field; Marx generator; Capacitor diode voltage multiplier. Abstract. Recently, the pulsed power and pulsed electric field systems have had wide applications in various industries. Therefore, using pulsed power generators that provide the advantages of compactness, high flexibility, high repetition rate, and cost efficiency, in addition to responding to the needs of the users, seems inevitable. In this study, a hybrid solid-state pulsed power generator is introduced that is modular and very flexible. This converter, which is a combination of Marx generator and capacitor diode voltage multiplier, is capable of producing high-voltage pulses with varying amplitudes at different frequencies. The advantages of high reliability, low cost, low weight, and simplicity of structure offer a wide area of applications of the proposed converter. In this paper, after introducing the proposed topology, its analytical design is described. Then, it is verified by the simulation results in MATLAB\SIMULINK and the measurement results derived from the experimental prototype in low voltages.

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1. Introduction

Nowadays, Pulsed Power Systems (PPSs) and Pulsed Electric Field (PEF) have found wide applications. These systems are used in medical applications [1,2], water and air cleaning [3,4], food treatment, synthesis of metal nanoparticles [5], etc. One of the most important components of PPS is pulsed power generator. Various generators are used in PPS. However, generators that use power semiconductor switches, having compactness, high pulse repetition rate, high reliability, high flexibility, and long life, have drawn considerable attention [6–8].

Various topologies of solid-state converters are

used in pulsed power applications such as the flyback, forward, push-pull, half-bridge, and full-bridge converters [9–14]. Capacitor Diode Voltage Multiplier (CDVM), Marx topology, Blumlein generator, and pulse network forming topology are also other topologies utilized in solid-state pulsed power generators [15– 18].

Among these topologies, Marx generator is the most common and reliable topology for pulsed power applications [19]. Functioning of the conventional Marx generator is based on charging capacitors in parallel and discharging them in series into the load. Figure 1 shows the basic topology of Marx generator circuit. During the charging mode, capacitors are charged in parallel. Then, the switches S_1, S_2, \dots, S_n are closed and the capacitors are discharged in series into the load. The output voltage is obtained by the following equation:

$$V_{load} = V_{c1} + V_{c2} + \dots + V_{cn}.$$
 (1)

The solid-state Marx modulators are a new class

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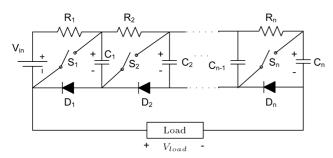


Figure 1. Marx generator.

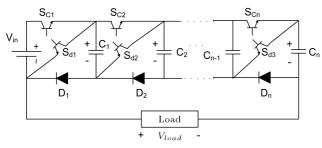


Figure 2. Solid-state Marx generator.

of modulators for the generation of high-voltage pulses [16]. Figure 2 shows an *n*-stage solid-state Marx generator. When switches $S_{c1}, S_{c2}, \dots, S_{cn}$ are closed and $S_{d1}, S_{d2}, \dots, S_{dn}$ are opened, the capacitors C_1, C_2, \dots, C_n are charged by the power supply through opening $S_{c1}, S_{c2}, \dots, S_{cn}$ and closing $S_{d1}, S_{d2}, \dots, S_{dn}$. These capacitors are discharged in series into the load.

Marx generators provide the ground for a wide area of research on the use of semiconductor switches. Acharya and Shrivastava employed a main Marx unit and a corrector Marx unit in their presented topology to reach a relatively flat pulse [16]. Elserougi et al. suggested charging the capacitors in Marx topology sequentially by a relatively low voltage supply [19]. Adachi et al. used a simple semi-conductor Marx generator with four stages and the switches employed in all the four stages were MOSFETs [20]. To increase the blocking voltage capability of each stage in Marx generators, series connection of the devices can be applied. Voltage distribution should be controlled either actively or by passive elements [21]. The topology suggested by Sakamoto and Akiyama was also based on a completely solid-state Marx-type circuit using fullbridge switch-capacitor cells series connection [22].

On the other hand, charging the capacitors to a relatively high voltage is one of the challenges of PPSs such as Marx generators. Any pulsed power application requires a capacitor charging system, which can charge capacitors fast to the target voltage. Therefore, production of such chargers with compact size, high power density, high efficiency, and safe performance has become an urgent need [23–25].

CDVMs with high efficiency, low voltage stress on diodes and capacitors, compactness, small size, simplicity, and low cost are the best option for high-voltage applications [8,26–28]. The basis of the performance of these inverters is charging the capacitors by low input voltage in a specific time interval and discharging the stored energy to the load in a short time. In two basic CDVM topologies, the output voltage comes from either a series of capacitors or only a single capacitor. Figure 3 shows samples of these topologies.

Many papers have been published on CDVM topology in non-pulsed power applications [29-32]. There are also a number of papers on the use of CDVM circuit in pulsed power applications. Redondo used the CDVM circuit fed by the AC grid, where the output voltage came from a single capacitor [8]. A combination of a boost DC-DC converter and CDVM fed by AC low voltage and low frequency for water treatment application was also proposed [27]. Zabihi et al. designed an LC resonant circuit supplied by an H-bridge inverter [33]. A simple one-stage Cockcroft-Walton CDVM circuit was also connected in cascade to the capacitor in the LC circuit in order to escalate the amplitude of voltage oscillation and to rectify the oscillating voltage to dc voltage. Mao et al. used the Hbridge inverter along with CDVM aimed at improving the rise time and decreasing the response time [34].

In all of the aforementioned CDVM topologies, increase in voltage is achieved by increasing the number of stages. In these converters, accordingly, the voltages of the semiconductor and the capacitor are increased stage by stage. This is considered as the main drawback of these topologies as it imposes limitations to increas-

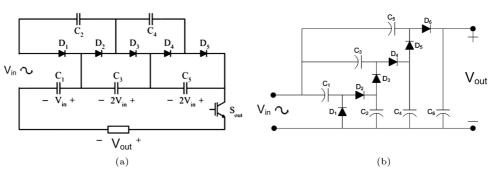


Figure 3. Two types of capacitor diode voltage multipliers.

ing the output voltage. Rezanejad et al. proposed a new topology of CDVM by adding semiconductor switches to CDVM circuit [15]. In this topology, which was fed by AC grid, in discharging mode, a number of capacitors in CDVM circuit were connected in series. Rezanejad et al. also proposed a new topology by combining CDVM and resonant circuit [35]. In this topology, a number of CDVM capacitors were also connected in series during the discharging mode. Although higher voltages were obtained in these structures, there were still restrictions on the number of stages. These structures were not completely modular as well.

This paper proposes a novel topology that has the advantages of Marx and CDVM topologies. The proposed generator has a modular structure that can be fed by a low DC or AC input voltage. Input voltage is multiplied by CDVM modules and output capacitors are charged to a relatively high voltage. Then, the output capacitors are connected in series to discharge into the load. After introducing the structure of the proposed generator, its performance with two modules of one-stage multiplier is described. Finally, the proposed approach will be experimentally validated in order to confirm its viability.

This study is an extension of the work presented by Kebriaei et al. [36]. Here, some switches are removed from the previous topology for making improvements in it. In this paper, the design process is described and switching losses are analyzed. Removing a number of switches will have the following benefits:

- By removing each switch, its losses are also eliminated and efficiency of the generator increases;
- Reducing switches simplifies topology as much as possible;
- In the modified topology with fewer switches, smaller solid-state driver circuit will be required and the control system will be simpler;
- The final cost of the modified generator will be reduced.

2. Combination of Marx and CDVM

2.1. Proposed topology

Figure 4 shows the schematics of the proposed generator, which is a combination of Marx generator and CDVM. As the figure demonstrates, this topology is completely modular and very flexible. It consists of an AC-DC converter, a full-bridge converter, m modules of *n*-stage voltage multipliers, (2m - 1) power electronic switches, and a controller. Each voltage multiplier consists of relatively-low-voltage diodes and capacitors. $S_{m1}, S_{m2}, \dots, S_{mm}$ are charging switches and $S_{h1}, S_{h2}, \dots, S_{h(m-1)}$ are pulsing switches. When the charging switches are closed and pulsing switches are opened, the capacitor can be charged. When charging switches are opened and pulsing switches are closed, the output voltage can be obtained from the following equation:

$$V_{load} = V_{c1n} + V_{c2n} + \dots + V_{cmn}.$$
 (2)

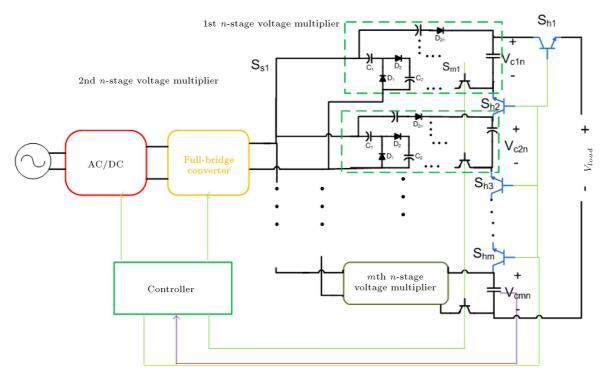


Figure 4. Schematics of the proposed topology.

The output voltage is determined by the following factors:

- Number of voltage multipliers (m);
- Stage of voltage multipliers (n);
- Control of the full-bridge converter;
- Output voltage of AC-DC converter.

In the proposed model, which is shown in Figure 4, mis the number of voltage multipliers or the number of Marx generator stages and n is the number of stages of voltage multipliers. The rating of Marx generator (the voltage of output capacitor of each voltage multiplier) depends on n and the voltage of input power source, and it is restricted by rating of output capacitors and discharging switches. The output frequency can be controlled by controlling the full-bridge converter and switching the charging and pulsing switches. It is obvious that AC-DC and full-bridge converters can be removed and low-voltage, low-frequency supply is directly connected to the voltage multipliers. In this case, however, the output voltage will become uncontrollable and high-output frequency cannot be achieved.

2.2. Functional modes

To introduce the principles of the operation of the circuit, a simple circuit of the proposed topology with two modules of one-stage voltage multiplier is studied. In this circuit, the full-bridge converter is connected to an inductor before applying the voltage multiplier modules. This creates a resonant circuit with the voltage multiplier capacitors and the full-bridge converter can operate in a Zero-Current Switching (ZCS) mode. The resonant circuit used in this structure can reduce the stress on switching element and increase the output voltage [37]. It has three switching modes, as shown in Figures 5–7. These modes are described in detail in the following. V_{dc} in these figures is the output voltage of AC-DC converter. The results for the presented circuit in these figures can be extended to more modules and stages:

1. The first switching mode. As shown in Figure 5, S_{m1} and S_{m2} are on and D_{12} and D_{22} conduct current. In this mode, the inductor L and capacitors C_{11} , C_{12} , C_{21} , and C_{22} make the resonant circuit. For simplicity, the capacities of the capacitors are considered to be equal. The resonant frequency can be obtained by the following equation:

$$C_{eq1} = \frac{C_{12}C_{11}}{C_{11} + C_{12}} + \frac{C_{22}C_{21}}{C_{21} + C_{22}} = C,$$
 (3)

$$\omega_{r1} = \frac{1}{\sqrt{LC_{eq1}}} = \frac{1}{\sqrt{LC}}.$$
 (4)

In the above equation, ω_{r1} is resonant frequency

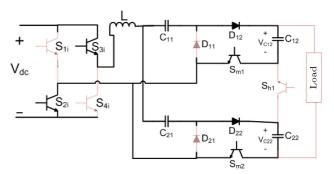


Figure 5. The first switching mode.

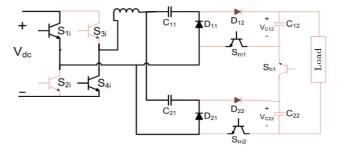


Figure 6. The second switching mode.

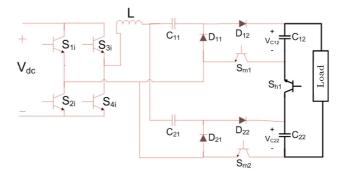


Figure 7. Switching status in discharging mode.

(rad/s) in the first switching mode. With the initial zero conditions;

$$V_{C_{12}}(t) = V_{C_{22}}(t) = \frac{1}{2} V_{C_{eq1}}(t)$$
$$= \frac{1}{2} V_{dc}(1 - \cos(\omega_{r1}t)).$$
(5)

It is clear that at time $t = \pi \sqrt{LC}$, voltage on all capacitors will be equal to V_{dc} and inductor current will be zero;

2. The second switching mode. Status of power switches and diodes in this mode is shown in Figure 6. D_{12} and D_{22} are turned off and D_{11} and D_{21} are turned on. The resonant circuit in this mode includes the inductor L and capacitors C_{11} and C_{21} . The resonant frequency is calculated as follows:

$$C_{eq2} = C_{11} + C_{21} = 2C, (6)$$

$$f_{r2} = \frac{1}{2\pi\sqrt{LC_{eq2}}} = \frac{1}{2\pi\sqrt{2LC}},$$
(7)

where f_{r2} is the resonant frequency in the second switching mode. In this mode, the voltages of C_{12} and C_{22} do not change, but after $\pi\sqrt{2LC}$ seconds, the other capacitor voltages reach their maximum value $(3V_{dc})$.

After this switching mode, the first switching mode should be repeated. With the new initial values, the following holds for this state:

$$V_{C_{12}}(t) = V_{C_{22}}(t) = \frac{3}{2} V_{dc}(1 - \cos(\omega_{r1}t)) + V_{dc}.$$
 (8)

After $\pi\sqrt{LC}$ seconds, the voltages of C_{12} and C_{22} reach $4V_{dc}$. The minimum required time for the output capacitor voltages to reach their maximum value $(4V_{dc})$ can be calculated as follows:

$$T_{c,\min} = \pi \sqrt{LC} + \pi \sqrt{2LC} + \pi \sqrt{LC}$$
$$= 2\pi \sqrt{LC} + \pi \sqrt{2LC}.$$
(9)

As shown in Figure 1, resistors are used in the conventional Marx generator to charge the capacitors in parallel. The resistance should be high enough to prevent an objectionable loss of energy during the erected or discharge mode. The high value of resistance dictates a long charging period [38]. Tc, min is the time taken to charge the Marx generator in the proposed model. It is quite obvious that the charging time in this model is less than that in the conventional Marx.

3. The third switching mode (discharging mode). For pulsing, S_{m1} and S_{m2} are turned off and S_{h1} turned on, as shown in Figure 7. The output voltage can be obtained from the following equation:

$$V_{load} = V_{C12} + V_{C22} = 8V_{dc}, (10)$$

where V_{C12} and V_{C22} are the output voltages of multipliers and V_{load} is the load voltage. For the *n*-stage voltage multiplier, the output voltage of each multiplier after the last switching step reaches $4nV_{dc}$. For *m* modules of *n*-stage voltage multiplier, the maximum output voltage can be written as follows:

$$V_{load} = 4mnV_{dc}.$$
(11)

2.3. Design considerations

The proposed generator produces exponential pulses in resistance load. If all the energy stored in the output capacitors is discharged, the energy of the output pulse is obtained by the following equation:

$$E_{pulse} = \frac{C_{12}C_{22}}{2(C_{12} + C_{22})} \left(V_{C12} + V_{C22} \right)^2 = \frac{C}{4} (V_{load})^2, (12)$$

where E_{pulse} is the energy in Joules. In practice and for system design, the capacitance of circuit is obtained by Eq. (12) with regard to the voltage and the amount of energy required per pulse. The maximum achievable output frequency by the generator is obtained by the following equation;

$$f_{\max} = \frac{1}{T_{c,\min} + T_{load} + T_{delay}},\tag{13}$$

where T_{load} is pulse duration and T_{delay} is the required delay time both in seconds. $T_{c,\min}$ is obtained by Eq. (13) with the desired pulsed repetition rate and pulse duration. The value of inductance, L, is obtained from Eq. (9).

The power losses on the solid-state switches and diodes are an issue that should also be considered in the design. Total power loss of each solid-state element is the sum of turn-on and turn-off losses (switching losses), conduction losses, and off-state losses. Neglecting the losses in the off state, the total power loss is given by:

$$P_l = P_s + P_c, \tag{14}$$

where P_s is the switching loss and P_c is the conduction loss. During the full-bridge switches, the switching loss is negligible because turn-on and turn-off commutation occurs with ZCS. For these switches, the power loss can be obtained by the following equation:

$$P_{lb} = 2f \left(\int_{0}^{\sqrt{LC}} I_{1L}(t) V_{sat,b} dt + \int_{0}^{\sqrt{2LC}} I_{2L}(t) V_{sat,b} dt + \int_{0}^{\sqrt{LC}} I_{3L}(t) V_{sat,b} dt \right),$$
(15)

where f is the pulsed power generator frequency, $I_{1L}(t)$ is the maximum inductor current in the first mode, $V_{sat,b}$ is the saturation voltage of full-bridge switches, $I_{2L}(t)$ is the maximum inductor current in the second mode, and $I_{3L}(t)$ is the maximum inductor current in the first mode for the second time. Since the two switches are turned on in each mode, the expression is multiplied by 2. In a similar way, for the losses on the CDVM diodes, S_{m1} and S_{m2} can be written as:

$$P_{ld} = 2f \left(\int_{0}^{\sqrt{LC}} \frac{1}{2} I_{1L}(t) V_{on,d} dt + \int_{0}^{\sqrt{2LC}} \frac{1}{2} I_{2L}(t) V_{on,d} dt + \int_{0}^{\sqrt{LC}} \frac{1}{2} I_{3L}(t) V_{on,d} dt \right),$$
(16)

$$P_{lm} = 2f \left(\int_{0}^{\sqrt{LC}} \frac{1}{2} I_{1L}(t) V_{sat,m} dt + \int_{0}^{\sqrt{LC}} \frac{1}{2} I_{3L}(t) V_{sat,m} dt \right) (17)$$

In the above equations, P_{ld} and P_{lm} are the total power loss on the CDVM diodes and total power loss on S_{m1} and S_{m2} , respectively. $V_{on,d}$ is the on-state voltage of diodes and $V_{sat,m}$ is the saturation voltage in the on state of S_{m1} and S_{m2} .

During the Marx switching (S_{h1}) , having a resistance load, the power losses are given by:

$$P_{lh} = P_{sh} + P_{ch}, \tag{18}$$

$$P_{sh} = fE_s, \tag{19}$$

$$P_{ch} = f \int_{0}^{t_p} V_{sat,h} \frac{V_{load}(t)}{R_{load}} dt, \qquad (20)$$

where E_s is the switching energy loss provided by the manufactory and $V_{sat,h}$ is the saturation voltage in the on state of S_{h1} .

3. Simulation and experimental results

To evaluate the performance of the proposed topology, the values in Table 1 were used for simulation in MAT-LAB/SIMULINK. Simulation results for the inductor current, the capacitor voltage, and the output voltage are shown in Figure 8. It is clear from the inductor current that switching is done in zero current. At the end of any cycle, the voltage of output capacitor of each voltage multiplier reaches $4V_{dc}$ and the output voltage, which is the sum of the voltages of the output capacitors at the start of pulsing, is equal to $8V_{dc}$.

By reducing the duration of the first and second switching modes, different output voltages can be achieved. However, the maximum output voltage by this circuit is $8V_{dc}$.

A setup prototype is developed to practically investigate the concept of this circuit. The prototype is composed of a full-bridge converter, an inductor, two one-stage voltage multipliers, semiconductor switches as shown in Figure 5, a resistive load, MOSFET and Insulated Gate Bipolar Transistor (IGBT) drivers, isolated DC-DC converters for drivers, a DC power supply, and a microcontroller board. The microcontroller controls the full-bridge converter so that switching is done in zero current. Low-rating MOSFETs are used as power switches in the full-bridge converter and conventional IGBTs such as IXGH40N60 are used in its structure. The component specifications are addressed in Table 1. In the prototype, a simple plasma load model has been used. This model is a resistance in the range of a few ohms that represents the load resistivity in the period of the plasma reaction [39].

The experimental test is conducted in the lowvoltage range because of the voltage restrictions on the input DC power supply and the measurement instruments. The input voltage is adjusted to 28 V. The results of inductor current and capacitor voltage are shown in Figure 9 and the output voltage is shown in Figure 10. V_{C12} and V_{C22} reach 104 V and the output pulse frequency is 4.17 kHz. As these measurement results show, the capacitor voltage is

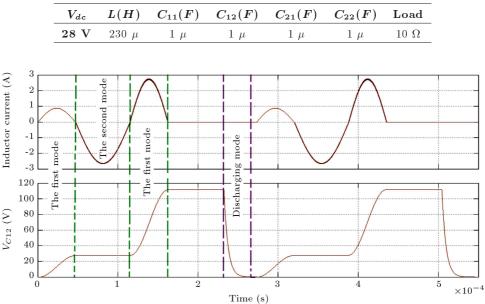


 Table 1. Circuit parameters in simulation.

Figure 8. Simulation results for inductor current and capacitor voltage.

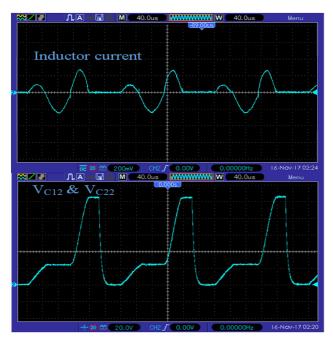


Figure 9. Experimental results for inductor current and V_{C12} .

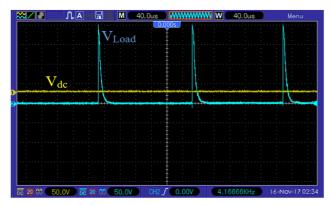


Figure 10. Output voltage of experimental hybrid solid state pulsed power generator.

almost four times the input voltage and the summation of voltages across C_{12} and C_{22} appears across the load. The output voltage is almost eight times the input voltage. There is a difference of almost 8.5% between this measured voltage and the expected voltage in ideal case ($8V_{dc}$), which is due to non-ideal characteristics of elements such as forward voltage of diodes, saturation voltage of switches, and resistance of elements.

This simplified model can be extended to more stages and more modules, and the generated voltage can be increased. When designing a higher-voltage generator, the Marx switches $(S_{h1}, S_{h2}, S_{h3}, \cdots)$ increase and it is required that these switches act simultaneously. It is possible to use diodes in each Marx stage that can bypass the switch and capacitor in that specific stage (Figure 11). In this way, if a switch cannot be turned on in time, its diode

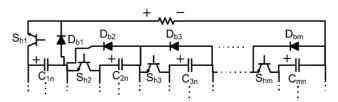


Figure 11. Output modifications for deal to high voltages in asynchronous operation of Marx switches.

provides a freewheeling path so that the switch does not cause significant damage at high voltages. Also, it is necessary to use isolated or optocoupler driver and isolated power supply for control and driver circuits to avoid considerable damage to the circuits at high voltages.

4. Conclusion

In this paper, a new pulsed power generator based on the combination of Marx topology and capacitor diode voltage multiplier topology has been proposed for wide pulsed power applications. This topology is completely modular and very flexible. The maximum output voltage of this combination is dependent on the number of multipliers, the number of modules, and input voltage while the output voltage can be changed easily. Therefore, the maximum output voltage can be easily increased by adding modules. Conventional solid-state switches and capacitors can be used in the proposed topology, while high-voltage and high-frequency pulses are accessible. Simulations and experimental tests were carried out and the obtained results verified proper performance and operation of the proposed generator.

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