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Research Note

A high-performance full-wave rectifier using a single CCII-, two diodes, and two resistors

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Abstract. In this paper, a voltage-mode full-wave rectifier circuit is proposed. The proposed full-wave rectifier circuit consists of only a single negative-type second-generation current conveyor, two diodes, and two matched resistors. The proposed circuit, without requiring any external bias voltages and currents, has a simple structure using a minimum number of active and passive components. It is implemented with AMS 0.35 μm technology operating with $\pm$1.65 V. Computer simulation and experimental results are included to verify the theory.

1. Introduction

Full-wave rectification is an essential subject in a number of areas such as control engineering, analog signal processing, telecommunication, instrumentation, and measurement. There are a number of full-wave rectifier circuits available in the related open literature [1-23]. Simple rectifiers, consisting of only diodes and passive elements, operate inaccurately due to the threshold voltage of the diodes. Thus, active elements are employed for high-precision rectification [2]. In general, rectifier circuits can be achieved with diodes, active building blocks, such as second-generation current conveyors (CCIIs), Operational Amplifiers (Op-Amps), etc. or both. The full-wave rectifiers, including Op-Amps, diodes, and resistors, have been proposed in open literature [3-5,18,19]. However, the most important problem with the full-wave rectifiers using Op-Amps and diodes is the well-known distortion due to the diode commutation and finite slew rate of the Op-Amp [5,6]. This distortion is growing for low-level signals. Also, the operating frequency of the rectifier is restricted by the finite gain bandwidth product of the employed Op-Amps [7]. A precise full-wave rectifier with low operating frequency using Op-Amps is given in [4]. To increase the operating frequency, Current-Mode (CM) active elements, such as CCIIs, can be used instead of Op-amps; thus, diodes are switched ON and OFF with output currents of these elements [7,8]. Operational Trans-conductance Amplifiers (OTAs) are also used for full-wave rectification. The most important advantage of this idea is designing the circuit with only active circuit blocks [9]. Nevertheless, trans-conductance of the OTA is adjusted with the input signal of the circuit. Another OTA-based full-wave rectifier circuit given in [10] uses two extra CMOS transistors and a resistor. Although, as an interesting approach, the rectifier circuit in [11] employs Current Followers (CFs), it needs extra four diodes and three resistors. Full-wave rectifier circuits, consisting of CCIIs and a Dual-X Current Conveyor (DXCCII), have been respectively proposed in [12,13] where NMOS

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transistors are used for switching purposes rather than for diodes. Also, a Voltage-Mode (VM) full-wave rectifier, composed of two CCIIs, has been reported in [14]. A VM full-wave rectifier proposed in [15] uses one CCII and a number of MOS transistors. VM full-wave rectifier topologies of [16] employ one CCII and one DXCCII. Also, a VM full-wave rectifier circuit, consisting of two dual output CCIIs, have been proposed in [17]. Op-Amp based full-wave rectifiers use at least two active components, at least three resistors requiring at least one matching condition and two P-N junction diodes [3-5,18,19].

In the literature, a CM full-wave rectifier employing two-diode, two CCIIs, and one DC voltage source has been presented in [2] and another CM full-wave rectifier configuration consisting of four diodes and a single Current Differencing Trans-conductance Amplifier (CDTA) has been given in [20]. A full-wave rectifier structure composed of a CDTA and two Schottky diodes has been proposed in [21]. CM full-wave rectifier configurations using only CMOS transistors have been proposed in [22,23]. Moreover, there are some CM full-wave rectifier circuits given in [6,11].

Many full-wave rectifiers reported in literature aim to provide high-operation frequency for low-level signals. However, most of these circuits operating in VM suffer from using at least four diodes and/or two active elements [2-5,7-9,11,12,14,16,17].

A new full-wave rectifier circuit is proposed in this study which operates in VM and employs a single negative-type CCII (CCII-), two diodes, and two resistors. The proposed full-wave rectifier structure and the employed CCII- are implemented with AMS 0.35 μm CMOS technology parameters with $\pm$1.65 V DC power supply voltages. Non-ideal analysis of the proposed rectifier is also investigated. Some experimental and computer simulation results are included to confirm the theory.

This paper is organized as follows: After introduction, the CCII which is used to construct the full-wave rectifier structure is discussed in Section 2. The suggested full-wave rectifier circuit is treated in Section 3. Experimental and simulation results of the full-wave rectifier circuit are given in Section 4. Some conclusion remarks are finally discussed in Section 5.

2. Current conveyor

The CCII demonstrated in Figure 1 is an active device with high-impedance current output terminal, Z, high-impedance voltage input terminal, Y, and low-impedance current input terminal, X. The characteristics of the positive/ negative type CCII (CCII+/CCII–) are given as:

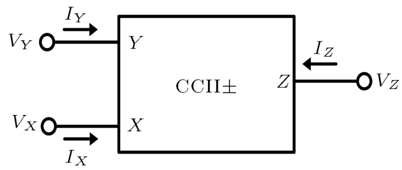


Figure 1. Symbol of the second-generation current conveyor.

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} \beta & R_X + sL_X & 0 \\ sC_Y & 0 & 0 \\ 0 & \pm\alpha & sC_Z + 1/R_Z \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}, \quad (1)$$

where α and β, which are ideally equal to unity, are current and voltage gains, respectively. In addition, R_X, L_X, C_Z, and R_Z are parasitic elements at their respective terminals. So, ideally, $V_X = V_Y$, $I_Y = 0$, and $I_Z = -I_X$ for negative-type CCII (CCII-), while $I_Z = I_X$ for positive-type one (CCII+).

3. The proposed voltage-mode rectifier circuit

The proposed full-wave rectifier using a single CCII-, two diodes, and two matched resistors is depicted in Figure 2.

The circuit operation with $R_2 \geq R_1$ can be expressed in two different cases. First, $V_{\text{in}} > 0$, $I_R > 0$, and $I_Z > 0$, and then diode D_1 is in ON and D_2 is in OFF states; so, $V_{\text{out}} = V_{\text{in}}$. Second, $V_{\text{in}} < 0$, $I_R < 0$, and $I_Z < 0$, and then diode D_1 is in OFF and D_2 is in ON states; the following equation can be written as follows:

$$\frac{V_{\text{out}} - V_{\text{in}}}{R_2} = -I_R = -\frac{V_{\text{in}}}{R_1} \qquad (\text{if } V_{\text{in}} < 0), \quad (2)$$

or equivalently:

$$V_{\text{out}} = \left(1 - \frac{R_2}{R_1}\right) V_{\text{in}} \qquad (\text{if } V_{\text{in}} < 0). \quad (3)$$

If $R_2 = 2R_1$ is chosen, Eq. (3) turns to:

$$V_{\text{out}} = -V_{\text{in}} \qquad (\text{if } V_{\text{in}} < 0). \quad (4)$$

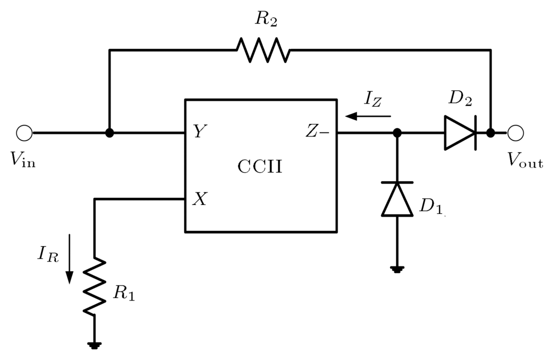


Figure 2. The proposed full-wave rectifier circuit.

In other words, the output voltage is ideally expressed as:

$$V_{\text{out}} = |V_{\text{in}}|. \tag{5}$$

It can be realized that $V_{\text{out}} = V_{\text{in}}$ even under non-ideal gain effects for $V_{\text{in}} > 0$, but for $V_{\text{in}} < 0$, $R_2 = 2R_1$, V_{out} is evaluated under non-ideal gain effects as follows:

$$V_{\text{out}} = (1 - 2\alpha\beta)V_{\text{in}} \qquad (\text{if } V_{\text{in}} < 0). \tag{6}$$

However, as it can be seen from Eq. (6) that for negative input signals, the performance of the rectifier is affected by the non-ideal gains of the CCII-. If only X terminal parasitic impedance effects with the ideal gains and $R_2 = 2R_1 = 2R$ for simplicity are taken into account, the output can be expressed as:

$$V_{\text{out}} = \begin{cases} V_{\text{in}} & \text{if } V_{\text{in}} > 0 \\ V_{\text{in}}\left(1 - \frac{2R}{R+R_X+sL_X}\right) & \text{if } V_{\text{in}} < 0 \end{cases} \tag{7}$$

For proper operation:

$$\omega L_X + R_X \ll R \qquad (\text{if } V_{\text{in}} < 0), \tag{8}$$

must be chosen. Likewise, if only Z terminal parasitic impedance effects are taken into account, the output can be given by:

$$V_{\text{out}} = \begin{cases} V_{\text{in}} & \text{if } V_{\text{in}} > 0 \\ -\frac{V_{\text{in}}}{1+sC_Z 2R+\frac{2R}{R_Z}} & \text{if } V_{\text{in}} < 0 \end{cases} \tag{9}$$

For proper operation:

$$\omega C_Z 2R + \frac{2R}{R_Z} \ll 1 \qquad (\text{if } V_{\text{in}} < 0), \tag{10}$$

must be chosen. From Eqs. (8) and (10), the useful frequency range is found as follows:

$$f \leq \frac{0.1}{2\pi} \min\left(\frac{R - R_X}{L_X}, \frac{1 - \frac{2R}{R_Z}}{C_Z 2R}\right) \qquad (\text{if } V_{\text{in}} < 0). \tag{11}$$

Note that as the employed resistors have to be matched, R_X, L_X, and C_Z should be as small as possible and R_Z should be as large as possible in order to minimize the non-ideal effects. On the other hand, if only diode resistors and R_Z are taken into account, $V_{\text{out}} = V_{\text{in}}$ for $V_{\text{in}} > 0$. However, for $V_{\text{in}} < 0$, the following output voltage is obtained:

$$V_{\text{out}} = -\frac{R_Z - R_{d2}}{R_Z + 2R + R_{d2}} V_{\text{in}}. \tag{12}$$

Here, R_{d2} is the parasitic resistor of D_2 which is modeled as an ideal diode series with a parasitic resistor.

4. Test results of the CCII- and full-wave rectifier

For the simulation and experimental tests, we used the CCII implemented on an IC classifier circuit previously reported. The implemented CCII has both positive and negative Z outputs. Also, 1N4148 diodes are used in both simulation and experimental tests of the proposed circuit. The employed CCII has been fabricated with CMOS AMS 0.35 μm process technology. The area of the CCII circuit in the classifier IC is 100 $\mu\text{m} \times 80$ μm. The parasitic element values of the CCII- are given in Table 1. To show the performance of the CCII- circuit working with ± 1.65 V and $V_{\text{bias}} = 0.8$ V, $V_Z - V_X$ (or equivalently $I_Z - I_X$) and $V_X - V_Y$ characteristics have been extracted and the results are given in Figures 3 and 4, respectively.

Table 1. The parasitic element values of the CCII-.

Parasitic symbol	Value
R_X	2 Ω
L_X	5 μH
R_Z	15.5 kΩ
C_Z	0.014 pF
C_Y	0.044 pF

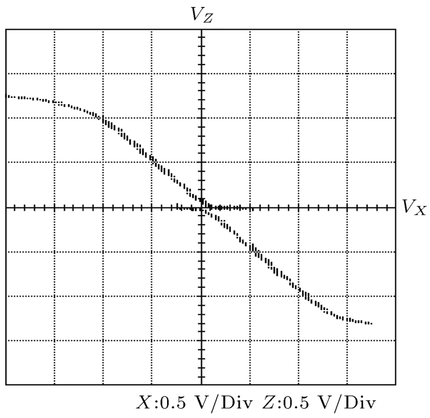


Figure 3. $V_Z - V_X$ characteristics of the CCII-.

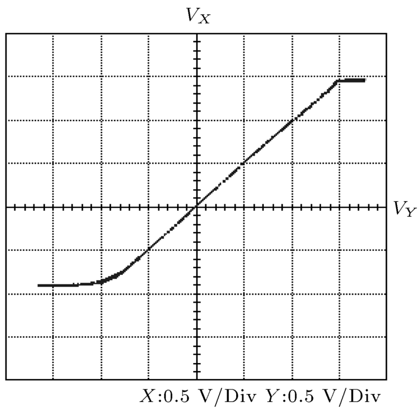


Figure 4. $V_X - V_Y$ characteristics of the CCII-.

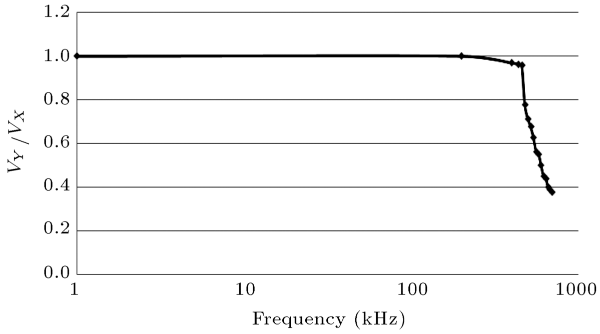


Figure 5. Experimental results for V_X/V_Y frequency response of the CCII-.

To obtain $I_Z - I_X$ characteristics, equal resistors of 10 kΩ are connected to X and Z terminals of the CCII-, and a DC voltage source changing from –1.5 V to 1.5 V is applied to port Y. Since X and Y scales on the oscilloscope screen are chosen as 0.5 V/Div and 0.5 V/Div, it can be realized that $I_Z - I_X$ characteristics of the CCII- are operating in the range of –100 μA to 125 μA. A similar approach is also used to obtain $V_X - V_Y$ characteristics of the CCII-. It can be seen from Figure 4 that voltage V_X can follow voltage V_Y from –0.75 V to 1.5 V. In addition, the frequency characteristic of the voltage gain of the CCII- is shown in Figure 5, where the test result data are collected from the measured values. f-3dB frequency of voltage gain V_X/V_Y is 600 kHz. The important performance parameters of the full-wave rectifier circuits are the DC value transfer (p_{DC}) and RMS error (p_{RMS}), which are used to show the accuracy of the rectifier. These values can be respectively obtained as follows:

$$p_{\mathrm{DC}} = \frac{\int_T V_{oa}(t)dt}{\int_T V_{oi}(t)dt}, \tag{13}$$

$$p_{\mathrm{RMS}} = \sqrt{\frac{\int_T [V_{oa}(t) - V_{oi}(t)]^2 dt}{\int_T V_{oi}^2(t)dt}}, \tag{14}$$

where $V_{oa}(t)$ and $V_{oi}(t)$ represent the actual and the ideal output values of the rectifier.

In the ideal case, the values of p_{DC} and p_{RMS} should be 1 and 0, respectively. The simulations and experimental results of p_{DC} and p_{RMS} are shown in Figures 6 and 7, respectively. It can be seen that as the frequency of the full-wave rectifier increases, the non-ideal effects cause the value of p_{DC} to decrease and the value of p_{RMS} to increase. The time-domain simulation result of the proposed full-wave rectifier circuit is shown in Figure 8. Resistors $R_2 = 20$ kΩ and $R_1 = 10$ kΩ in Figure 2 are chosen externally. The simulation given in Figure 8 is performed for a sinusoidal input signal with 200 mV peak value and frequency of 40 kHz. The simulation and experimental results of the input-output DC transfer characteristic of the proposed full-wave rectifier are shown in Figure 9(a) and (b), respectively. It can be seen that the circuit has a restriction on the negative input voltages approximately obtained as −370 mV from simulation and –220 mV from practical test. It should be mentioned that there is no limitation to the positive input signals since the output is directly connected to the input through resistor R_2.

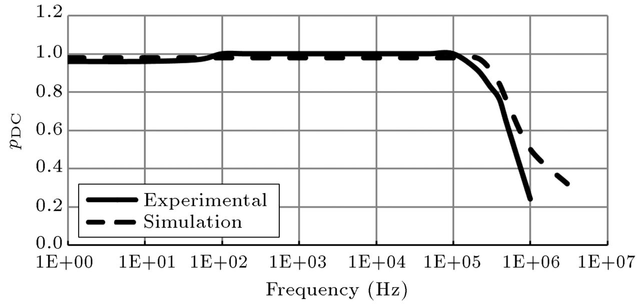


Figure 6. Simulation and experimentals result of the full-wave rectifier circuit for p_{DC}.

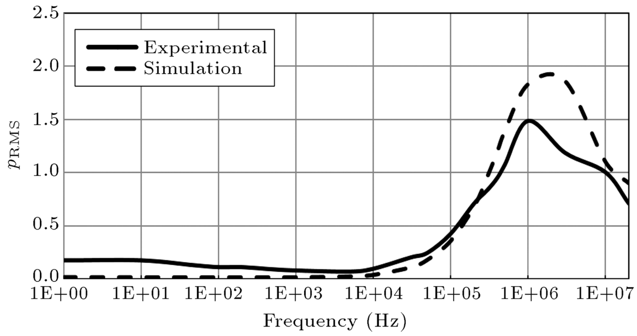


Figure 7. Simulation and experimental results of the full-wave rectifier circuit for p_{RMS}.

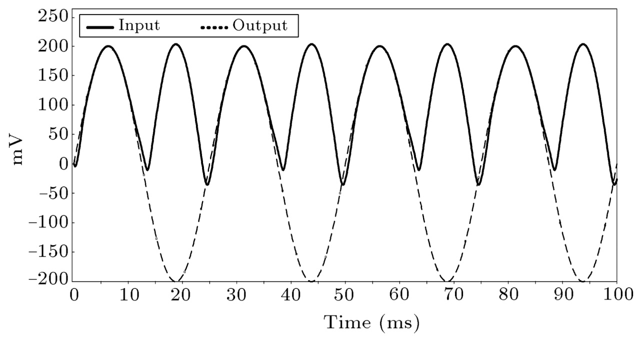
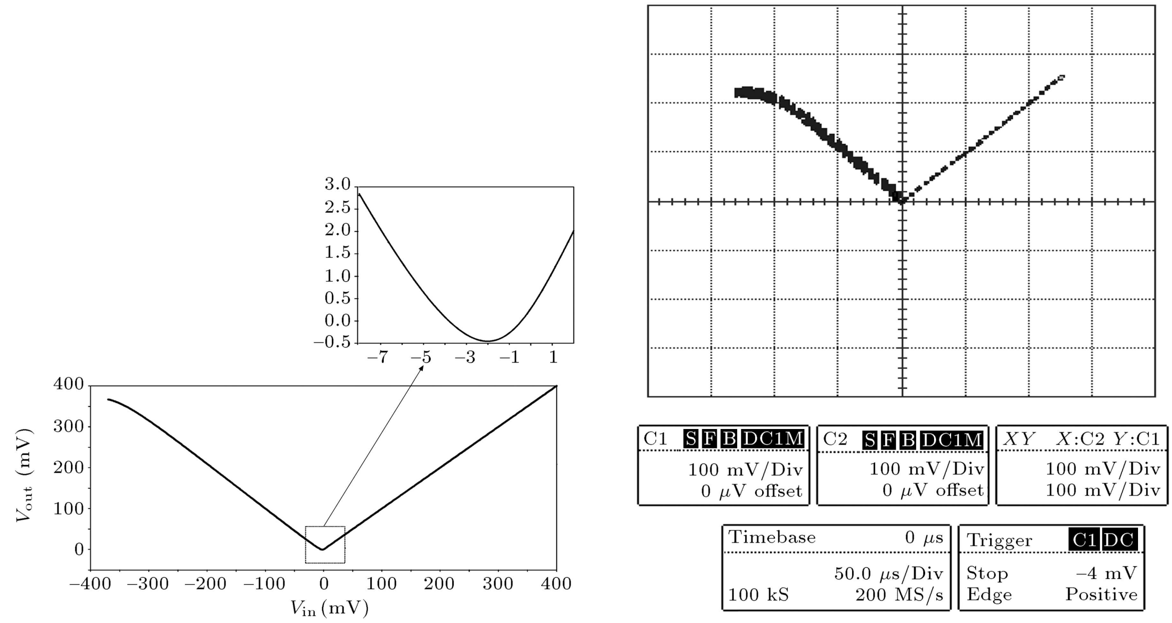


Figure 8. Time-domain response of the developed full-wave rectifier.

Nevertheless, the input-output DC transfer characteristic of the proposed full-wave rectifier is not symmetrical due to non-idealities of the CCII-. In addition, it can be seen from Figure 9(b) that the offset voltage is approximately zero; thus, the proposed rectifier can work with very small input signals. It operates properly with input signals lower than a few mV.

The proposed full-wave rectifier is also experimentally tested using the CCII of the classifier circuit.



(a) (b)

Figure 9. DC transfer characteristics ($V_{out} - V_{in}$) of the suggested full-wave rectifier structure: (a) simulation result, and (b) experimental result (Y-axis = V_{out}, X-axis = V_{in}).

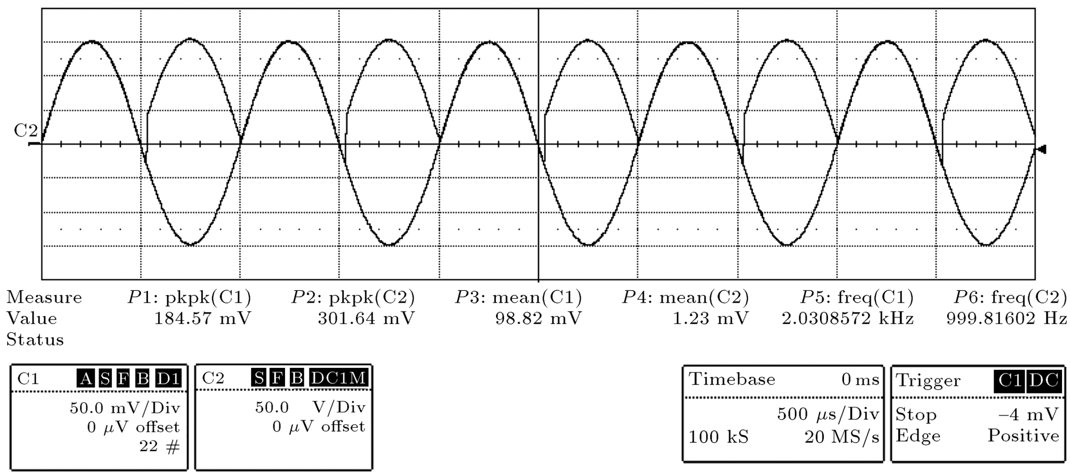


Figure 10. Input/output waveforms for input frequency of 1 kHz.

Sinusoidal voltages with frequencies of 1 kHz and 10 kHz are applied to the input of the circuit, and the rectified output signal is observed as shown in Figures 10 and 11, respectively. A comparison of the previously published rectifier circuits [1-5,7-14] and the proposed one is given in Table 2.

It is observed from simulation and experimental results that they agree quite well with the claimed theory, whereas the discrepancy among them can be attributed to parasitics of the board used in experimental test as well as non-idealities of the CCII- and diodes. It should be mentioned that the proposed circuit has no high input and low output impedances, so buffer stage may be required at its input or output. However, if the proposed circuit is used in the middle stage of an electronic device with a low output impedance from the previous stage and high input impedance from the next stage, there is no need to use buffers. Meanwhile, if necessary, a voltage buffer can be easily realized by using only two MOS transistors [24].

5. Conclusion

In this paper, a new full-wave rectifier circuit operating in VM is proposed. The proposed full-wave rectifier circuit without requiring any external bias voltages and currents is composed of only a CCII-, two diodes, and two matched resistors. The proposed full-wave rectifier structure has been designed using MENTOR software and manufactured with CMOS AMS 0.35 μm

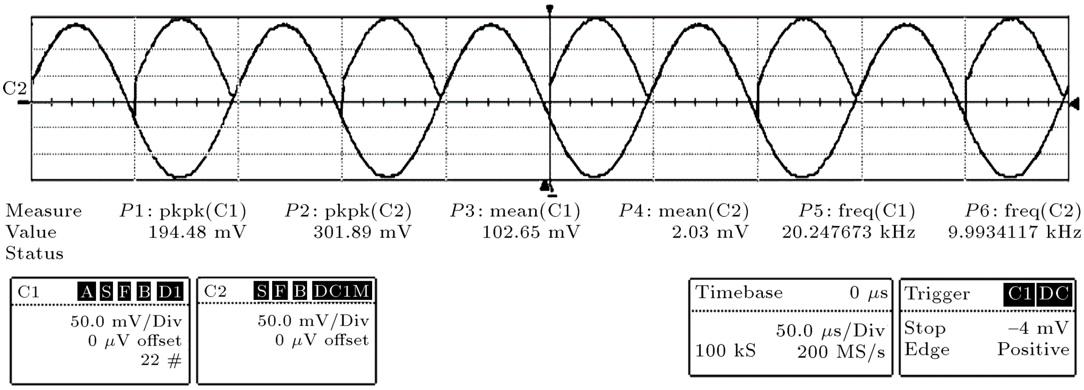


Figure 11. Input/output waveforms for input frequency of 10 kHz.

Table 2. Comparison of the rectifier circuits.

References	[1]	[2]	[3]	[4]	[5]	[7]	[8]	[9]	[10]	[11]	[12]	[13]	[14]	**This work**
# of active elements (# of diodes)	3 Trans-conductor 1 NMOS 1 PMOS (0)	2 CCII (2)	2 OA 1 CCII (2)	2 OA (2)	1 CCII 1 OA (2)	2 CCII (4)	2 CCII (4)	5 OTA (0)	1 OTA 1 NMOS 1PMOS (0)	1 CF (4)	2 CCII 3 NMOS (0)	1 DXCCII 3 NMOS	2 CCII (2)	1 CCII- (2)
High input/ low output impedance	Yes/ No	Yes/ No	No/ Yes	No/ Yes	Yes/ Yes	Yes/ No	Yes/ No	Yes/ No	Yes/ No	No/ No	No/ No	Yes/ No	Yes/ No	No/ No
# of resistors	1	3	3	7	3	2	2	2	1	3	0	0	3	2
Resistive matching requirement	No	No	Yes	Yes	Yes	Yes	No	No	No	No	No	No	Yes	Yes
Supply voltages	±5 V	±1.5 V	NA*	NA	NA	±5 V	NA	±15 V	±5 V	±10 V	±1.25 V	±1.25 V	±12 V	±1.65 V

*NA: Not Available

technology parameters. The performances of the employed CCII- as well as the proposed full-wave rectifier circuit are investigated through simulation and experimental tests which confirm the theory well as desired. Nevertheless, the difference among the ideal, simulation, and experimental results arises from parasitics of the board used in experimental test along with non-idealities of the CCII- and diodes.

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Biographies

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Erkan Yuce was born in 1969 in Nigde, Turkey. He received BSc degree from Middle East Technical University, MSc degree from Pamukkale University, and PhD degree from Bogazici University all in Electrical and Electronics Engineering in 1994, 1998, and 2006, respectively. He is currently an Associative Professor at the Electrical and Electronics Engineering Department of Pamukkale University. His current research interests include analog circuits, active filters, synthetic inductors, and CMOS-based circuits. He is the author or co-author of about 140 papers published in scientific journals or conference proceedings.