Scientia Iranica D (2019) 26(3), 1637–1651

Sharif University of Technology
Scientia Iranica
Transactions D: Computer Science & Engineering and Electrical Engineering
http://scientiairanica.sharif.edu

Performance and stability analysis of single-phase grid-connected inverters used in solar photovoltaic systems

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Received 11 February 2016; received in revised form 12 June 2017; accepted 14 August 2017

KEYWORDS
Photovoltaic system;
Single-phase inverter;
Phase locked loop;
Dynamic stability;
Grid strength.

Abstract. Single-Phase Voltage Source Inverters (SP-VSIs) are widely used in grid-connected solar photovoltaic (PV) systems. This paper deals with the dynamic modeling and stability analysis of single-phase grid-connected PV inverters while taking the PLL dynamics into account. The PLL structure employed in this paper includes two control branches: (1) The main branch, known as phase estimation loop, extracts the phase and frequency of the grid voltage and (2) The other branch, known as voltage peak estimation loop, determines the grid voltage amplitude. In this way, the paper first proposes design considerations for the dc-link voltage control and PLL control loops. Then, unified dynamic modeling of the SP-VSI system comprising PLL, dc-link dynamics, and grid is presented, and a linearized block diagram of the whole system is extracted. The linearized block diagram depicts the interaction between the control loops of the PLL and dc-link system, where the PLL control loops consist of phase/frequency and amplitude estimation loops of the grid voltage. Next, the small signal stability of the full system is presented. In addition, impacts of grid strength, operating point, and PLL closed-loop bandwidth on the performance of SP-VSI are investigated by the modal analysis and time domain simulations.

1. Introduction

Single-phase full-bridge voltage source inverters, converting dc power to AC one, are widely used in a large number of applications such as grid-connected solar PV sources [1], Uninterruptable Power Supplies (UPS) [2,3], low power drives, and static VAR compensators. Single-Phase Voltage Source Inverters (SP-VSIs) are mainly employed in two operating modes:

(i) Voltage control mode with a LC filter for stand-alone [4,5] and micro grid [6,7] applications;

(ii) Current control mode with L and LCL filters in grid-connected applications [8-12].

This paper deals with the dynamic modeling and stability analysis of single-phase grid-connected PV inverters while taking the PLL dynamics into account. Most of the research works published recently regarding the single-phase VSIs deal with the advanced control strategies to improve different performance features of the SP-VSI such as tracking error, Total Harmonic Distortion (THD), electromagnetic interference (EMI), resonance damping of interfaced LCL and LC filters, double-line frequency ripple, low voltage ride through, stability and grid synchronization. In [13,14], control

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doi: 10.24200/sci.2017.4384

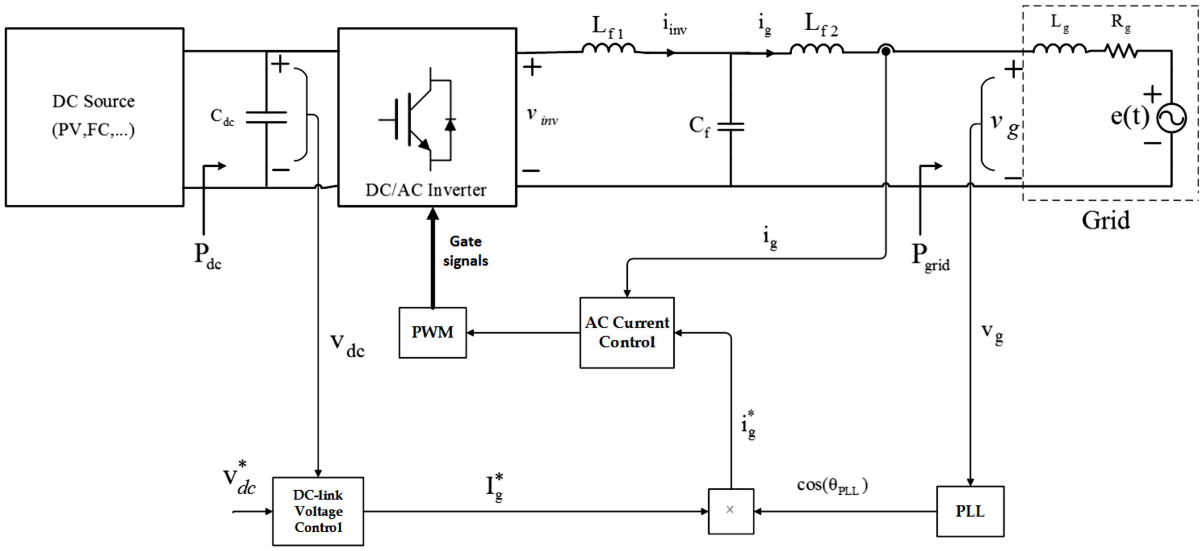

Figure 1. Configuration of the system under study .

strategies were presented for damping the inherent resonance of the LCL filter used in the single-phase grid-connected VSI. In [15], a method was proposed to reduce EMI in single-phase VSIs through periodic dithering of the Pulse-Width Modulated (PWM) switching frequency. In [16], a technique was proposed to reduce the low-frequency dc-link energy oscillation in an SP-VSI by incorporating two auxiliary active switches and one passive energy storage element to the rectifier and inverter sides.

Zhu et al. [17] and Shi et al. [18] described a single-phase full-bridge inverter that possesses limited current ripple at the dc link; thus, the double-line frequency ripple current was prevented from flowing into the input of the inverter. In [19], a sliding-mode control scheme was presented via multi-resonant sliding surface for single-phase grid-connected VSIs with an LCL filter to eliminate the grid current tracking error and suppress its Total Harmonic Distortion (THD). In [20], an improved passivity-based control was proposed for SP-VSI that led to the good quality output voltage with a reasonably low harmonic distortion and offered a global asymptotic stable operation. Yang et al. [21] dealt with the low voltage ride through capability behavior of SP-VSI. Grid synchronization, performed by the Phase Locked Loop (PLL), plays an important role in the control of grid-connected SP-VSIs. Several papers on PLL techniques for SP-VSI application have been published in recent years [22-25] in order to respond quickly and accurately to grid disturbances and, also, good harmonic rejection capability.

Even though dynamic stability of the single-phase PLL solely, without taking the dynamics of the VSI and grid into account, has been investigated in some published papers [25,26], to the best knowledge of the author, few studies on the stability of the whole grid-connected SP-VSI system have been published considering the PLL dynamics. This paper evaluates dynamic stability of the single-phase grid-connected PV inverter system considering the PLL dynamics and using unbalanced transformation from the stationary frame to the dq synchronous frame. In this way, dynamic modeling of the entire system comprising PLL, dc-link dynamics, and grid is presented; then, a linearized block diagram of the whole system is extracted. The linearized block diagram depicts the interaction between the control loops of the PLL and dc-link system, where the PLL control loops consist of phase/frequency and amplitude estimation loops of the grid voltage. Next, small signal stability of the full system is presented; impacts of grid strength, operating point, and PLL closed-loop bandwidth on the performance of the SP-VSI are investigated by the modal analysis. At the end, results of theoretical analyses are verified through time domain simulation.

2. Structure of a single-phase grid-connected inverter

The schematic diagram of a single-phase grid-connected solar PV inverter used as the system under study is shown in Figure 1. This system consists of a PV panel, a DC-DC converter, a dc-link capacitor C_{dc}, and a single-phase full-bridge inverter connected to the grid through an LCL filter. The control system of the inverter consists of three parts: the first part is the dc-link voltage control loop that balances the power flow between the dc-line capacitor and dc-source, thus keeping the dc-link voltage constant. The output of the dc-link voltage controller assigns the magnitude of grid injected current reference I_g^*. The second part is the phase-locked control loop, which is employed to

capture phase θ_g and frequency of the grid voltage at PCC. The third part is the inner VSI current control loop, which is intended to set grid injected current i_g to its reference value i_g^*.

2.1. Inner current control loop

This section deals with the controller design for the inner VSI current control loop. As shown in Figure 1, an LCL filter is used between the VSI and grid to limit the switching harmonics injected to the grid. For weakening the switching harmonics, the resonance frequency of the filter (f_{res}) is required to be smaller than and far from the switching frequency [27]. Besides, the resonance frequency should not interfere with the bandwidth of the current control system [28]; thus, it is selected several times greater than the grid frequency. According to Figure 1, the resonance frequency of the LCL filter is given by $f_{res} = \frac{1}{2\pi\sqrt{L_T C_f}}$, where $L_T = \frac{L_{f1}L_{f2}}{L_{f1}+L_{f2}}$. For the system under study with parameters of Appendix A (given in Table A.1), f_{res} is equal to 3254.7 Hz. If the closed-loop bandwidth of the VSI current control loop is sufficiently below the LCL resonance frequency, for the frequency range of interest, i.e., $\omega << 2\pi f_{res}$, C_f does not influence the inverter output current, and $i_{inv} = i_g$. Hence, considering Figure 1, for the frequency range of $\omega << 2\pi f_{res}$, the interfaced LCL filter can be approximated with a simple L filter; thus, the dynamics of the inverter current is given by:

$$v_{inv} = R_f i_g + L_f \frac{di_g}{dt} + v_g, \tag{1}$$

where $L_f = L_{f1} + L_{f2}$. Considering Eq. (1), Figure 2 depicts the closed-loop block diagram of the inner current control loop.

To select the PI controller parameters, the approach presented in [29] is used. Considering the current controller as PI, $K_I = k_{p-i} + k_{i-i}/s$, and removing the pole of the plant with the zero of the controller, we obtain:

$$\frac{k_{i-i}}{k_{p-i}} = \frac{R_f}{L_f}. \tag{2}$$

By selecting $k_{p-i} = \alpha_i L_f$ and using Eq. (2), the closed-loop transfer function from i_g^* to i_g is given by $i_g(s)/i_g^*(s) = \alpha_i/(s+\alpha_i)$, where α_i is the closed-loop bandwidth. In this study, α_i is selected to be equal to

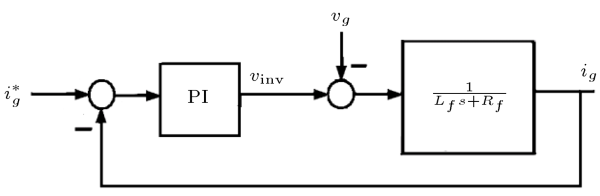

Figure 2. VSI inner current control loop.

$2\pi \times 800$ rad/sec which is much below the LCL filter resonance frequency, where $\omega_{res} = 2\pi \times 3254.7$ rad/sec. Since i_g^* is an ac signal with the fundamental frequency of 50 Hz, i_g cannot accurately track i_g^* with the selected PI controller. However, closed-loop bandwidth α_i is 16 times greater than the grid fundamental frequency, 50 Hz, which, in turn, results in $I_g = 0.9981 I_g^*$, with the tracking error of 0.19%.

2.2. DC-link voltage control

The relation between the inverter output current and dc-link voltage (v_{dc}) can be obtained through the power balance equation. According to Figure 1, the power balance equation for the dc-link capacitor is given as follows:

$$P_{dc} - P_{\text{grid}} - P_{\text{loss}} = v_{dc} C_{dc} \frac{dv_{dc}}{dt}, \tag{3}$$

where v_{dc} and C_{dc} are the dc-link voltage and capacitor, respectively. In addition, P_{dc}, P_{grid}, and P_{loss} are the average values of the dc-source output power, grid injected power, and converter losses, respectively. According to Figure 1, P_{grid}, under unity power factor operation, can be given as follows:

$$P_{\text{grid}} = \frac{1}{2} V_g I_g, \tag{4}$$

where V_g and I_g are the amplitudes of the grid voltage and current at the connection point of the SP-VSI to the grid. By linearizing Eq. (3) around the operating point, we have:

$$\Delta P_{dc} - \Delta P_{\text{grid}} - \Delta P_{\text{loss}} = V_{dc0} C_{dc} \frac{d\Delta v_{dc}}{dt}, \tag{5}$$

where Δ denotes the variation of the variables around the operating point, and V_{dc0} is the dc-link voltage at the operating point and is equal to its reference value. Based on Eqs. (4) and (5) and by using PI controller, a block diagram of the dc-link voltage control loop is extracted as depicted in Figure 3.

The transfer function $\alpha_i/(s+\alpha_i)$ in Figure 3 is the closed-loop transfer function of the inner current control loop with bandwidth of α_i; V_{dc}^* is the dc-link voltage reference; $PI(s)$ is the dc-link PI controller, $PI(s) = k_{P,dc} + k_{I,dc}/s$.

The output of the dc-link controller determines the reference value of the grid injected current amplitude. If the grid voltage is assumed as $v_g(t) = V_g \cos(\omega_g t)$, the reference value of the grid injected current is obtained according to Figure 4 and can be written as follows:

$$i_g^*(t) = I_g^* \cos(\theta_{PLL}) = I_g^* \cos(\omega_g t), \tag{6}$$

where ω_g is the grid frequency, and θ_{PLL} under stable steady state conditions is equal to $\omega_g t$.

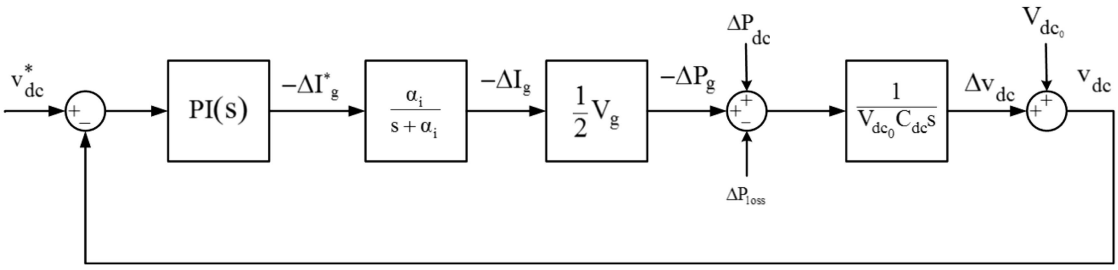

Figure 3. Block diagram of the dc-link voltage control loop.

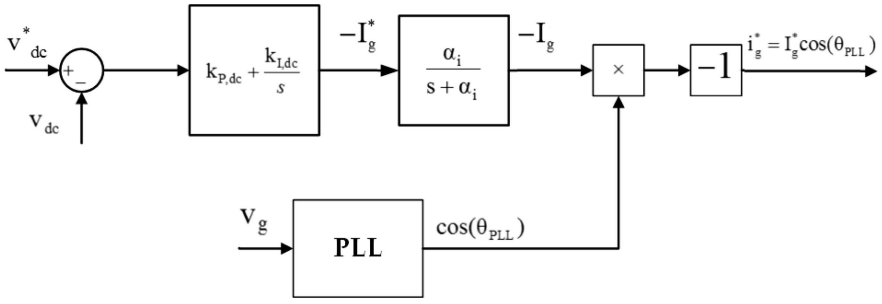

Figure 4. dc-link voltage control.

2.3. Selection of controller parameters

In single-phase systems, the SP-VSI instantaneous power injected to the grid is not constant and contains a double-line frequency component resulting in double-line frequency ripple on the dc-link voltage. It is shown that the amplitude of the double-line frequency ripple on the dc-link voltage is obtained as follows:

$$V_{2\omega} = \frac{P_g}{2\omega_g C_{dc} V^*_{dc}}, \tag{7}$$

where P_g is the average value of the SP-VSI output active power injected to the grid. If the average value of the dc-link voltage is equal to its reference value, i.e., $V_{dc0} = V^*_{dc}$, and the double-line frequency ripple of the dc-link voltage is given as $\tilde{v}_{dc}(t) \approx V_{2\omega}\sin(2\omega_g t + \theta_0)$, then, according to Figure 4, the amplitude of the grid injected current reference can be obtained as follows:

$$I^*_g \approx (V_{2\omega}\sin(2\omega_g t + \theta_0))\left(k_{P,dc} + \frac{k_{I,dc}}{s}\right). \tag{8}$$

In Eq. (8), I^*_g comprises two terms: the first term with double-line frequency originates from the proportional gain of the PI controller, and the second term corresponds to the integral gain. If the second term corresponding to integrator is assumed to be a constant dc value, I^*_g in Eq. (8) can be given as follows:

$$I^*_g \approx k_{P,dc}V_{2\omega}\sin(2\omega_g t + \theta_0) + I^*_{g_{Int}}. \tag{9}$$

Replacing Eq. (9) into Eq. (6) results in the following expression for $i^*_g(t)$:

$$i^*_g(t) \approx I^*_{g_{Int}}\cos(\omega_g t) - \frac{k_{P,dc}V_{2\omega}}{2}\sin(\omega_g t + \theta_0) + \frac{k_{P,dc}V_{2\omega}}{2}\sin(3\omega_g t + \theta_0). \tag{10}$$

According to Eq. (10), the inverter reference current contains both the fundamental and the third-order harmonic components. According to [30], the amplitude of the third-order harmonics should be lower than $0.04I_{gn}$, where I_{gn} is the nominal value of the SP-VSI output current. Hence, the following constraint on $k_{P,dc}$ is obtained as follows:

$$k_{P,dc} \leq \frac{0.08I_{g_n}}{\hat{V}_{2\omega}}. \tag{11}$$

For the system under study with parameters of Appendix A (given in Table A.1), the upper limit of $k_{P,dc}$ is 0.078; thus, $k_{P,dc}$ is selected equal to 0.07. For selection of integral gain, we use root locus of the closed-loop dc-link system for $k_{P,dc} = 0.07$ and different values of integral gain $k_{I,dc}$ (see Figure 5). It is clear that, for $k_{I,dc} = 1.57$, the damping ratio of the dominant oscillatory poles of the closed-loop system is 0.7; thus, this value is selected for $k_{I,dc}$.

3. Modeling of a single-phase grid-connected inverter

This Section 3 and Section 4 deal with the unified dynamic modeling of the single-phase grid-connected inverter. In order to simplify the system analysis, the following assumptions are considered:

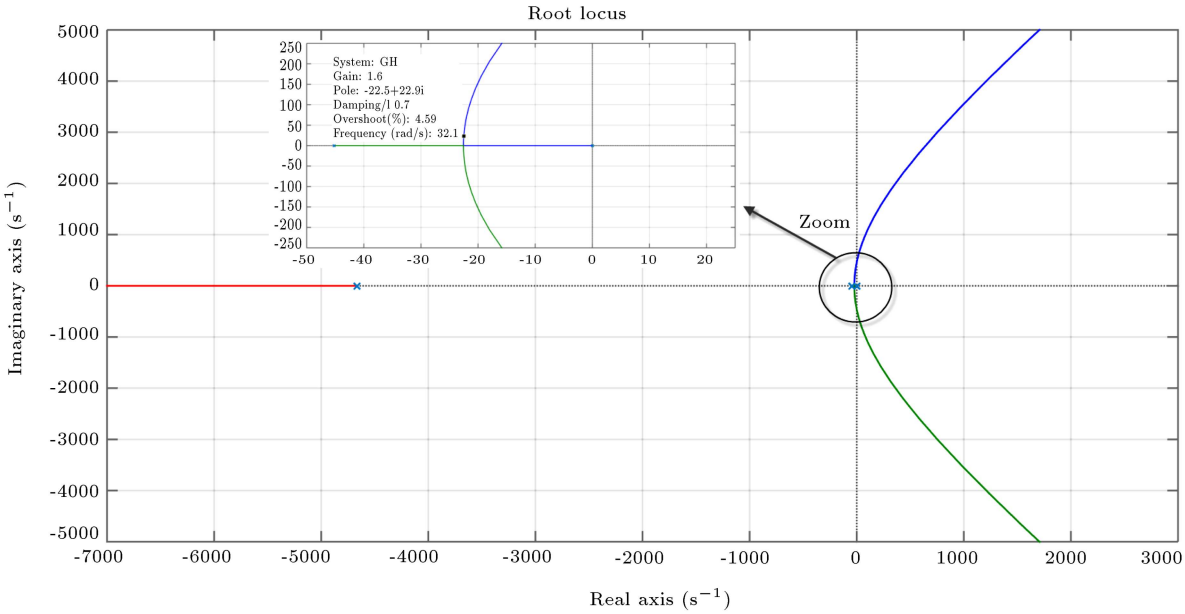

Figure 5. Locus plot of the closed-loop dc-link system under variation of the integral gain, $k_{I,dc}$.

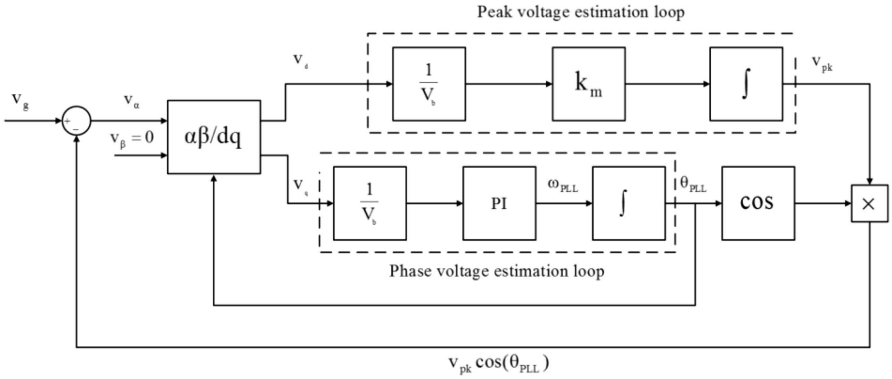

Figure 6. Block diagram of the PLL used for study.

1. The shunt branch of the LCL filter, i.e., C_f, is neglected, thus $i_{inv} \approx i_g$;
2. Positive directions of the system voltage and current are considered according to Figure 1.

3.1. Dynamic modeling of single-phase PLL

Synchronous Reference Frame PLLs (SRF-PLLs) are widely used in three-phase applications [31] for grid synchronization. For implementing the SRF-PLL in SP-VSIs, an orthogonal signal should be built to transform the system from the stationary frame to the dq synchronous frame. Some approaches to orthogonal signal generation include low-pass filters resulting in time delays, Kalman filter requiring too much digital implementation, and SOGI approach suffering from dc offset [22]. An efficient SRF-PLL for SP-VSI, employed in this study, was reported in [22], which was achieved using unbalanced transformation from the stationary frame to the dq synchronous frame. The block diagram of this PLL is shown in Figure 6, where the unbalanced $\alpha\beta - dq$ transformation is applied to convert $\alpha\beta$ signals to dq ones.

According to Figure 6, the PLL structure includes two control branches: the main branch, known as phase estimation loop, extracts the phase and frequency of the grid voltage; the other branch, known as peak voltage estimation loop, determines the grid voltage amplitude. According to Figure 6, by using grid voltage, $v_g(t)$ and phase and amplitude of the grid voltage extracted by the PLL, i.e., θ_{PLL} and v_{pk}, signal v_α is constructed as $v_\alpha = v_g(t) - v_{pk}\cos(\theta_{PLL})$ and signal v_β is set to zero. By applying the Park transformation to v_α and v_β, the dq signals of v_d and v_q are provided. Hence, the q axis signal v_q is used to generate phase angle θ_{PLL}, forming the PLL phase estimation loop, and the d axis signal v_d propagates through an integrator and, then, yields the PLL peak voltage (v_{pk}) estimation loop.

With regard to Figure 6, the PLL dynamics in s-domain can be derived as follows:

$$v_{pk}(s) = \frac{k_m}{V_b s} v_d(s), \tag{12}$$

$$\omega_{PLL}(s) = \frac{1}{V_b}\left(k_{P,PLL} + \frac{k_{I,PLL}}{s}\right) v_q(s), \tag{13}$$

$$\theta_{PLL}(s) = \frac{1}{s}\omega_{PLL}(s), \tag{14}$$

where V_b is the base value of the grid voltage, and v_{pk}, ω_{PLL}, and θ_{PLL} are the estimated values of the magnitude, frequency, and phase angle of the grid voltage, respectively. PI in Figure 6, with parameters of $k_{P,PLL}$ and $k_{I,PLL}$, is the controller used in the PLL phase estimation loop, and k_m is the integral gain used in the PLL peak voltage estimation loop. In Section 3-2, design methodology for selection of $k_{P,PLL}$, $k_{I,PLL}$, and k_m will be given.

According to Figure 6 and assuming $x_c(s) = \frac{1}{V_b s} v_q(s)$, the state space equations of the PLL system can be given as follows:

$$\dot{v}_{pk} = \frac{k_m}{V_b} v_d, \tag{15}$$

$$\dot{\theta}_{PLL} = \frac{k_{P,PLL}}{V_b} v_q + k_{I,PLL} x_c, \tag{16}$$

$$\dot{x}_c(t) = \frac{1}{V_b} v_q(t), \tag{17}$$

where $x = \begin{bmatrix} v_{pk} & \theta_{PLL} & x_c \end{bmatrix}^T$ is the vector of PLL state variables. For a single-phase system with a so-called variable f, the $\alpha\beta$ to dq transformation can be defined as follows:

$$f_{dq} = f_\alpha \times e^{-j\theta_{PLL}}, \tag{18}$$

where $f_{dq} = f_d + jf_q$ and $f_\alpha = f$. Assuming that the grid voltage as the PLL input is $v_g(t) = V_g \cos(\theta_g)$; in addition, according to Figure 6 and Eq. (18), v_d and v_q in the PLL block diagram of Figure 6 are obtained as follows:

$$\begin{cases} v_d = \dfrac{V_g}{2}\cos(\theta_g - \theta_{PLL}) - \dfrac{v_{pk}}{2} \\ \qquad + \dfrac{V_g}{2}\cos(\theta_g + \theta_{PLL}) - \dfrac{v_{pk}}{2}\cos(2\theta_{PLL}) \\ v_q = \dfrac{V_g}{2}\sin(\theta_g - \theta_{PLL}) - \dfrac{V_g}{2}\sin(\theta_g + \theta_{PLL}) \\ \qquad + \dfrac{v_{pk}}{2}\sin(2\theta_{PLL}) \end{cases} \tag{19}$$

According to Eq. (19), each of v_d and v_q comprises quasi dc and double-line frequency components. When θ_{PLL} and v_{pk} converge to θ_g and V_g, respectively, i.e., $\theta_{PLL} \to \theta_g$ and $v_{pk} \to V_g$, then double-line frequency components decay to zero and the quasi dc components converge to dc ones. Neglecting the double-line frequency components, we have:

$$\begin{cases} v_d \approx \frac{1}{2} V_g \cos(\theta_g - \theta_{PLL}) - \frac{1}{2} v_{pk} \\ v_q \approx \frac{1}{2} V_g \sin(\theta_g - \theta_{PLL}) \end{cases} \tag{20}$$

On the other hand, transferring $v_g = V_g \cos(\theta_g)$ into dq reference frame by using Eq. (18) yields:

$$v_{g,dq} = \frac{1}{2} V_g e^{j(\theta_g - \theta_{PLL})} + \frac{1}{2} V_g e^{-j(\theta_g + \theta_{PLL})}. \tag{21}$$

Neglecting double-frequency terms in Eq. (21), i.e., $\frac{1}{2} V_g e^{-j(\theta_g + \theta_{PLL})}$, and separating $v_{g,dq}$ components result in the following expressions for $v_{g,d}$ and $v_{g,q}$:

$$\begin{cases} v_{g,d} = \frac{1}{2} V_g \cos(\theta_g - \theta_{PLL}) \\ v_{g,q} = \frac{1}{2} V_g \sin(\theta_g - \theta_{PLL}) \end{cases} \tag{22}$$

According to Eqs. (20) and (22), the relationship between v_d, v_q and $v_{g,d}$, $v_{g,q}$ can be given by:

$$\begin{cases} v_d = v_{g,d} - \frac{1}{2} v_{pk} \\ v_q = v_{g,q} \end{cases} \tag{23}$$

3.2. PLL control structure

In this section, control loops of the PLL extracting the amplitude and phase angle of the single-phase grid are given. By linearizing (20) around the operating point, i.e., θ_{PLL0} and θ_{g0} where $\theta_{PLL0} = \theta_{g0}$, we have:

$$\begin{cases} \Delta v_d \approx \frac{1}{2}\Delta V_g - \frac{1}{2}\Delta v_{pk} \\ \Delta v_q \approx \frac{1}{2} V_{g0}(\Delta\theta_g - \Delta\theta_{PLL}) \end{cases} \tag{24}$$

According to Figure 6 and Eq. (24), the PLL control loops used for estimation of amplitude, phase angle, and frequency of the grid voltage are obtained as depicted in Figure 7.

In Figure 7, V_b is the base value of the grid voltage and is equal to the grid voltage amplitude.

In Figure 7(a) and (b), controllers k_m/s and $PI(s) = k_{P,PLL} + k_{I,PLL}/s$ are used for setting v_{pk}

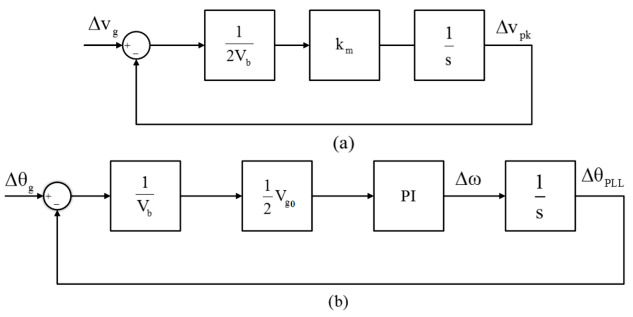

Figure 7. PLL control loops: (a) PLL amplitude estimation loop and (b) PLL phase estimation loop.

and θ_{PLL} to their reference values, i.e., V_g and θ_g, respectively. Parameters k_m, $k_{P,PLL}$, and $k_{I,PLL}$ are designed to obtain stable closed-loop systems, zero tracking error, and better low frequency disturbance rejection. According to Figure 7(a), the closed-loop transfer function from V_g to v_{pk} is given by:

$$\frac{v_{pk}}{V_g} = \frac{\omega_{PLL,mag}}{s + \omega_{PLL,mag}}, \tag{25}$$

where $\omega_{PLL,mag} = k_m/2V_b$ is the closed-loop bandwidth of the amplitude estimation loop in Figure 7(a). In addition, in Figure 7(b), the closed-loop transfer function from θ_g to θ_{PLL} is given by:

$$\frac{\theta_{PLL}}{\theta_g} = \frac{2\zeta\omega_{PLL,ph} + \omega^2_{PLL,ph}}{s^2 + 2\zeta\omega_{PLL,ph} + \omega^2_{PLL,ph}}, \tag{26}$$

where $\omega_{PLL,ph}$ is the closed-loop bandwidth of the phase estimation loop and $\omega^2_{PLL,ph} = k_{I,PLL}/2$ and $2\zeta\omega_{PLL,ph} = k_{P,PLL}/2$. Since grid voltage amplitude V_{g0} is close to its rated value, V_{g0} and V_b (in Figure 7(b)) are identical; thus, they do not appear in Eq. (26). In Figure 7, there is interaction between the PLL amplitude and phase estimation loops; thus, to have better harmonic rejection and stability margin, $\omega_{PLL,mag}$ should be much larger than $\omega_{PLL,ph}$. In this study, $\omega_{PLL,mag} = 2\pi \times 210$ rad/sec and $\omega_{PLL,ph} = \omega_{PLL,mag}/20 = 2\pi \times 10.5$ rad/sec are selected.

4. Dynamic modeling of the grid and dc-link voltage

According to Figure 1, the single-phase grid at the connection point with the SP-VSI can be modeled with internal voltage $e(t)$ in series with R_g and L_g as the grid resistance and inductance. The grid dynamics can be described by:

$$v_g(t) = R_g i_g(t) + L_g \frac{di_g(t)}{dt} + e(t), \tag{27}$$

where v_g and i_g are the grid voltage and current injected to the grid by the inverter, respectively, and $e(t)$ is the grid internal voltage. Transferring Eq. (27) into dq frame, we have:

$$v_{g,dq} = R_g i_{g,dq} + j\omega_{PLL} L_g i_{g,dq} + L_g \frac{di_{g,dq}}{dt} + e_{dq}. \tag{28}$$

By neglecting derivative of the grid injected current and resistance voltage drop and considering $e(t) = E\cos(\theta_e)$, Eq. (28) can be rewritten as follows:

$$v_{g,dq} = j\omega_{PLL} L_g i_{g,dq} + \frac{1}{2} E e^{j(\theta_e - \theta_{PLL})} + \frac{1}{2} E e^{-j(\theta_e + \theta_{PLL})}. \tag{29}$$

By neglecting the double-line frequency term in Eq. (29), i.e., $\frac{1}{2}Ee^{-j(\theta_e+\theta_{PLL})}$, components d and q of the grid voltage can be given as follows:

$$v_{g,d} = -\omega_{PLL} L_g i_{g,q} + \frac{1}{2} E\cos(\theta_e - \theta_{PLL}), \tag{30}$$

$$v_{g,q} = \omega_{PLL} L_g i_{g,d} + \frac{1}{2} E\sin(\theta_e - \theta_{PLL}). \tag{31}$$

The linearized forms of Eqs. (30) and (31) are given as follows:

$$\Delta v_{g,d} = -L_g I_{g,q0}\Delta\omega_{PLL} - L_g\omega_0\Delta i_{g,q} - \frac{1}{2} E\sin(\theta_{e0} - \theta_{PLL0})[\Delta\theta_e - \Delta\theta_{PLL}], \tag{32}$$

$$\Delta v_{g,q} = L_g I_{g,d0}\Delta\omega_{PLL} + L_g\omega_0\Delta i_{g,d} + \frac{1}{2} E\cos(\theta_{e0} - \theta_{PLL0})[\Delta\theta_e - \Delta\theta_{PLL}], \tag{33}$$

where Δ denotes the small signal value.

At unity power factor operation, $I_{g,q0}$ and $\Delta i_{g,q}$ in Eq. (32) are equal to zero; thus, $\Delta v_{g,d}$ can be simplified to:

$$\Delta v_{g,d} = -\frac{1}{2} E\sin(\theta_{e0} - \theta_{PLL0})[\Delta\theta_e - \Delta\theta_{PLL}]. \tag{34}$$

4.1. dc-link dynamic modeling

Regarding Figure 4, the amplitude of grid injected reference current, I_g^*, can be written as follows:

$$I_g^*(s) = -\left(k_{P,dc} + \frac{k_{I,dc}}{s}\right)(v_{dc}^* - v_{dc}). \tag{35}$$

By defining $x_a = \frac{1}{s}(v_{dc}^* - v_{dc})$, Eq. (35) can be given as follows:

$$I_g^* = -k_{P,dc}(v_{dc}^* - v_{dc}) - k_{I,dc}x_a, \tag{36}$$

$$\dot{x}_a = v_{dc}^* - v_{dc}. \tag{37}$$

In addition, considering Figure 3, the state equation corresponding to inner current control loop can be given as follows:

$$I_g^\bullet = -\alpha_i I_g + \alpha_i I_g^*. \tag{38}$$

According to Figure 4 and assuming the grid current control to be fast enough, the grid injected current, $i_g(t)$, can be given as follows:

$$i_g(t) = I_g\cos(\theta_{PLL}). \tag{39}$$

By transferring Eq. (39) into dq-frame by using Eq. (18) and neglecting double-frequency terms, we have:

$$\begin{cases} i_{g,d} = \frac{1}{2} I_g \\ i_{g,q} = 0 \end{cases} \tag{40}$$

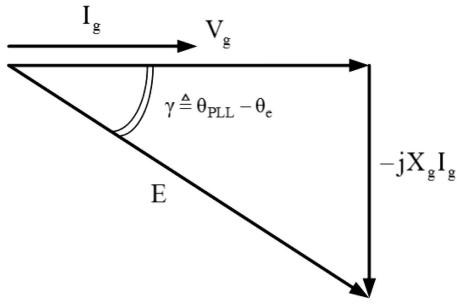

Figure 8. Phasor diagram of the grid voltage and current at unity power factor operation.

Considering Eq. (40) and replacing Eq. (36) into Eq. (38) yields:

$$i^{\bullet}_{g,d} = -\alpha_i i_{g,d} - \alpha_i \frac{k_{P,dc}}{2}(v^*_{dc} - v_{dc}) - \alpha_i \frac{k_{I,dc}}{2} x_a. \quad (41)$$

Assuming the lossless inverter and using the dc-ink power balance equation, we have:

$$P_{dc} - P_g = C_{dc} v_{dc} \frac{dv_{dc}}{dt}, \quad (42)$$

where P_{dc} and P_g are the dc-source power and the grid injected power, respectively. Figure 8 shows the phasor diagram of the grid voltage and current at unity power factor operation of the inverter. Considering Figure 8, the average value of the grid injected power is given by:

$$P_g = \frac{1}{2} E I_g \cos(\theta_{PLL} - \theta_e), \quad (43)$$

where E is the amplitude of the grid internal voltage (see Figure 1).

Substituting Eq. (40) into Eq. (43) yields:

$$P_g = E \cos(\theta_{PLL} - \theta_e)\, i_{g,d}. \quad (44)$$

Hence, by replacing Eq. (44) into Eq. (42), we have:

$$P_{dc} - E \cos(\theta_{PLL} - \theta_e)\, i_{g,d} = C_{dc} v_{dc} \frac{dv_{dc}}{dt}. \quad (45)$$

The linearized form of (45) is expressed as follows:

$$\Delta P_{dc} - E\cos(\gamma_0)\Delta i_{g,d} + E I_{g,d0} \sin(\gamma_0)\Delta\gamma = V_{dc0} C_{dc} \frac{d\Delta v_{dc}}{dt}, \quad (46)$$

where $\gamma = \theta_{PLL} - \theta_e$. Based on Eq. (46), the dc-link dynamics can be described as follows:

$$\Delta \dot{v}_{dc} = \frac{1}{V_{dc_0} C_{dc}} \left[\Delta P_{dc} - E\cos(\gamma_0)\Delta i_{g,d} + E I_{g,d0} \sin(\gamma_0)\Delta\gamma\right]. \quad (47)$$

5. Small signal stability analysis

The linearized dynamic equations of the single-phase grid-connected inverter are derived in the last sections. Considering Figures 6 and 4 and Eqs. (23), (33), (34), and (47), the linearized block diagram of the PLL, grid, and dc-link dynamics can be given as depicted in Figure 9.

According to Eqs. (15)-(17), (37), (41),, and (47), linearized state space model of the system may be given by:

$$\Delta \dot{x} = A\Delta x + B\Delta u, \quad (48)$$

where x and u are the vectors of the state variables and exogenous inputs and are defined as follows:

$$\Delta x^T = \begin{bmatrix}\Delta v_{dc} & \Delta x_a & \Delta v_{pk} & \Delta\theta_{PLL} & \Delta x_c & \Delta i_{g,d}\end{bmatrix}, \quad (49)$$

$$\Delta u^T = \begin{bmatrix}\Delta v^*_{dc} & \Delta\theta_e & \Delta P_{dc}\end{bmatrix}. \quad (50)$$

In addition, A and B are the state and input matrices, respectively. In order to evaluate dynamic stability of the single-phase grid-connected inverter, modal analysis is performed on the current system in Figure 1 with parameters of Appendix A (given in Table A.1).

The system modes and the corresponding participation factors under the nominal operating conditions with rated inverter output power are shown in Tables 1 and 2. The results of Table 1 correspond to the grid Short-Circuit Ratio (SCR) of 20 pu. Of note, the SCR is defined as the ratio of the grid short-circuit power to the inverter rated power. By using participation factors, the degree of contribution of each state variable in the system modes can be detected [32] (see Appendix B). Based on Table 1, it can be concluded that

Table 1. Results of modal analysis ($P_g = 1$ pu and SCR = 20 pu).

Modes	Eigenvalues	Frequency (Hz)	Damping
λ_1	-1338.919	0	1
$\lambda_{2,3}$	$-46.35 \pm j46.251$	7.361	0.708
$\lambda_{4,5}$	$-22.293 \pm j22.449$	3.573	0.705
λ_6	-4965.4	0	1

Table 2. Results of participation factors calculation.

Mode	State					
	Δv_{dc}	Δx_a	Δv_{pk}	$\Delta\theta_{PLL}$	Δx_c	$\Delta i_{g,d}$
λ_1	0	0	1	0	0	0
$\lambda_{2,3}$	0.027	0.011	0	0.72	0.732	0.732
$\lambda_{4,5}$	0.698	0.692	0	0.008	0.011	0.011
λ_6	0	0	0	0	0	1

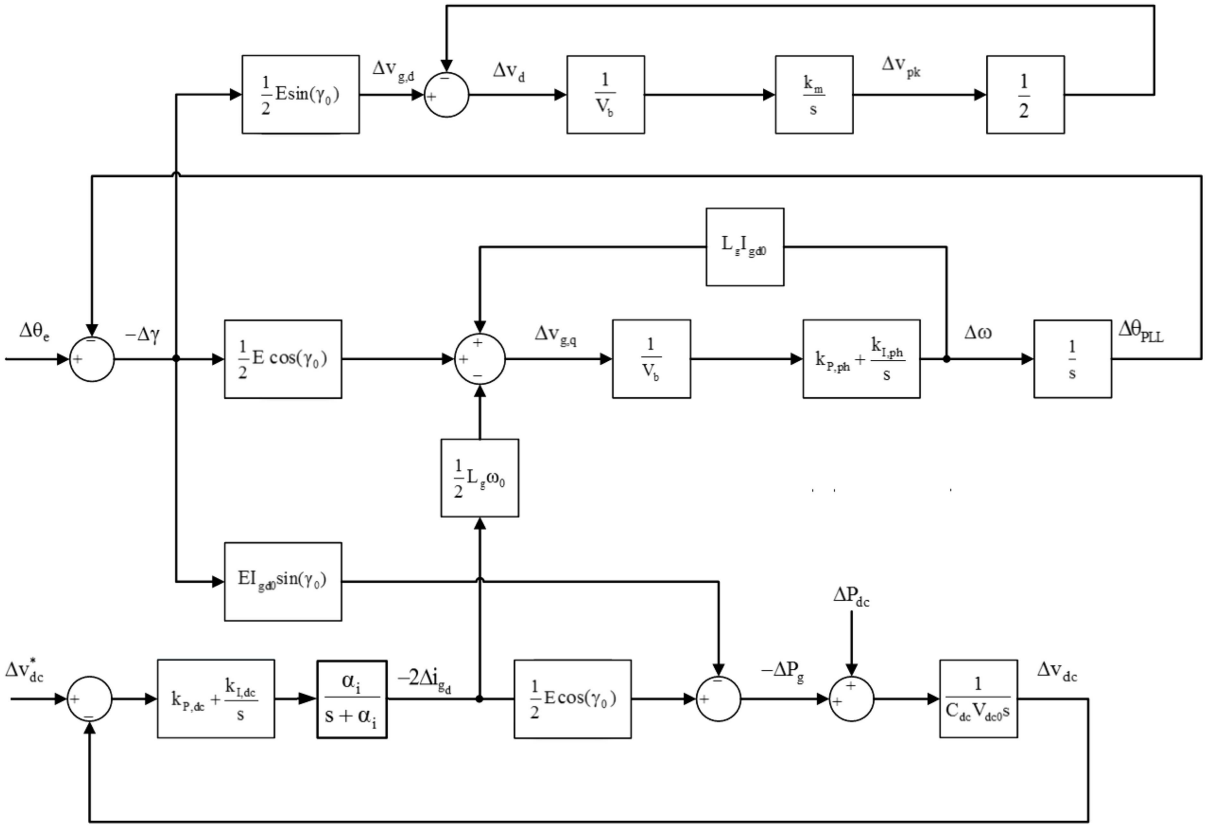

Figure 9. Linearized block diagram of the PLL, grid, and dc-link dynamics.

the overall system consists of two real and two pairs of conjugate complex eigen values under $P_g = 1$ pu. According to the results of Tables 1 and 2, the following key points are found:

- The real mode $\lambda_1 = -1338.919$ corresponds to state variable Δv_{pk} and is relatively equal to bandwidth of the grid voltage amplitude estimation loop (see Figure 7(a));
- The oscillatory modes $\lambda_{2,3} = -46.35 \pm j46.251$ belong to state variables $\Delta\theta_{PLL}$ and Δx_c with damped frequency of 7.361 Hz;
- The modes $\lambda_{4,5} = -22.293 \pm j22.449$ are mostly associated with the state variables of the dc-link dynamics, i.e., Δv_{dc} and Δx_a, with damped frequency of 3.573 Hz. These modes, as will be shown in the next section, may cause system instability under a weak grid condition;
- The real mode $\lambda_6 = -4965.4$ corresponds to state variable $\Delta i_{g,d}$ and is relatively equal to the bandwidth of the inner current control loop, where the closed-loop bandwidth of the inner current control loop is $\alpha_i = 2\pi \times 800$ rad/sec.

5.1. Effects of the grid Short-Circuit Ratio (SCR) and operating point

The grid SCR and operating point of the system are the two important factors that affect system stability. Hence, this section evaluates system stability according to these factors.

5.1.1. Effect of the grid SCR

Table 3 depicts the system modes at nominal operating

Table 3. System modes under different values of the grid SCR.

	Grid SCR (pu)			
	20 pu	**5 pu**	**3.3 pu**	**2 pu**
Eigenvalues	$\lambda_1 = -1338.919$	$\lambda_1 = -1338.919$	$\lambda_1 = -1338.919$	$\lambda_1 = -1338.919$
	$\lambda_{2,3} = -46.35 \pm 46.251i$	$\lambda_{2,3} = -47.6 \pm 45.98i$	$\lambda_{2,3} = -48.636 \pm 44.947i$	$\lambda_{2,3} = -51.835 \pm 40.275i$
	$\lambda_{4,5} = -22.293 \pm 22.449i$	$\lambda_{4,5} = -20.8 \pm 22.7i$	$\lambda_{4,5} = -18.348 \pm 22.753i$	$\lambda_4 = 0$, $\lambda_5 = 1.98$
	$\lambda_6 = -4965.4$	$\lambda_6 = -4965.4$	$\lambda_6 = -4965.4$	$\lambda_6 = -4965.4$

point and under different values of the grid SCR. Of note, the grid SCR is defined as the ratio of the grid short-circuit power to the rated power of the grid-connected inverter. It can be seen that with the decrease of the grid SCR, mode λ_1 remains constant, while modes $\lambda_{2,3}$ move toward the left-half plane, and modes $\lambda_{4,5}$ move toward the right-half plane resulting in the system instability. This means that dc-link control and dynamics have the highest impact on the system instability.

5.1.2. Effect of the operating point

Table 4 shows the system modes at SCR = 2.4 under different values of the inverter output active power. According to Table 4, with the increase of the inverter output active power, λ_1 remains constant, $\lambda_{2,3}$ move slightly toward the left-half plane, and $\lambda_{4,5}$ move toward the right-half plane. When the output power reaches the value of 1.2 pu, mode λ_5 and, thus, the whole system become unstable.

6. Simulation results

In order to illustrate the validity of the theoretical results obtained from the linearized model of the system, a 2-kW single-phase grid-connected inverter fed by the PV system is simulated in Matlab-Simulink environment. The system under study parameters is given in Appendix A (in Table A.1).

Figure 10 depicts the time responses of the SP-

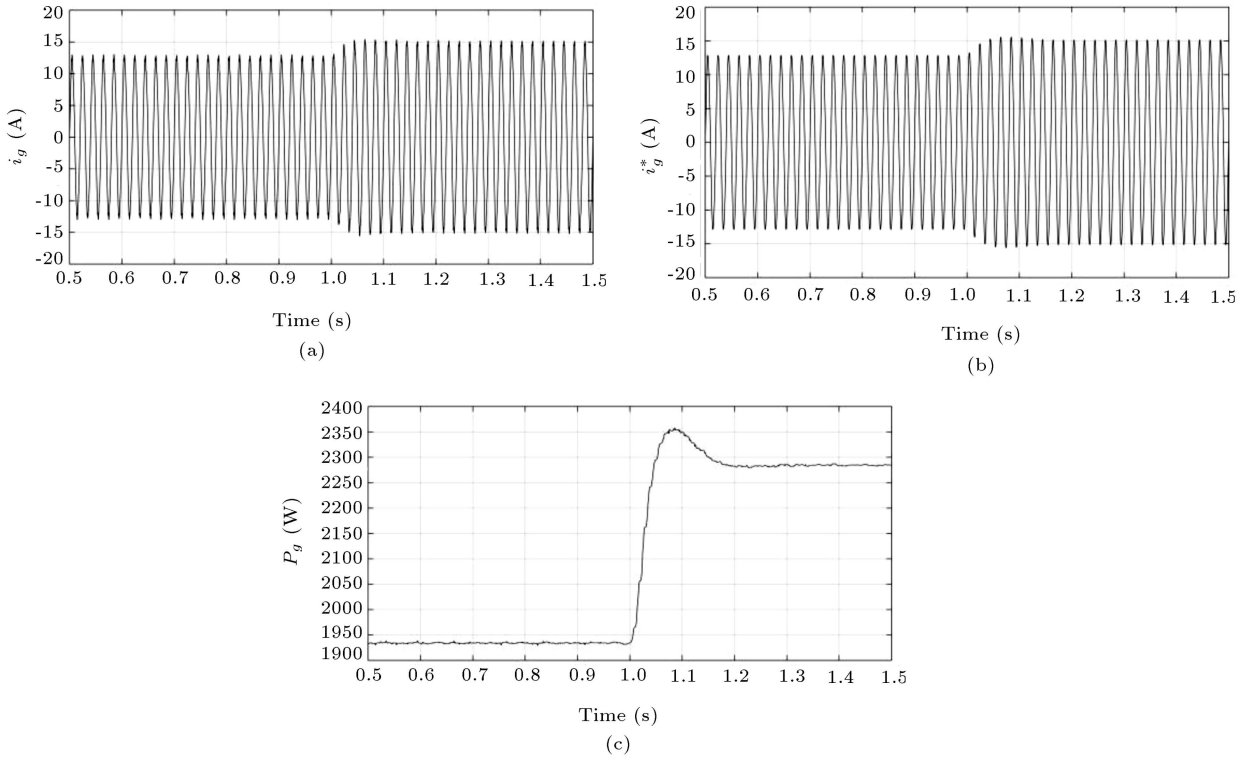

Figure 10. Time responses of the SP-VSI under the step change of the solar irradiance at $t = 1$ sec from 1000 W/m^2 to 1200 W/m^2: (a) Current injected to the grid, i_g, (b) current reference injected to the grid, i_g^*, and (c) inverter output active power injected to the grid, P_g.

Table 4. System modes under different values of inverter output power.

	Active power output			
	0.5 pu	**0.8 pu**	**1 pu**	**1.2 pu**
Eigenvalues	$\lambda_1 = -1338.919$	$\lambda_1 = -1338.919$	$\lambda_1 = -1338.919$	$\lambda_1 = -1338.919$
	$\lambda_{2,3} = -47.65 \pm 45.92i$	$\lambda_{2,3} = -49.06 \pm 44.45i$	$\lambda_{2,3} = -50.33 \pm 42.91i$	$\lambda_2 = -51.96 + 40.25i$
	$\lambda_{4,5} = -20.62 \pm 22.71i$	$\lambda_{4,5} = -17.15 \pm 22.64i$	$\lambda_{4,5} = -12.73 \pm 21.46i$	$\lambda_3 = -51.73 - 40.29i$
	$\lambda_6 = -4965.4$	$\lambda_6 = -4965.4$	$\lambda_6 = -4965.4$	$\lambda_4 = -4.08 + 4.06i$
				$\lambda_5 = 6.05 - 6.18i$
				$\lambda_6 = -4965.4$

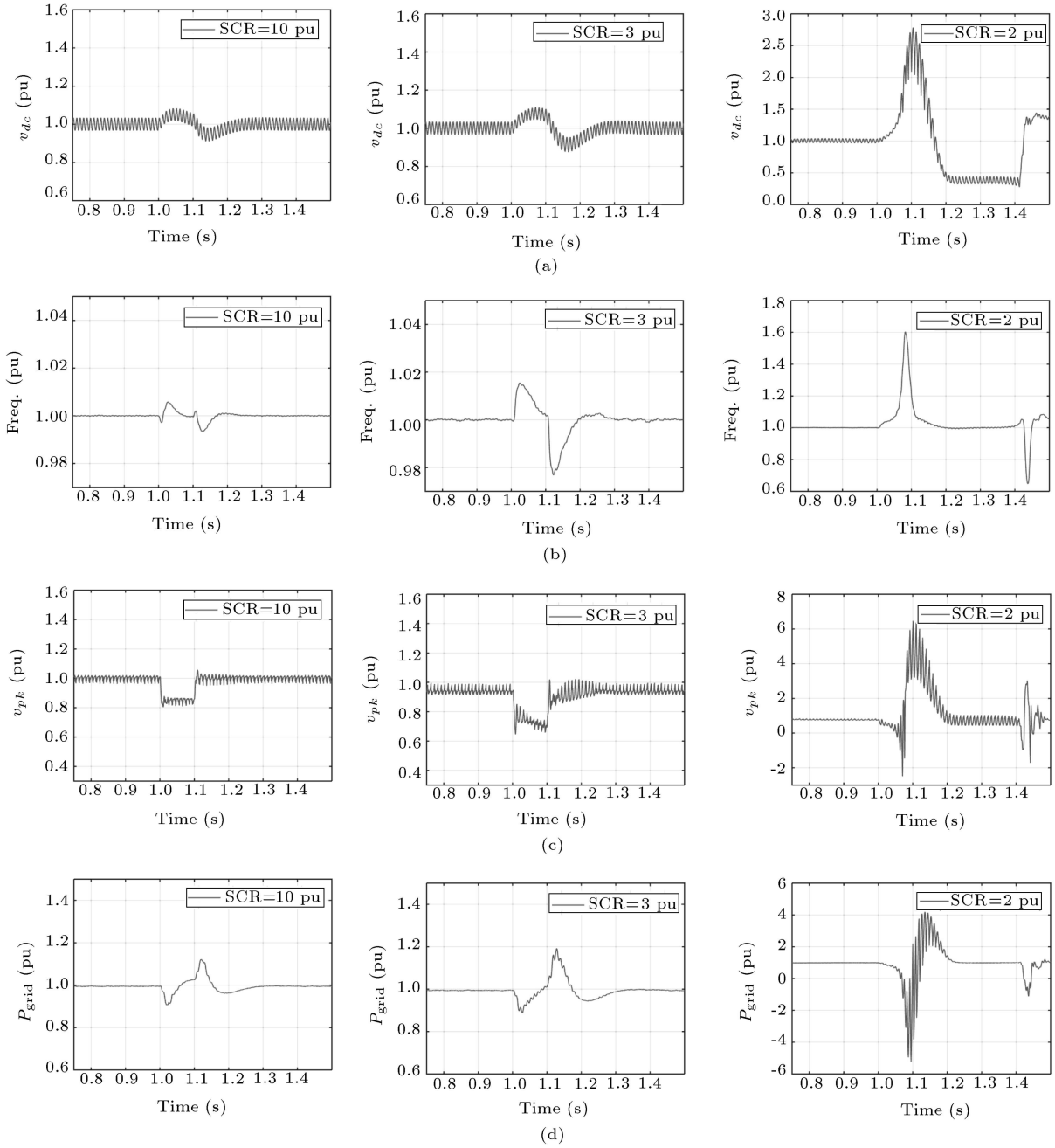

Figure 11. System response under different values of the grid SCR: (a) dc-link voltage, (b) estimated voltage frequency (f_{PLL}), (c) estimated voltage magnitude (v_{pk}), and (d) active power output.

VSI under the step change of the solar irradiance at $t = 1$ sec from 1000 W/m^2 to 1200 W/m^2. This figure comprises the time responses of the current and current reference injected to the grids, i_g and i_g^*, and the inverter output active power injected to grid P_g. According to Figure 10, after the change of the solar irradiance, I_g increases from 12.43 A to 14.7 A and P_g from 1940 W to 2280 W.

Figures 11-13 show the time domain simulations of the single-phase grid-connected inverter when the system is excited by a small disturbance on the grid side at $t = 1$ (s). Simulations are carried out under the different values of the grid SCR, inverter output active power, and PLL closed-loop bandwidth, respectively. In Figures 11-13, the responses of the dc-link voltage, grid frequency estimated by the PLL, peak of the grid voltage detected by the PLL, and inverter output active power are depicted in pu, where the base values correspond to their nominal values and are equal to 380 v, 50 Hz, $220\sqrt{2}$ v, and 2 kW, respectively.

Figure 11 shows the simulation results of the test system at the nominal VSI output active power and

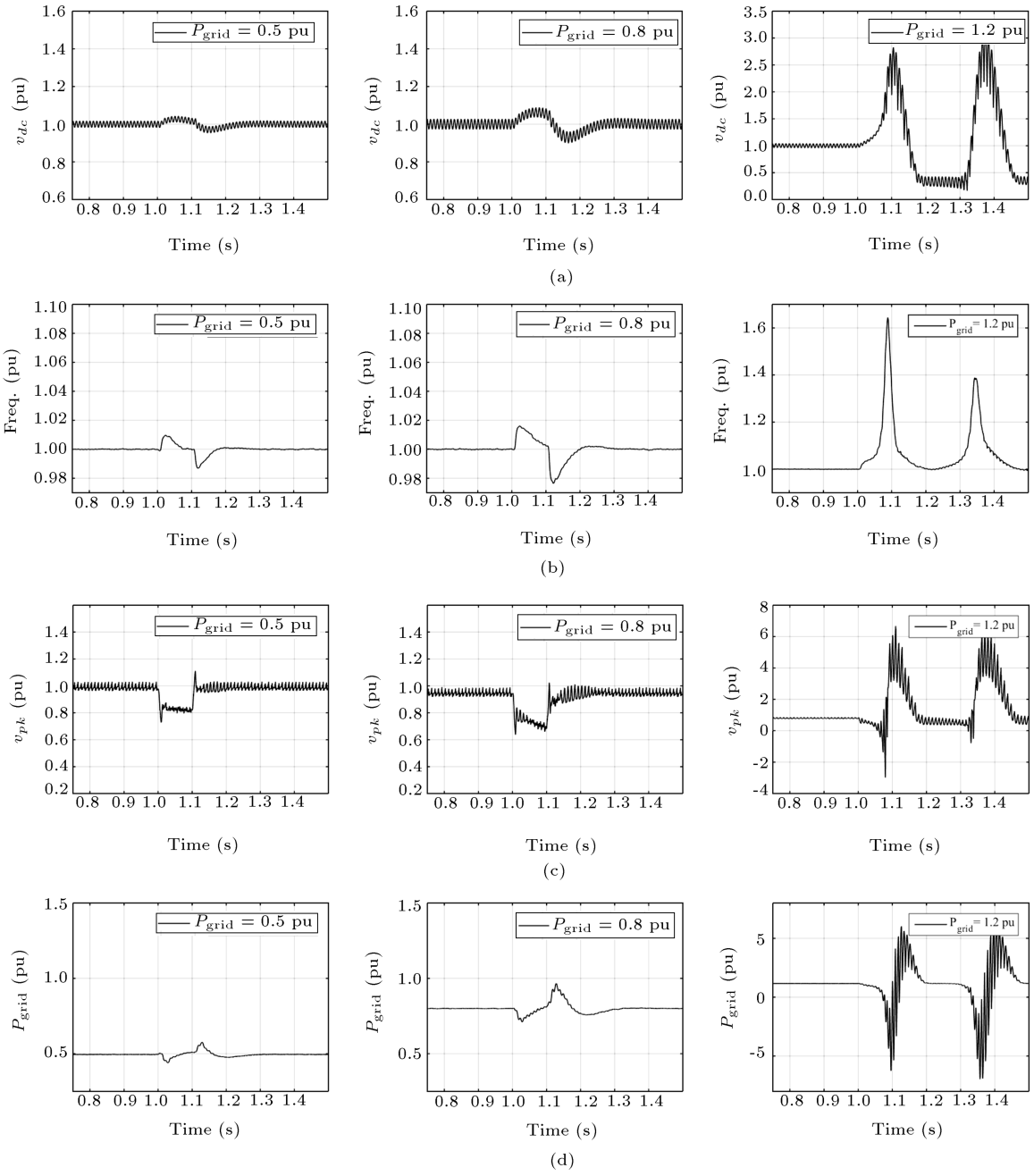

Figure 12. System response under different values of the SP-VSI output active power: (a) dc-link voltage, (b) estimated voltage frequency (f_{PLL}), (c) estimated voltage magnitude (v_{pk}), and (d) active power output.

under different values of the grid SCR, i.e., SCR = 10, 3, and 2. It is clear that the dc-link voltage has larger overshoot and longer settling time with the decrease of grid SCR, and system will become unstable when SCR reaches the value of 2 pu. Simulation results of Figure 11 confirm the output results of the modal analysis given in Table 3.

Figure 12 illustrates the time responses of the system under different values of the inverter output active power at SCR = 2.4. It can be seen that dc-link voltage has larger overshoot and longer settling time with the increase of the output active power, and the system will become unstable when the output active power is 1.2 pu. Simulation results of Figure 12 confirm the results of modal analysis in Table 4.

Figure 13 depicts the results of the study system for different values of the PLL bandwidth. It is clear that by increasing the PLL closed-loop bandwidth, the overshoot and ripples of the grid frequency and voltage peak detected by the PLL increase. Hence, in order to have a stable SP-VSI, the PLL closed-loop bandwidth should be limited below the threshold value.

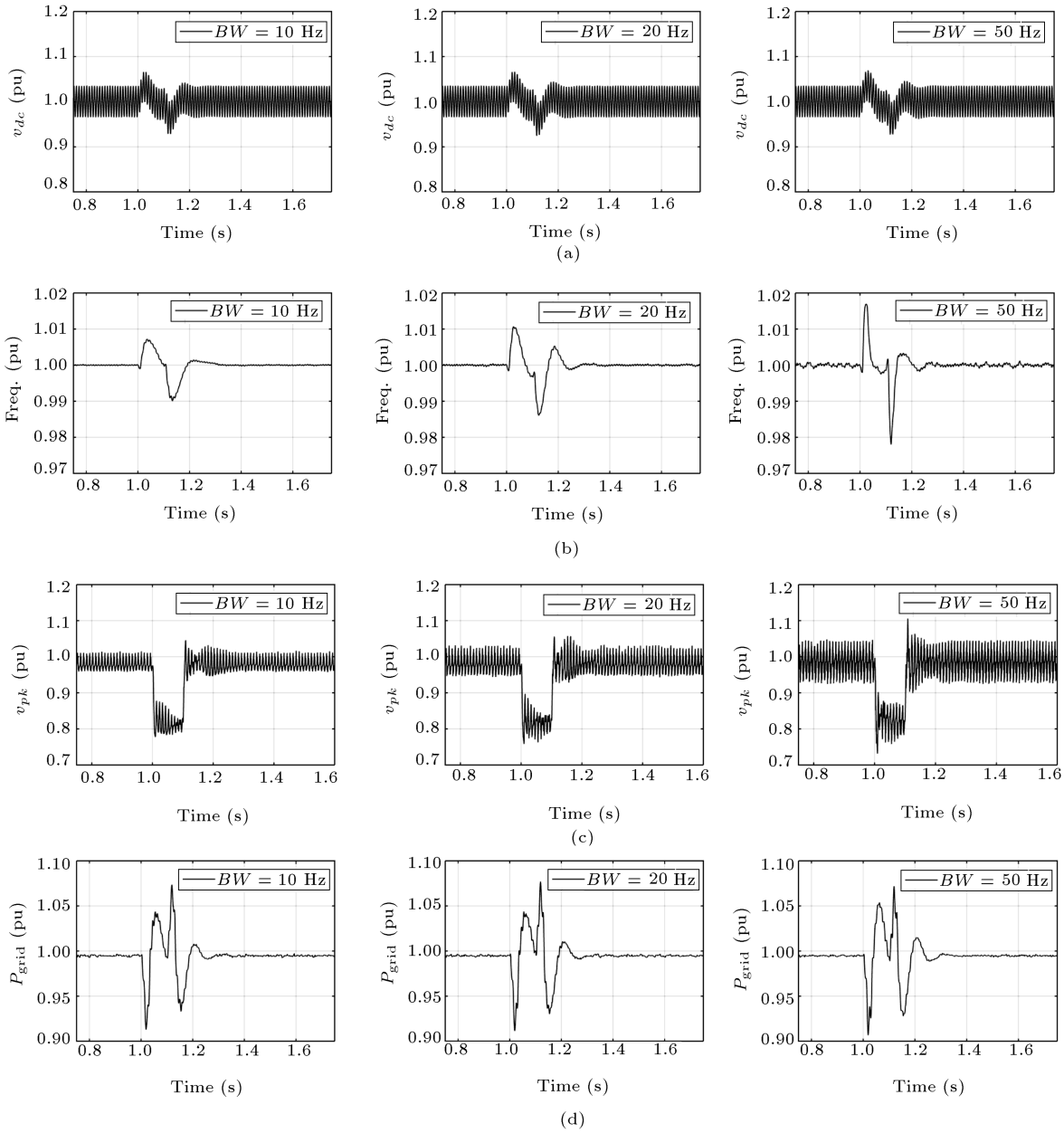

Figure 13. System response under different values of PLL closed-loop bandwidth: (a) dc-link voltage, (b) estimated voltage frequency (f_{PLL}), (c) estimated voltage magnitude (v_{pk}), and (d) active power output.

7. Conclusion

This paper evaluated the dynamic stability of the single-phase grid-connected PV inverter system while taking the PLL dynamics into account. The PLL structure employed in this paper includes two control loops: grid voltage phase estimation loop and grid voltage peak estimation loop. The paper proposed unified dynamic modeling of the SP-VSI system comprising PLL, dc-link dynamics, and grid; then, the linearized block diagram of the whole system was extracted. The linearized block diagram depicts the interaction between the control loops of the PLL and dc-link system. Next, small signal stability of the full system was presented, and impacts of the grid SCR, operating point, and PLL closed-loop bandwidth on the performance of the SP-VSI were examined. It was shown that the dc-link voltage had larger overshoot and longer settling time with the decrease of the grid SCR, and system would become unstable when SCR reached the value of 2 pu. In addition, the dc-link voltage had larger overshoot and longer settling time with the increase of the VSI output active power, and system would become unstable when the output active power was 1.2 pu. Further, it was shown that by increasing the PLL closed-loop bandwidth, the overshoot and

ripples of the grid frequency and voltage peak detected by the PLL increased. Hence, in order to have a stable SP-VSI, the grid SCR, the VSI output active power, and the PLL closed-loop bandwidth should be limited below the threshold value.

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Appendix A

System under study parameters

Table A.1 shows the current system's parameters used for the modal analysis and simulation studies.

Table A.1. System under study parameters.

Inverter parameters	Rated power	2 kw
	Switching frequency	15 KHz
dc-link	C_{dc}	640 μF
	V_{dc}	380 V
	$k_{P,dc}$, $k_{I,dc}$	0.07, 1.57
PLL	k_m	8.33×10^5
	$k_{P,PLL}$, $k_{I,PLL}$	184, 8464
Grid	Rated voltage (rms)	220 V
	Rated frequency	50 Hz
	L_g	$0.05L_{\text{base}}$
LCL filter	L_{f1}, L_{f2}	2.3 mH, 0.43 mH
	C_f, R_{cf}	6.6 μF, 1.9 Ω

Appendix B

Participation factors

For identifying the relationship between the states and the modes, the participation factor matrix is calculated using Eqs. (B.1) and (B.2):

$$p_i = \begin{pmatrix} p_{1i} \\ p_{2i} \\ \vdots \\ p_{ni} \end{pmatrix}, \tag{B.1}$$

$$p_{ki} = \frac{|\Phi_{ki}|\,|\psi_{ik}|}{\sum_{k=1}^{n} |\Phi_{ki}|\,|\psi_{ik}|}, \tag{B.2}$$

where n is the number of state variables, p_{ki} is the participation factor of the kth state variable into mode i, Φ_{ki} is the kth element of the ith right eigenvector of A, and ψ_{ki} is the kth element of the ith left eigenvector of A [32].

Biographies

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