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Fast detection of open-switch fault in cascaded H-bridge multilevel converter

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Abstract. Cascaded H-bridge converter has been utilized recently in different high-power applications due to its modular and simple structure. In order to have a balanced operation after a fault occurrence in this converter, it is necessary to detect the switch fault and its location. In this paper, a fast power-switch fault detection method is presented to identify a fault and its location. Only one voltage measurement per phase is required by this method, and the fault detection is faster compared to the existing methods. Moreover, it is suitable for implementation on an FPGA device due to the use of simple math, relational, and state machine blocks. The proposed method is verified by computer simulations and FPGA-based experimental tests.

1. Introduction

Multi-level converters have been used in recent years in a large number of power electronics applications due to their promising benefits over the conventional two-level converters, especially in high-power applications. Amongst structures for multi-level converters are diode clamped [1], flying capacitor [2], and Cascaded H-bridge (CHB) converters [3-8]. CHB consists of cascaded connection of H-bridges in each phase and, therefore, has been an interesting solution in high power applications due to its simple and modular structure. In this converter, each switching device has to withstand only a portion of the total voltage. Therefore, CHB can produce higher voltages while producing lower harmonics.

However, having a large number of devices significantly increases the risk of failure in one of the power converter switches. Therefore, it is important to detect and compensate for fault occurrence in these converters. Several methods have been proposed for the post-fault operation of multi-level converter [9-17], providing the possibility of balanced operation of the converter, even after a fault. The faster the fault is detected, the smaller its effect on the system performance will be. In addition, using a large number of additional sensors for Fault Detection (FD) will in turn increase the cost and reduce the system reliability; therefore, it is desired to lower the number of additional sensors as much as possible.

In this paper, the cascaded H-bridge converter and open-circuit power-switch fault detection are concerned. A diagram of a CHB converter is given in Figure 1.

Few fault detection schemes are proposed in the literature for detection of the fault and its location in CHB converters. A method based on voltage magnitude measurement is presented in [18], yet it is relevantly slow in detecting faults. A fault can be detected within one fundamental cycle (a few milliseconds) in

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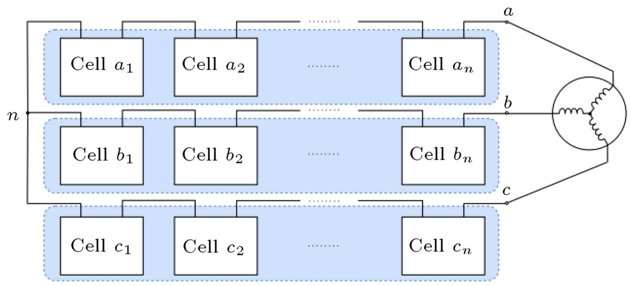

Figure 1. Three-phase CHB.

this method. In [12,19], some methods based on the artificial intelligence are proposed for the fault detection in CHB. In [12], Neural Network (NN) classification is used for fault diagnosis. A multi-layer perceptron network is used for detecting the type and location of the fault. Moreover, a genetic algorithm optimization technique is used to optimize the NN training. The fault detection time has been in place around six fundamental periods. Overall, this method is not very quick and is complicated for practical implementation; further, its performance depends on the correct training of the NN. A similar method is proposed in [19], which has the same drawbacks. In [20], the fault detection is based on the spectral analysis of the phase output voltage. The magnitude and phase angle of switching frequency component of the output phase voltage are observed in this method for fault detection. This method has better performance compared to previous ones; however, it uses a complicated approach to fault detection that is not very easy to implement. In addition, this approach may experience difficulties in finding faulty cell's location when a higher number of cells are utilized. In [21], Fast Fourier Transform is used on the output voltages to preprocess these signals. Then, PCA (Principal Component Analysis) is used to extract the fault signatures and, finally, multi-class Relevance Vector Machine (mRVM) is used to classify fault samples. Fault detection times of around 50-130 ms are reported in simulation and experimental test. However, the fault detection is very complicated, and still relatively slow.

In this paper, a very fast method for detection of open-switch faults is developed and, then, validated for multi-level CHB converters. This method is capable of detecting the fault and its location in a few hundreds of microseconds, which is several times faster compared to the previous methods [12,19,21] and is comparable with [20]. Moreover, the proposed method uses only simple math, relational and state machine blocks; therefore, its implementation on a digital target, such as FPGA, would be easy. Like previous methods, only the output phase voltage measurement is required; therefore, no additional cost is imposed on the system.

In the following, first, the multi-level CHB converter is reviewed. Then, in Section 3, the proposed fault detection method is detailed. The simulation results are provided in Section 4. The FD method is implemented on an FPGA, experimental tests are carried out, and the results are discussed in Section 5. Both simulation and experimental tests are in accordance and testify to the effectiveness and high performance of the proposed method.

2. Multi-level CHB converter

2.1. The structure

A three-phase CHB converter is shown in Figure 1. Each cell consists of an H-bridge inverter and an isolated *DC* source. One cell is depicted in Figure 2. Normally, all *DC* sources have the same *DC* voltage. The switches' commands in each leg of the H-bridge inverter are complementary. An additional switch, S_T, is used between the two output terminals of the cell, allowing the cell to be bypassed in case of a fault. In this way, other cells can continue powering the load [20].

Since each cell can produce three voltage levels, the maximum voltage level of each output phase will be $2n+1$, where n is the number of the cells per phase.

Different modulation methods are suggested for output voltage control of this topology. The most popular methods are Phase Shifted Pulse Width Modulation (PSPWM) and level-shifted PWM [21,22]. PSPWM method is the most suitable PWM which is recommended for cascaded H-bridge converters [23] and is extensively used for its ease of implementation, even for power distribution amongst the cells. Moreover, this method produces "n" times lower switching losses than the level shifted PWM [24]. In this paper, the PSPWM is concerned due to its better performances. In this method, each cell is controlled as a unipolar PWM inverter. The same reference signal is used in all unipolar PWM blocks of a given phase, while the carrier signals of the cells are shifted with respect to each other. In a CHB converter with "n" cells, the carrier signal of cell (i) is $180°/n$ shifted with respect to

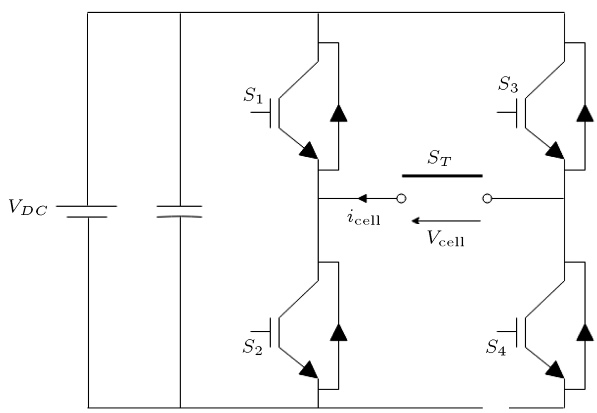

Figure 2. One elementary cell of the CHB with bypass switch.

the cell number $(i-1)$. For each cell, the second carrier that is required for its second leg (switches S_3 and S_4) is produced by negation of this carrier. Figure 3 shows the operation principle for an 11-level (five cells per phase) converter. The effective output frequency is $2n$ times the carrier frequency. Therefore, it is possible to have an equivalent high switching frequency at the output of the converter even by using a low switching frequency in each cell. Hence, the switching losses of each cell can be reduced. It is also evident that each switching has an effect on the output voltage, and as later is shown, it is possible to use this expected effect along with the measured output voltage to detect a fault.

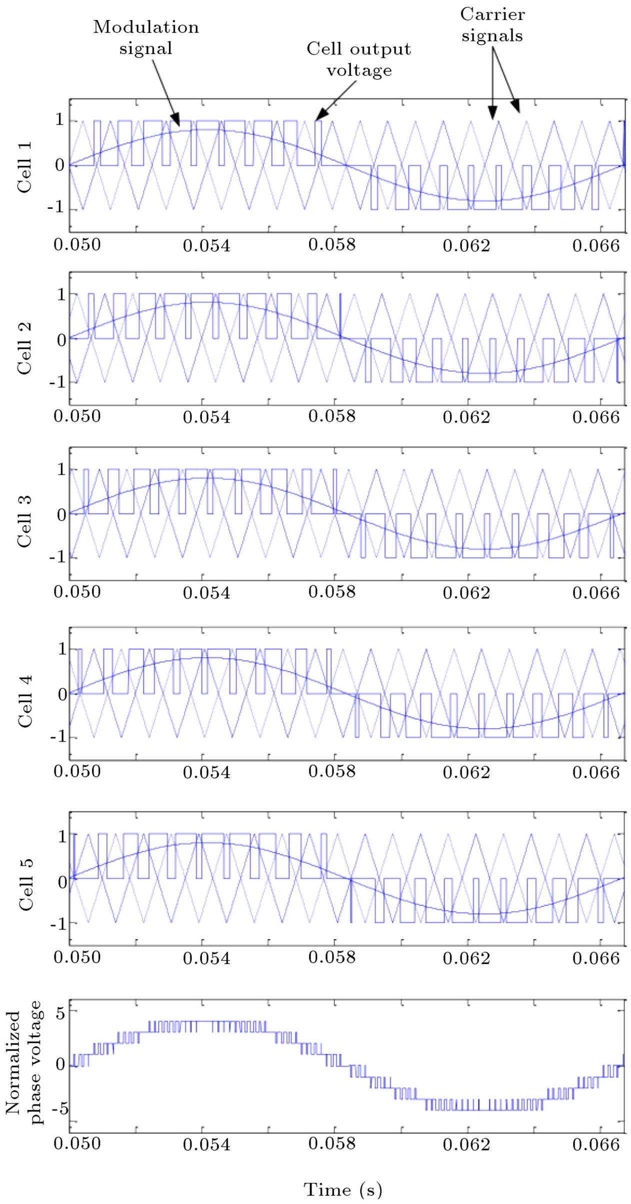

Figure 3. Normalized values of the modulation and carrier signals, the cell output voltages, and the phase output voltage in PSPWM for a five-cell (11-level) CHB converter.

3. Fault detection algorithm

Fast fault detection is mandatory in power electronics converters in order to minimize the undesirable behavior of the converter by changing the converter topology or the control method after fault detection. For *DC-DC* and conventional two-level converters, fast detection methods are proposed in [25,26]. In this paper, a generalized version of those method is proposed for the CHB converter that not only detects the fault, but also detects the faulty cell, which is necessary for the reconfiguration of the converter in order to be capable of using any of the post-fault control methods proposed in [12,16,18]. In this paper, open-circuit faults are considered. For short-circuit switch faults, normally, using fast-acting fuses, the converter topology will become similar to that after an open-switch fault [25], or special supplementary hardware is needed to detect the fault, as the software methods are not fast enough to detect the short-circuit switch faults. It is also worth mentioning that many drivers have the possibility to identify the short-circuited switches and stop the operation [27,28]. Nonetheless, this is outside the scope of this paper.

3.1. Fault detection

In the ideal condition, an open-switch fault can be easily detected by comparing the measured and estimated phase voltages of the converter. By considering a single cell (cell C) in one phase of a CHB converter as shown in Figure 2, let us assume that the fault is in S_1 switch. Clearly, the observations can be generalized to other switches as well. Gate command for switch k is shown with $T_k \in \{0,1\}$, and commands for two switches in each leg are complementary. The phase output current is shown by i_{cell}, and V_{DC} is the DC voltage at the input of the cell (see Figure 2). For a fault in S_1, when $T_1T_3 = 10$ and $i_{\text{cell}} < 0$, diode D_{S2} conducts instead of S_1; therefore, while the estimated output voltage is V_{DC}, the measured voltage would be equal to 0. If $i_{\text{cell}} > 0$, diode D_{S_1} conducts and the converter would behave normally; therefore, no fault in the system can be detected. For the fault in S_1, estimated and measured voltages of the cell and the error between them are resumed in Table 1. Herein, $V_{es,C}$ and $V_{m,C}$ represent the estimated and measured voltages of cell 'C', respectively. It is assumed that

Table 1. Estimated and measured voltages in case of an open switch fault in S_1 in cell C.

T_1T_3	$V_{es,C}$	$V_{m,C}$	Error $V_{es,C} - V_{m,C}$
00	0	0	0
01	$-V_{DC}$	$-V_{DC}$	0
10	$+V_{DC}$	0	$+V_{DC}$
11	0	$-V_{DC}$	$+V_{DC}$

$i_{\text{cell}} < 0$; therefore, the fault in S_1 will affect the output voltage of the cell.

Since the measured and estimated voltages are equal in normal operation in other cells, the total error between measured and estimated voltages can be written as follows:

$$V_{es} - V_m = V_{es,C} - V_{m,C} = +V_{DC}. \qquad (1)$$

Therefore, the fault in any of the switches can be effectively detected.

However, in practice, the estimated and measured voltages are always different, mostly due to measurement and discretizing errors, and more importantly because of non-ideal behaviors of the switches and the drivers, such as turn-off and turn-on delay times and dead time generated by the controllers or drivers. Therefore, to avoid false detection, separate time and voltage criteria must be adopted to account for the probable time and voltage mismatches. On the other hand, in order to make the fault-tolerant control possible, not only the occurrence of a fault, but also its location must be detected. Generally, it is necessary to detect the faulty cell and bypass it to continue the operation of the converter. The proposed method is designed to account for voltage mismatches and detect the fault and its location very quickly.

Figure 4 shows the proposed detection method. Only one voltage measurement per phase is required by this method, and it consists of simple blocks that make its implementation on FPGA easy. First, the estimated voltage is produced using the gate commands of the switches and DC voltages of the cells. Then, error between estimated and measured voltages is calculated. Fault is detected by evaluating this error, using two levels of mismatch compensation for voltage and time, as discussed before. First, two comparators check if the voltage error amplitude is large enough. If the voltage error is larger than C_V or smaller than $-C_V$, output of these comparators becomes '1'. As previously observed, a fault will induce a voltage error equal to $\pm V_{DC}$; thus, choosing $C_V = V_{DC}/2$ seems very reasonable for voltage mismatch compensation.

Assuming that the fault detection algorithm operates with a 500 kHz clock, a moving sum is then performed for 15 sampling periods (equal to a window length of 30 μs) on these outputs to see in how many samples the voltage error has been considerable. Moving sum, also known as the running sum, is a simple form of a Finite Impulse Response (FIR) filter and is defined as the sum of elements over a moving window of values with length N, as shown in Eq. (2):

$$y(n) = x(n) + x(n-1) + \cdots + x(n-N+1). \qquad (2)$$

Herein, the moving sum shows in how many of the last observed samples (the observation window) the input has been equal to one.

The outputs of the moving sum blocks are investigated then, and if they are larger than C_t, then one can be sure that a fault has occurred somewhere in the circuit. Since the observation window considers 15 samples, C_t is chosen equal to 12.

3.2. Fault location identification

After fault detection, it is necessary to detect the fault location as well. Herein, a simple, yet effective, method is used because the voltage error disappears and the converter acts normally again when the command of the faulty switch goes back to zero. The third comparison and moving sum unit detect the fault removal and signal it to the Fault Detection State Machine (FDSM). As it is visible in Figure 4, when the error voltage is less than C_V and larger than $-C_V$ for at least C_t samples, one can be sure that there is no fault in the system, and the *Fault_removed* input of the FDSM will become equal to 1. The FDSM is shown in Figure 5.

If a fault is already detected, one of the *Fault_positive* or *Fault_negative* states in FDSM is active, and the SM is waiting for the fault removal signal (*Fault_removed*) to arrive. When this signal arrives, it is only necessary to investigate in which cell(s) a switching has occurred among previous C_t samples. This is done by means of D_ip and D_in signals. Figure 6 shows D_ip and D_in generations for one cell. For each cell, basically, these signals show if a switching is commanded that increases or decreases the cell's output voltage in the last C_t sampling. In

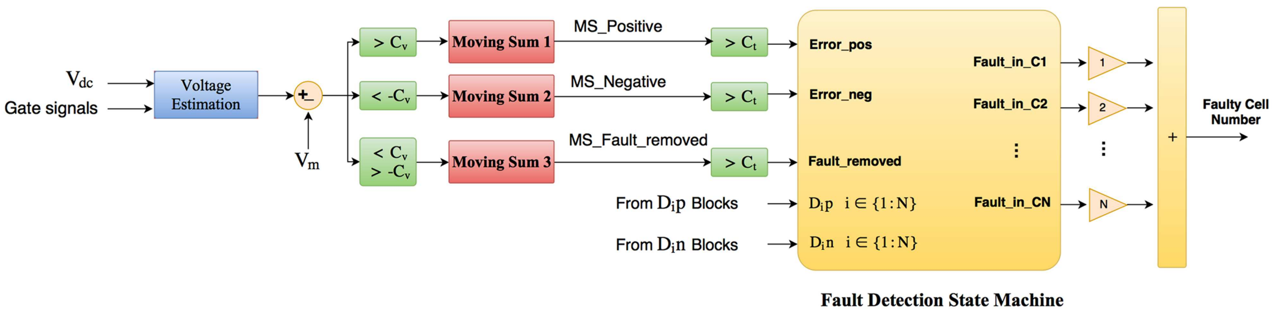

Figure 4. Proposed fault detection scheme for CHB converter.

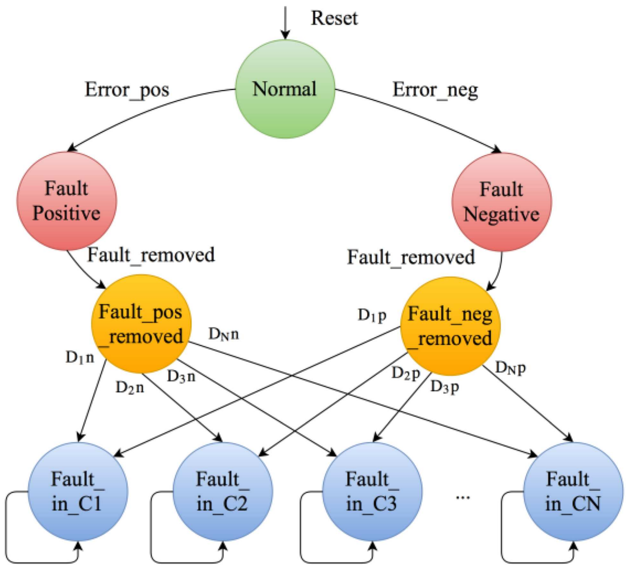

Figure 5. Fault detection state machine.

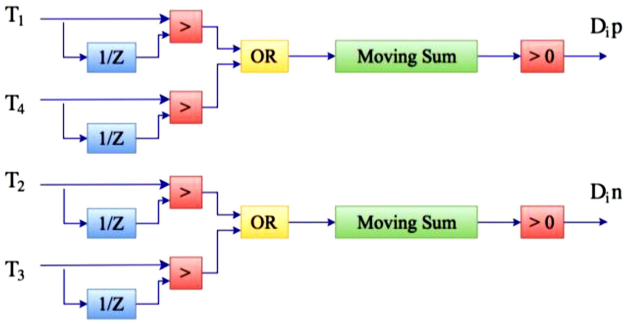

Figure 6. Generation of D_ip and D_in signals.

other words, D_ip means that a positive voltage step is commanded, and D_in means that a negative voltage step is commanded.

Basically, a switching in S_1 or S_4 will tend to increase the output voltage by V_{DC}, while a switching in S_2 or S_3 will decrease it by V_{DC}. That is why T_1 and T_4 are associated with D_ip (positive voltage step), while T_2 and T_3 are associated with D_in (negative voltage step) in Figure 6. If the error is positive and the fault removal signal arrives, it can be concluded that a decreasing switching has occurred, which corresponds to one D_in signal going high. Based on D_in signals, the next state in the FDSM can be detected. For a negative error, similar reasoning applies. The FDSM stays in the faulty states (*Fault_in_Ci*, $i \in \{1 : N\}$) upon entering them, as long as a reset signal is not applied.

Finally, *Fault_in_Ci* outputs go high when the corresponding state is active. These outputs may be used in the fault-tolerant scheme to reconfigure the structure and control appropriately. In Figure 4, their information is combined to determine the faulty cell's number.

It is worth mentioning that after reconfiguration, the FDSM can be reset, and fault detection will

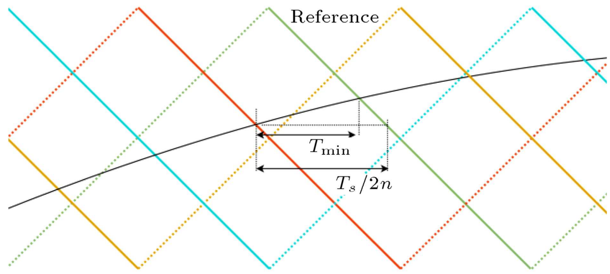

Figure 7. Minimum time between two consecutive rising levels.

be again possible for other switches, as long as the necessary changes in the calculation of the estimated voltage are applied.

One special condition is particularly interesting when two switchings have occurred in two legs during the last C_t sampling periods, because it is important to detect which one has been responsible for fault removal. In other words, it is important that only one D_ip and D_in signal be present in the observation window; otherwise, the FDST cannot decide between two D_ip or D_in signals. Figure 7 shows an example of such a condition for a Phase Shifted PWM (PSPWM). Referring to Figure 3, it can be verified that when a carrier becomes larger than the modulation signal, voltage of the corresponding cell will experience a $+V_{DC}$ change (rising level), and vice versa. The modulation signal frequency is several times smaller than the carrier frequency; therefore, it can be confirmed visually in Figure 7 that the minimum time between two $+V_{DC}$ or two $-V_{DC}$ transitions is equal to:

$$T_{\min} \cong \frac{1}{2Nf_s}. \tag{3}$$

If this minimum time is larger than the sampling window, the fault detection algorithm sees only one positive or negative transition; therefore, it can detect any fault effectively. Normally, this minimum time is at least several times larger than the length of sampling window. Herein, a conservatively large window time of $T_{\text{window}} = 30\ \mu$s is used in accordance with the value for experimental setups reported in [25]; therefore, if $T_{\min} > 30\ \mu$s, the FDA can work correctly. For a 5-cell converter, this translates to switching frequency calculated below:

$$f_s < \frac{1}{2 * 5 * 30\ \mu\text{s}} = 3333\ \text{Hz}. \tag{4}$$

Normally, the switching frequency is well beyond this limit, even with the conservative choice of T_{window} in this study.

4. Simulation results

Simulations are carried out to evaluate the effectiveness of the proposed method. A five-cell (11-level) three-phase CHB converter is simulated. DC-link voltages of the cells are equal to 1700 V. The fundamental switching frequency is equal to 1000 Hz, resulting in a $2 * n * f = 2 * 5 * 1000 = 10$ (kHz) equivalent switching frequency. We consider an open-loop control of the converter, and by using PSPWM, it generates a sinusoidal voltage at the converter's output. A fault is introduced in switch S_1 of cell 2 at $t = 0.035$ s. The fault detection algorithm operates with a 500 kHz clock. Since the estimated and measured voltages are different, *MS_positive* or *MS_negative* (Figure 4) signals will start to increase based on the sign of the voltage error, and when one of them becomes greater than 12, the fault is detected and one of the *Fault_positive* or *Fault_negative* states will become active.

Herein, the estimated and measured voltages of the faulty phase are shown in Figure 8. The voltage error is shown in Figure 9. As expected, a fault in S_1 has resulted in a $+V_{DC}$ error in phase voltage. It is also shown in the figure that, in certain periods of time, the voltage error disappears. This is due to a decreasing switching command used for identification of the fault's location.

Outputs of Moving Sum 1 and Moving Sum 3 blocks are shown in Figure 10. *MS_positive* signal starts to increase when a large enough positive voltage error exists. When it passes $C_t = 12$, a fault can be detected, and the FDSM goes to the *Fault positive* state. *MS_Fault_removed* signal starts to increase when the converter is acting normal or when the voltage error is smaller than its limits. It can be seen that during normal operation of the converter, this signal has a usually high value, but immediately after the fault occurrence at $t = 0.035$, it goes down to zero. However, when the fault is removed due to switching in the faulty cell, this signal goes high again.

Figure 11 shows the moment that the FDSM has reached its final stage as well as the final result. Fault location is correctly detected. In addition, the fault detection has been very fast. The fault is detected in less than 200 μs.

Figure 12 shows the details of the identification of fault location. The *MS_Fault_removed* signal is repeated here and shown with dashed lines. When this signal goes higher than 12, the FDSM will enter the *Fault_positive_removed* state and, then, will choose its next state based on D_in signals. It is shown in Figure 12 that D_2n is high, meaning that the fault disappears as a result of switching in cell 2. Therefore, the next and last state in FDSM will be *Fault_in_C2*, and the faulty cell number will be equal to 2.

It is worth mentioning that since fault detection uses the switching information of the faulty cell, in the worst case, the fault detection may take up to one switching period. On the other hand, the minimum detection time happens when a fault is followed by

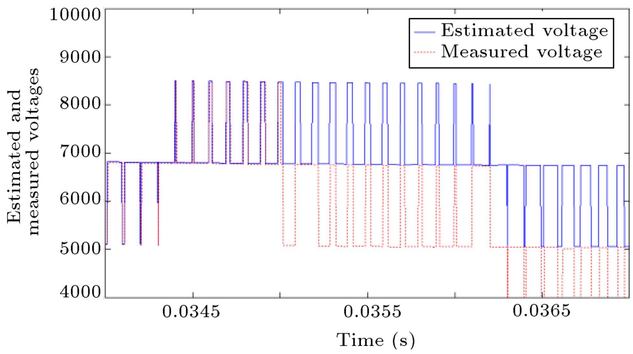

Figure 8. Estimated and measured phase voltages for a fault at $t = 0.035$ s.

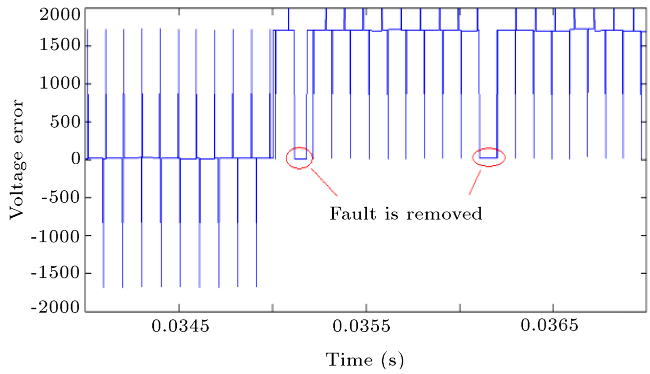

Figure 9. Voltage error between estimated and measured phase voltages for a fault at $t = 0.035$ s.

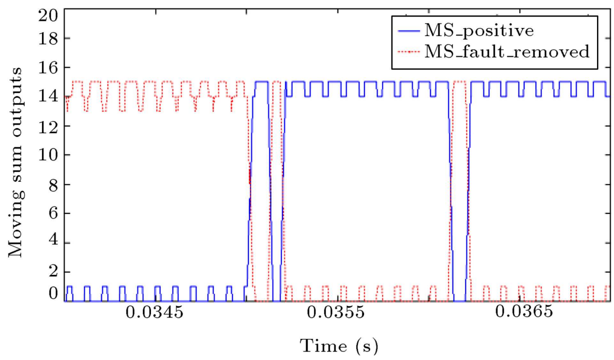

Figure 10. Output of moving Sums 1 and 3 for a fault at $t = 0.035$ s.

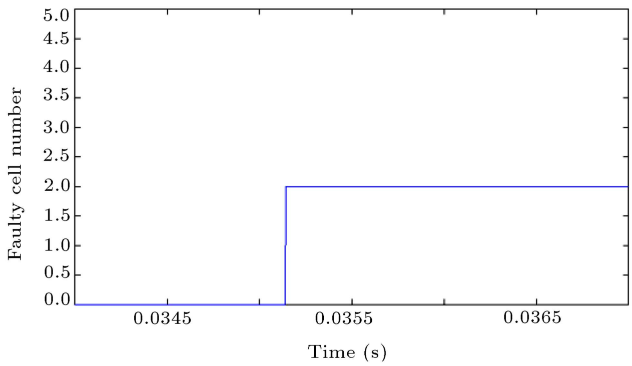

Figure 11. Detection of the fault and its location for a fault at $t = 0.035$ s.

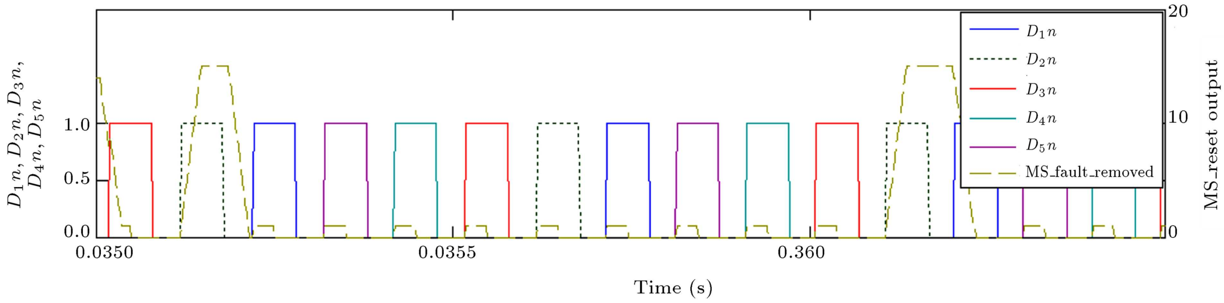

Figure 12. Detection of fault location.

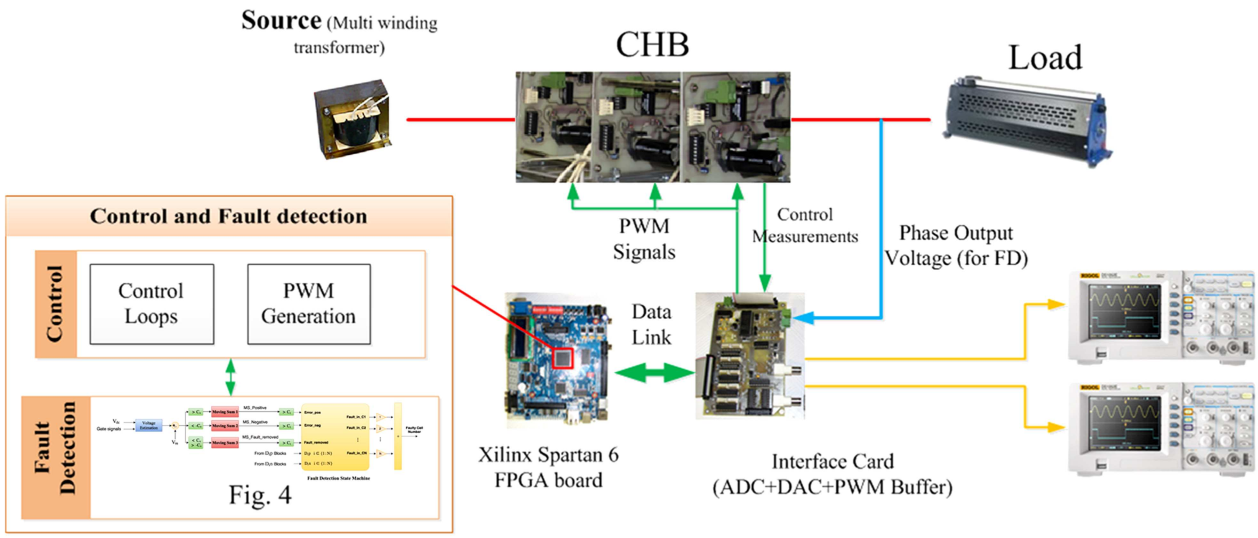

Figure 13. The experimental setup.

Error_pos or *Error_neg* signals and, then, consequently followed by *Fault_removed* signal, without any delays in between. In this case, the fault detection will take $2C_t$ samples, which is equal to 48 μs here. Moreover, fault detection has an inherent robustness as a result of the windowing technique that makes it possible to observe a signal for a long enough time before making any decision. The detection time is several times smaller than the values reported in [12,18,19] and is comparable to the result of [20]. However, this method is simpler than the method proposed in [20] which needs complicated frequency spectrum analysis. In addition, due to the use of simple math, comparison and state machine blocks, it is better suited for implementation on an FPGA.

5. Experimental results

In order to verify the effectiveness of the proposed scheme further, an experimental setup has been built in our laboratory. Figure 13 shows the structure of this setup. A seven-level CHB is implemented by cascading three cells in each phase. For switches, IRF540 MOSFETs are used and HIP4082 bridge drivers are used for gating them. The control and fault detection schemes are implemented on a XC6SLX9 Spartan 6 FPGA from Xilinx, which has over 9 k logic cells. An interface board is built as well with ADC, DAC, and PWM buffer functions. AD7829 is used for analog to digital conversion, with 500 kSPS conversion rate on each of its 4 used channels. AD7302 two-channel DAC with 8-bit resolution and maximum 2 us settling time is used for visualization of the digital fault detection signals. The control and detection use a clock of 500 kHz. All the delays on the control and detection loop (including the A/D conversion, switch on and off time and deadtime, driver and optocoupler delay) are estimated to be less than 10 us; therefore, a conservative observation window for FD is chosen equal to 30 us. Waveforms are captured using two two-channel oscilloscopes that are externally triggered by the fault occurrence signal.

A fault is applied to S_1 in *Cell*1 via a push button on the FPGA board. Fault is produced by setting the gate command of the faulty switch to zero. Figure 14 shows the fault detection signals. The outputs of MS1 (*MS_positive*) and MS3 (*MS_Fault_removed*) are shown in this figure. These two signals are visualized using two DAC outputs on the interface board. Since a

Table 2. Comparison of fault detection times of different methods.

Method	Complexity	Fault detection time
AI-based [12,19]	Complex (NN training)	6 fundamental cycles
Method of Yazdani et al. [18]	Simple	About 1 fundamental cycle
Voltage frequency analysis [20]	Complex (frequency analysis)	$\leq T_s$ (1 switching cycle)
PCA + mRVM [21]	Complex	50-130 ms
Proposed method	Simple	$\leq T_s$ (1 switching cycle)

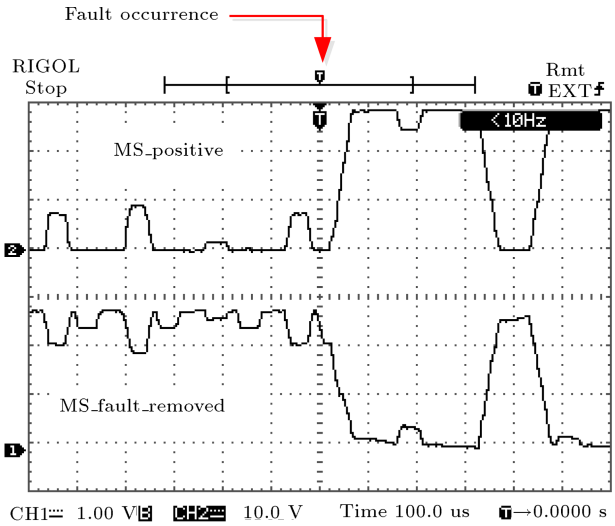

Figure 14. Inputs to FDSM, from top to bottom: *MS_positive* and *MS_Fault_removed*.

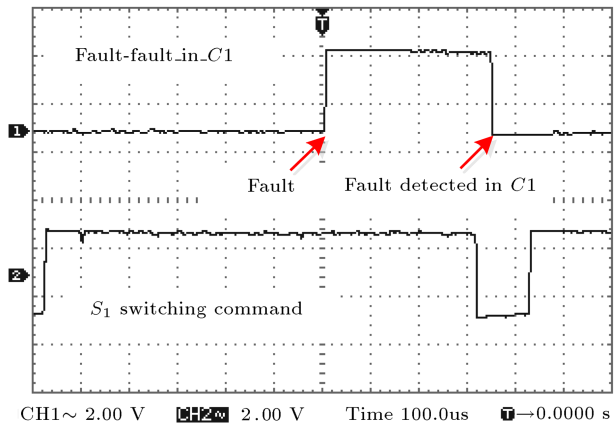

Figure 15. Fault detection signals, from top to bottom: *Fault-Fault_in_C*1, S_1 switching command.

fault in S_1 will result in a positive voltage error, only the output of the positive moving sum (*MS_positive*) is shown, and *MS_negative* does not include useful information; hence, it is not observed.

Before fault occurrence, the *MS_positive* has a limited output value. Small fluctuations in *MS_positive* before fault occurrence are mostly due to the delays and deadtime in the system. However, it can be verified that when the fault is applied, there will be a positive voltage error for a considerable amount of time; hence, the *MS_positive* will start to increase to higher values. The *MS_Fault_removed* output will decrease accordingly.

Figure 15 shows the details of fault occurrence and fault detection moments as well as the switching command of the faulty switch. These waveforms are also captured upon fault occurrence and, hence, have the same timing characteristics of those of Figure 14. Fault occurrence and fault detection are merged into one signal and shown in this figure as Fault- *fault_in_C1* to empty the second axis for the switching signals of the faulty switch. From these two figures, it is obvious that when the switching signals of the faulty switch return to zero, the converter acts normally again. Therefore, as seen in Figure 14, the *MS_Fault_removed* output will increase and *MS_positive* output will decrease. Once the *MS_Fault_removed* reaches its threshold, the FDSM of Figure 4 will detect the faulty cell. The difference between fault and *Fault_in_C*1 is reduced to zero after this point, which attests that the fault and its location are correctly detected. The fault detection in this particular example has been around 350 us. Obviously, fault is detected in 30 us after the first turn-off command of the faulty switch; therefore, as previously mentioned, fault detection can be as fast as 2*observation window (60 us in this case), and in the worst case, it can take up to one switching period. Therefore, while the clock rate of FPGA and possibly the sampling rate of the ADC can be higher, higher values do not increase the fault detection speed further and, hence, are not necessary.

Table 2 summarizes the fault detection time in this paper with the other methods available in the literature. Overall, the experimental results are in accordance with the simulation results and show the effectiveness of the proposed method for fast fault detection in CHBs. The output of this fault detection method can be used in order to make a fault-tolerant system that is able to use the information of fault and its location to reconfigure the system and its control in order to make the continuity of service possible.

6. Conclusion

In this paper, a very fast method for detection of open-switch faults in cascaded H-bridge converters was proposed. This method only needs one voltage measurement per phase and is fast and robust for the detection of semiconductor open-switch fault and its location. The proposed method detects faults by comparing the estimated and measured phase voltages of the converter. It should be noted that when the faulty switch command is equal to zero, the converter will act normally again; thus, fault location is found accordingly. Only simple math, relational and state machine blocks are used in the process; therefore, the implementation of this approach on a digital target, such as FPGA, will be easy. The detection time will be at maximum equal to one switching period and can be as low as a few tens of microseconds. Simulations and experimental results are carried out, and their results show the high performance of the proposed method. Fault is detected in 350 μs. The output of this detection method can be used in fault-tolerant control schemes to ensure the continuity of service of the converter after a fault occurrence.

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