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Invited/Review Article

A survey of bandgap and non-bandgap based voltage reference techniques

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Voltage reference.

Abstract. The design challenges of voltage reference generators in CMOS technology have increased over the years in low-voltage low-power CMOS integrated circuits, constituting analog, digital, and mixed-signal modules. The emergence of hand-held power autonomous devices pushes the power consumption limit to nW regime. Along with these confrontations, limited full-scale range of data converters at low supply levels demands accurate reference voltage generators. This paper reviews the allied design challenges and discusses the evolved methodologies to tackle them. This paper also prominently surveys the sub-1 V voltage reference topologies presented in the literature along with classic bandgap based voltage reference topologies. Non-bandgap (only CMOS) based reference architectures are proven to be area- and power-efficient, but always have to be accompanied with auxiliary on/off chip trimming mechanism for high accuracy. We also provide insightful analysis of the voltage reference topologies required by the designers.

1. Introduction

An accurate voltage reference is an important block in most of the Integrated Circuits (ICs). It establishes a reference voltage point for the rest of the circuit blocks in a complete system to achieve reliable and predictable performances. It can be used with a regulator to build a power-supply, in an operational amplifier to set up bias voltages, and/or in data converters to establish a standard voltage for comparison. The accuracy of the reference voltage often decides on the overall performance of a system.

Operating principle of the circuit adds a voltage that decreases linearly with temperature to one that increases linearly with temperature to produce a reference voltage that is constant with respect to temperature in the first order. The base-emitter voltage (V_{BE}) of a bipolar transistor decreases linearly with temperature, i.e. it has a Complementary-To-Absolute-Temperature (CTAT) dependence. The voltage that increases linearly with temperature, i.e., the Proportional-To-Absolute-Temperature (PTAT) voltage, is produced through the difference in the values of V_{BE} in two bipolar transistors operating under different current densities. A bandgap reference circuit adds these CTAT and PTAT voltages to produce a temperature-invariant voltage V_{REF}. The value of the reference voltage is close to the bandgap voltage of silicon (1.2 V).

This paper is a survey of voltage reference topologies since they were presented in the year 1971. We would like to explain the terminology, in which bandgap/sub-bandgap voltage references are the topologies that give the output voltage $\approx$ 1.23 V or up/downscaled version of that. Also, non-bandgap voltage references or voltage references generally do not constitute any bi-polar device/s. Therefore, these voltage reference circuits are not bound to give $\approx$ 1.23 V

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or scaled versions of 1.23 V. That means, non-bandgap voltage references mainly have only MOSFETs and/or resistors. The paper is basically divided into three parts. In the first part, we have discussed the classic reference generator topologies. These topologies are generally bandgap based. The second part of the paper deals with the reference topologies broadly proposed after 1997. Researchers started working on sub-1 V bandgap voltage as technology started shrinking and resulted in drastic fall of operating supply voltage. Finally, the third part of the paper discusses the curvature correction techniques that improve the accuracy.

2. Definition of performance indices

There are several different performance indices used to specify and compare voltage references. They are listed below:

1. Temperature Coefficient (TC);
2. Minimum operable supply voltage;
3. Power consumption;
4. Noise;
5. Line Sensitivity (LS);
6. Power Supply Noise Attenuation (PSNA);
7. Area consumption.

Some of these parameters like area, power consumption, and minimum supply voltage are quiet straight- forward, while others require explanations. Many of the indices are vulnerable to the characteristics and variations of the fabrication process.

Actually, the TC of a voltage reference has been presented in many ways. However, researchers commonly use the effective Temperature Coefficient (TC). It is given in Eq. (1). It measures the maximum variation of the voltage reference across a specific temperature range ΔT and normalizes this value against the nominal V_{REF} at room temperature. Its unit is ppm/°C.

$$TC = \frac{V_{\mathrm{REF}_{\max}} - V_{\mathrm{REF}_{\min}}}{V_{\mathrm{REF}_{\mathrm{nom}}} \Delta T}. \tag{1}$$

Another important performance index is the ability of the voltage reference to reject supply variations. This measurement at DC is called Line Sensitivity (LS) or Line Regulation (LR), given by Eq. (2), and measured in mV/V. Its frequency behavior is given by Eq. (3), called Power Supply Noise Attenuation or PSNA [1], and measured in dB. The PSNA response is primarily evaluated at two frequencies, i.e. 100 Hz and 1 MHz (as low-frequency and high-frequency responses).

$$\mathrm{LS} = \frac{V_{\mathrm{REF}_{\max}} - V_{\mathrm{REF}_{\min}}}{\Delta V_{DD}}, \tag{2}$$

$$\mathrm{PSNA}(\omega) = \frac{V_{REF}(w)}{V_{DD}(w)}. \tag{3}$$

As with every electronic circuit, the intrinsic device noise is one of the limiting accuracy factors. For recent voltage references, its power spectral density is usually specified at 100 Hz (low frequency) for comparison purposes, while the total RMS noise depends on the chosen bandwidth. Noise parameters are not discussed here, as all the mentioned papers did not mentioned it specifically.

Above discussed are the main performance indices used to specify and compare voltage references. We will use them extensively in the review of recent circuits. Besides the obvious design considerations, there are other design considerations in a voltage reference circuit that are important and that, at the same time, also affect the above performance parameters. Among these are circuit size and power dissipation. These two are becoming more important parameters as hand-held devices are becoming popular. We have extensively considered these parameters for our study.

3. Classic voltage references

One of the first bandgap voltage reference circuits was presented by Robert Widlar of the National Semiconductor in 1971. It is well-known as the Widlar's bandgap voltage reference circuit [2]. The Widlar bandgap voltage reference circuit was implemented with the conventional bipolar technology, of which the complete circuit is shown in Figure 1.

The Widlar bandgap voltage reference circuit gen-

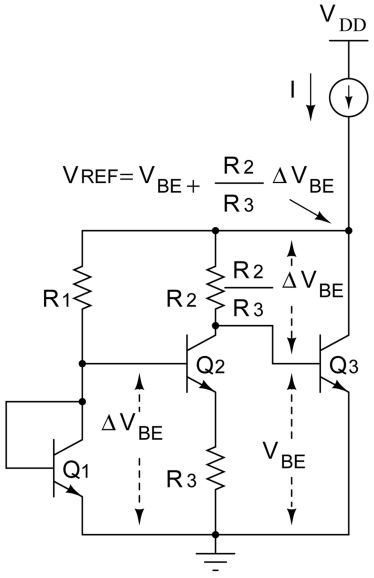

Figure 1. Widlar voltage reference: 1971.

erates a stable low-TC reference voltage at 1.23 V. This implementation of a bandgap voltage reference circuit was successfully applied in the National Semiconductors voltage regulator integrated circuit LM 113, which proved capable of achieving an output voltage with low TC. Since then, it has been applied in many voltage regulator ICs to generate the internal reference voltage/s.

3.1. Robert Widlar's voltage reference: 1971

One of the oldest $V_{\rm BE}$ and $\Delta V_{\rm BE}$ compensated bandgap voltage reference circuits is the Widlar bandgap voltage reference circuit introduced by Robert Widlar in 1971. These bandgap circuits are based on the principle shown in Figure 1. The transistors Q_1 and Q_2 are operated at different current densities to produce temperature-proportional voltages across R_3 and R_2. A third transistor Q_3 is used to sense the output voltage through R_2. As a result, Q_3 drives the output to a voltage which is the sum of $V_{\rm BE}$ of Q_3 and the temperature-dependent voltage across R_2. When the output voltage is set to approximate the bandgap voltage of silicon, the voltage across R_2 will compensate the temperature coefficient of $V_{\rm BE}$, and the output voltage will be temperature-invariant.

Furthermore, the thermal voltage (V_T) extracted from the $\Delta V_{\rm BE}$ of two BJTs with different emitter areas and, hence, different current densities will form the PTAT voltage, while the base-emitter voltage ($V_{\rm BE}$) of the BJT will form the CTAT voltage. The circuit is simple, but not easy to implement in modern CMOS process or to control the output, because the BJTs implemented in the CMOS process are sensitive to process variation.

In this circuit, Q_1 is operated at a relatively high current density. The current density of Q_2 is about 10 times lower and the emitter-base voltage difference $\Delta V_{\rm BE}$ between the two devices appears across R_3, defining the emitter current and the collector current if the transistor gain is high. Q_3 then works as a current gain stage, also providing the $V_{\rm BE}$ voltage necessary to form the output. A simplified analysis of the circuit follows.

The collector current IC of a BJT is written as:

$$I_C = I_0 \left[\exp\left(\frac{V_{\rm BE}}{\eta V_T} - 1\right)\right]. \tag{4}$$

where I_0 is a process-dependent constant, $V_{\rm BE}$ is the base-emitter voltage, η is the emission coefficient, and V_T is the thermal voltage. If two transistors are operated with different collector current densities, J_i, then the difference of their base-emitter voltages is given by Eq. (5).

$$\Delta V_{\rm BE} = V_T \ln\left(\frac{J_1}{J_2}\right). \tag{5}$$

In Figure 1, one can see that the output of the bandgap reference (BGR) proposed by Widlar is given by the sum of the base-emitter voltage of Q_3 and the multiplied PTAT term on R_2, as shown by Eq. (6):

$$V_{\rm REF} = V_{\rm BE} + \frac{R_2}{R_3}\Delta V_{\rm BE}. \tag{6}$$

For the time being, we consider that $V_{\rm BE}$ can be expressed by the linear expression $V_{\rm BE} = V_{\rm BG}CT$, where $V_{\rm BG}$ is the silicon bandgap voltage at 0 K, C is a constant, and T is the absolute temperature. Other higher-order temperature effects will be studied extensively in Section 7. Therefore, R_1 and R_2 can be scaled together with the current density difference of Q_1 and Q_2 to achieve $dV_{\rm REF}/dT = 0$.

3.2. Kuijk's voltage reference: 1973

Among the various existing bandgap voltage reference architectures to date, one of the most ubiquitous ones is the Kuijk bandgap reference circuit, shown in Figure 2 [3]. Reference voltage $V_{\rm REF}$ is evaluated as the sum of the voltage drops across R_1, R_3, and the base-emitter voltage of D_1 ($V_{\rm BE,1}$). If opamp gain is very high, reference voltage is:

$$V_{\rm REF} = V_{\rm BE} + V_T\left(1 + \frac{R_1}{R_3}\right)\ln\left(\frac{I_{S1}R_1}{I_{S2}R_2}\right), \tag{7}$$

where I_{S1} and I_{S2} represent the saturation currents of D_1 and D_2. The first term in Eq. (7) is Complementary To Absolute Temperature (CTAT) and the second term is V_T-based, i.e. Proportional To Absolute Temperature (PTAT). The sum of both is trimmed with scaling factor (selecting proper resistor values) to achieve temperature-insensitive reference voltage.

3.3. Brokaw's voltage reference: 1974

The important fact is that the Widlar's circuit neglects the effect of base current flowing in R_1 and R_2. The variability in this current due to processing and temperature effects on beta (feed-forward current gain)

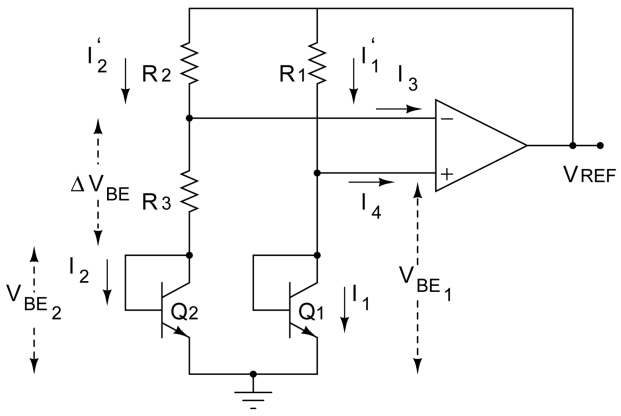

Figure 2. Kuijk voltage reference: 1973.

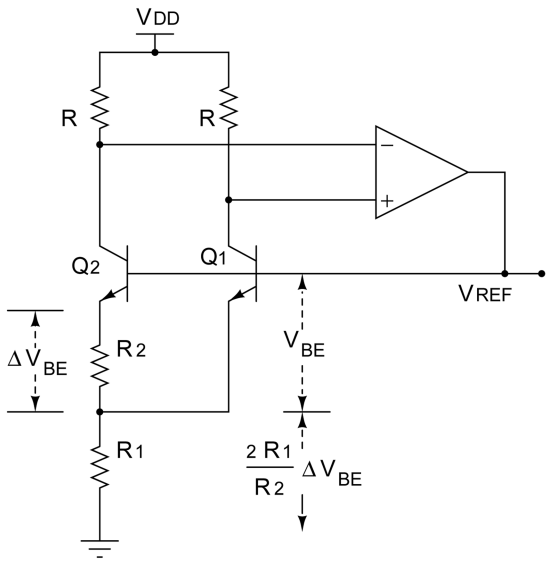

Figure 3. Brokaw voltage reference: 1974.

gives rise to an output voltage error and drift. This effect is particularly severe when the current in D_1 is made much smaller than currents in D_1 and D_2 to produce the required current density difference. To resolve this issue, Paul Brokaw introduced the well-known BGR circuit, shown in Figure 3 [4].

The Brokaw bandgap voltage reference circuit is simple and the compensation performance can be easily adjusted by post-processing, such as trimming resistors R_1 and R_2, thus overcoming the process variation problem. On the contrary, trimming resistors R_1 and R_2 in the Widlar bandgap voltage reference circuit alter the currents flowing through the BJTs and, hence, the performance of the voltage reference circuit. As a result, adjusting performance of the Widlar bandgap voltage reference circuit by trimming is not easy to implement. Nevertheless, a Brokaw bandgap voltage reference circuit that applies an opamp has the advantage of a large output driving power, which makes it suitable to be applied in circuits with heavy loads, while the Widlar bandgap voltage reference circuit requires an extra buffer stage to provide the driving power for large loads.

In this circuit, the operational amplifier makes $IC_1 = IC_2$ through resistances R, and the ΔV_{BE} that appears across R_2 is then multiplied by $2R_1$, since both emitter currents of Q_1 and Q_2 flow into this resistor. The reference output is the sum of V_{BE}, Q_1, and VR_1. The author also introduces some compensation schemes for the base currents of Q_1-Q_2 through the use of auxiliary base resistances, not shown in Figure 3.

4. Sub-1 V voltage references

The IC fabrication trend shows reduction in channel length, which leads to overall decrement in the geometry size of transistor. Reduction in the geometry size leads to increase in circuit capacity and speed. As transistor size decreases, the circuit functionality of a given area of substrate increases. Smaller device size also yields lower parasitic capacitance, which increases speed and decreases power consumption. Simultaneously, operating supply voltage must also be scaled down due to the increased electric field and reduced breakdown voltage caused by the higher doping profile required by small device. Decreased operating voltage facilitates low power consumption, which is increasingly important as circuit complexity increases. However, the voltage reference circuit becomes more difficult to design with the lower supply voltage.

The low operating voltage imposes two design challenges on voltage reference circuit designing. The first constraint is the output of the voltage reference circuit. The output voltage of the voltage reference circuit must be lower than the supply voltage. The output voltage of most of the conventional bandgap voltage reference circuits discussed in Section 3 is 1.23 V. When the supply voltage is lowered to below 1 V, how can one achieve a reference voltage with magnitude below 1 V. The voltage reference circuit capable of generating a lower output voltage is referred to as sub-1 V voltage reference circuit, which literally means that the output of the voltage reference circuit is lower than 1 V. The second design challenge is the operating supply voltage. The voltage reference circuit is required to be able to work with a low supply voltage. When the voltage reference circuit can operate at a supply voltage lower than 1 V, it is known as sub-1 V supply voltage reference circuit. Obviously, a sub-1 V supply voltage reference circuit can only generate reference voltage that is lower than the supply voltage. As a result, it is also a sub-1 V voltage reference circuit.

The conventional bandgap voltage reference circuits presented in Section 3 are suitable neither for low voltage applications nor for generating low reference voltage. The constraint on achieving a sub-1 V reference voltage is the bandgap voltage itself. In the subsequent section, we study some of the popular sub-1 V voltage reference generation circuits.

4.1. Neuteboom's voltage reference: 1997

While designing a DSP-based hearing instrument integrated circuit, Neuteboom et al. [5] were limited with supply voltage of 0.9 V. It was clear that with this limited supply voltage of 0.9 V, a conventional reference voltage of 1.23 V could not be realized. Neuteboom et al. proposed the reference circuit illustrated in Figure 4, which is based on the resistive division technique and provides an output voltage lower than 1.23 V. Their reference circuit makes use of three vertical PNP transistors with emitter ratio of $1 : N : N$. The opamp controls the emitter current and maintains a ΔV_{BE}

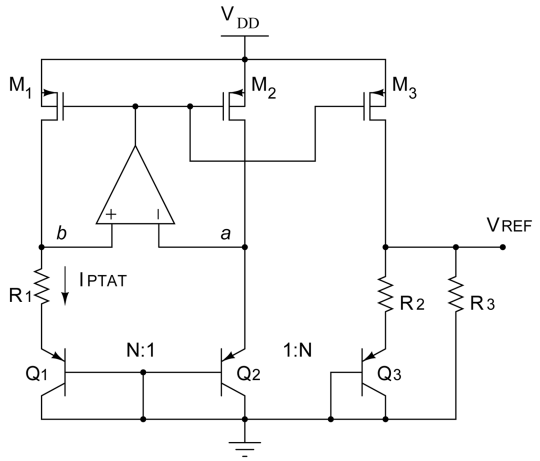

Figure 4. Neuteboom voltage reference: 1997.

across the resistor R_1 in the PTAT current generation loop. Operation under low supply voltage operation condition is achieved by connecting the resistor R_3 across the bandgap reference, and the resulting output voltage becomes a fraction of the bandgap voltage, which is given by:

$$V_{\mathrm{REF}} = \frac{R_3}{R_2 + R_3}(V_{\mathrm{BE}} + I_{\mathrm{PTAT}} R_2), \tag{8}$$

that can be scaled to any value. A down-scaling of the bandgap voltage is obtained by proper choice of resistors R_2 and R_3. The proposed circuit achieves an output voltage of 0.67 V under a minimum supply voltage of 0.9 V. Basically, the result is a simple resistive division of the bandgap reference voltage, i.e. 1.23 V.

4.2. Banba's voltage reference: 1999

Similar to Neuteboom et al. [5], Banba et al. [6] have also proposed a technique to overcome these limitations to implement sub-1 V bandgap voltage reference circuits in CMOS technology. They have used resistive sub-division technique to reduce the minimum required supply voltage. The operation of the sub-1 V opamp based bandgap voltage reference circuit with resistive division is similar to that of the conventional opamp based bandgap voltage reference circuit, where an opamp will form an inverted feedback loop to force the two input nodes of the opamp to have the same voltages. Consider the case of $R_2 = R_3$, such that $I_1 = I_2$; N is the emitter area ratio between Q_1 and Q_2. The current I_2 is mirrored to form I_3 and, therefore, the output voltage of the bandgap voltage reference circuit is given by:

$$V_{\mathrm{REF}} = \frac{R_4}{R_3}\left(V_{\mathrm{BE}_1} + \frac{R_3}{R_1} V_T \ln(N)\right). \tag{9}$$

It can be observed that the performance of this voltage reference circuit should be comparable to that

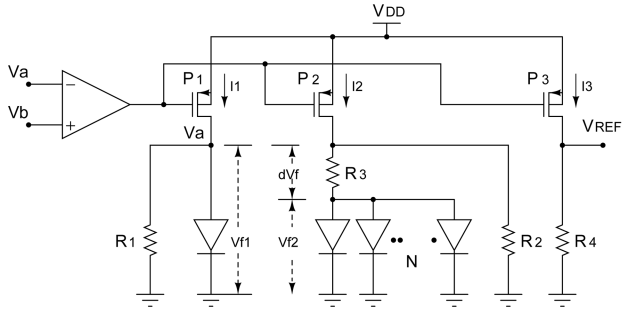

Figure 5. Banba voltage reference: 1999.

of the conventional bandgap voltage reference circuit, at least in theory. At the same time, we should also notice that V_{REF} can be scaled by the resistor ratio R_4/R_3, thus, achieving an arbitrary V_{REF}.

As observed from Figure 5, the minimum operating supply voltage of such a circuit is found to be 1.4 V, which is almost the same as that of the conventional bandgap voltage reference circuit. This is due to the limitation of the input common mode of the opamp. This limitation makes the sub-1 V bandgap voltage reference circuit with resistive division not applicable for low supply voltage applications. Moreover, susceptibility of the bandgap voltage reference circuit to noise increases because of the low output impedance of the bandgap voltage reference circuit, which is basically the output impedance of M_3. Finally, the transistor, M_3, has to be biased in saturation mode to form a proper current mirror; thus, the resistor value of R_4 will be confined to a certain region of values. The last, but not least, important fact is that the load regulation of the circuit is very low because of the low output impedance of the voltage reference circuit, which equals the output impedance of the current mirror.

Nevertheless, the resistive division technique does demonstrate that there are circuit topologies that can alleviate the common-mode input voltage constraint of the opamp in the reference circuit and, hence, inspire a lot of sub-1 V bandgap voltage reference circuit designs. Banba's architecture is the most common among industries as well as academic researchers. The following sections present modifications to this sub-1 V bandgap voltage reference circuit by resistive division, where the input voltage constraint to the opamp is lowered and, thus, overcomes the common-mode input voltage range problem to achieve sub-1 V opamp based bandgap voltage reference circuits.

4.3. Divided resistive V_{BE}-Leung and Mok's voltage reference: 2002

Although the resistor factor R_4/R_3 can help to overcome the sub-1 V output voltage problem, such that the output voltage can be smaller than 1.2 V, the bandgap voltage reference circuit in Figure 5 still cannot work with a sub-1 V supply voltage. The

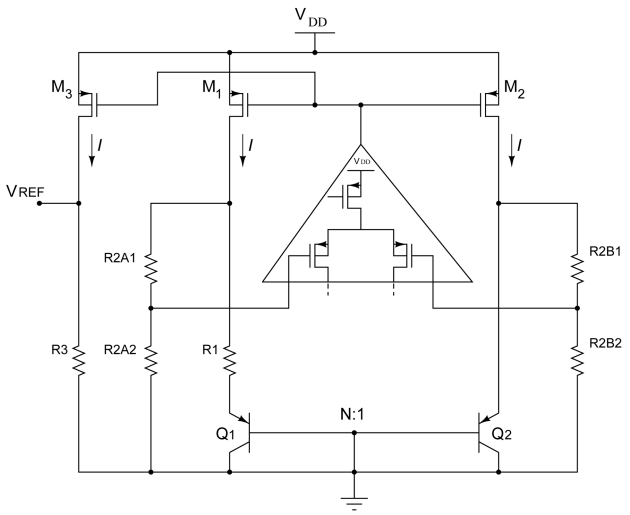

Figure 6. Leung and Mok voltage reference: 2002.

reference core circuitry proposed by Banba et al. [6] is modified by Leung and Mok [7]. The main differences are that an amplifier with a PMOS input stage is used and the inputs of the amplifier are connected to nodes N_1 and N_2 instead of N_3 and N_4. If a P-channel differential input stage opamp is used, the supply voltage is limited by the common-mode input voltage of the opamp. As a result, the input voltage to the opamp has to be low enough to make sure the P-channel input MOSFET pair are operating in the saturation region. Modified bandgap voltage reference circuit is shown in Figure 6 to lower the input voltages of the opamp by applying resistive voltage divider [7]. Assume $R_{1A} = R_{2A}$ and $R_{1B} = R_{2B}$. When the opamp has large gain, the inverted feedback loop of the amplifier will ensure $V_A = V_B$. As a result, reference voltage yields:

$$V_{\mathrm{REF}} = \frac{R_4}{R_1}\left(V_{\mathrm{BE}_1} + \frac{R_1}{R_3} V_T \ln(N)\right). \tag{10}$$

The minimum operating supply voltage of this voltage reference circuit is given by Eq. (11) with V_{BE} being replaced by the resistive sub-divided V_{BE} as:

$$V_{DD_{\min}} = \frac{R_{2B}}{R_2} V_{\mathrm{BE}_1} + |V_{th_p}| + 2|V_{DS_{\mathrm{sat}}}|. \tag{11}$$

As a result, the minimum operating supply voltage of the voltage reference circuit is being lowered by a factor of R_{2B}/R_2 acting on $V_{\mathrm{BE},1}$. We can almost conclude that the circuit has alleviated all the sub-1 V voltage reference circuit design problems.

4.4. Independent biased resistive divided V_{BE}: Ker's voltage reference: 2002

This circuit has a similar beta-multiplier circuit structure as the conventional opamp based bandgap voltage reference circuit where the current mirror transistors are directly connected to the temperature-sensitive BJTs [8]. As a result, when the temperature varies from 20°C to 100°C, the V_{BE} voltage of BJT varies from 812.55 mV to 646 mV, while the bandgap voltage reference circuit output stays almost the same. As a result, the drain to source voltages of M_1, M_2, and M_3 will not be the same and the transistors in the current mirror will suffer from the channel-length modulation effect. Hence, the above difference in source to drain voltages will cause the output current differences in the current mirror formed by M_1, M_2, and M_3. However, such mirror output current mismatch problems exist in all source-to-drain voltage conditions when V_{DD} is high. On the contrary, when V_{DD} is low and close to 1 V, M will be working close to the linear region. As a result, the I_{DS} current mismatch problem of the current mirror will be severe. Although the current mirror mismatch problem can be corrected by using a cascode current mirror, the extra layer of transistors in the cascode current mirror will increase the minimum operating supply voltage. Therefore, cascode current mirror is not applicable to correct the current mirror mismatch problem of the sub-1 V voltage reference circuit. Ker et al. [8] presented a modification to alleviate the current mirror mismatch problem by independently biasing the BJTs, instead of directly connecting the MOSFETs of the current mirror in the beta-multiplier circuit to the BJTs.

To alleviate the channel-length modulation effect that affects the performance of the current mirror, and hence the performance of the overall voltage reference circuit, Figure 7 shows a modified schematic, where the two BJTs are biased independently with two independent current sources instead of the opamp driven current sources. The independent biased resistive divided V_{BE} opamp based beta-multiplier bandgap sub-1 V voltage reference circuit was first proposed by Ker et al. [8].

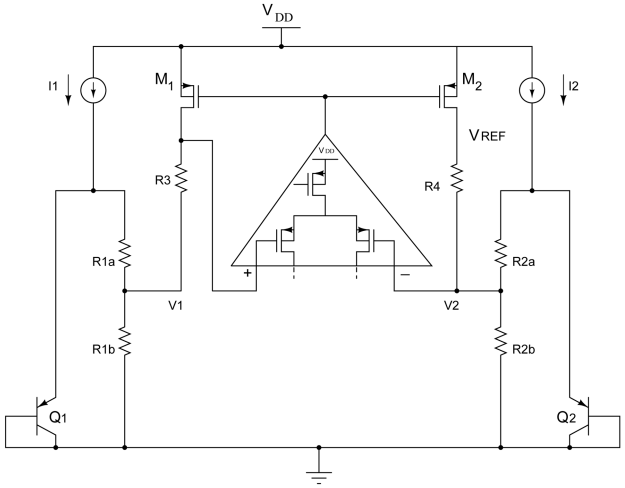

Figure 7. Ker's voltage reference: 2006.

Similar to the Banba's voltage reference circuit, resistive sub-division is applied to reduce the input voltage to the opamp. When implementing the circuit, any current source that can operate with sub-1 V V_{DD} can be applied. Note that although the current generated by the Widlar current source is PTAT, applying it to the sub-1 V opamp based beta-multiplier bandgap voltage reference circuit by resistive sub-division with independent biased $V_{\rm BE}$ will not affect the performance of the system as long as $I_1 = I_2$, and the two current sources have the same thermal property. The reference voltage is:

$$V_{\rm REF} = \left[\left(\frac{R_{1B}}{R_{1B}+R_{1A}} + R_4\right)\frac{\Delta V_{\rm BE_{1,2}}}{R_3} + V_{\rm BE_2}\right] \frac{R_{1B}}{R_{1B}+R_{1A}}. \quad (12)$$

Nevertheless, all resistive division voltage reference circuits require resistors with large resistance to scale down the reference voltage. The use of resistors with large resistance causes the resistive division voltage reference circuit to suffer from the problems of large silicon area. Use of dummy resistors for avoiding process variations results in additional area consumption. Area related problem is aggravated due to implementing resistor-matching techniques used of resistors, such as inter-digitization; which is area consuming. The production cost of this kind of bandgap voltage reference circuit is high, which prohibits their implementation in many existing applications.

4.5. Annema's voltage reference: 2012

Most of the sub-1 V bandgap voltage reference designs are based on the structure introduced by Banba et al. [6]. For low-power operation, high-ohmic resistors (occupying a large area) must be used in all these techniques, leading to an immediate trade-off between power consumption and chip-area, as we have discussed in the previous subsection. However, this trade-off prevents the local generation of reference voltages where they are required: either the power penalty or the area penalty would be too significant. Alternative topologies that do not require high-ohmic resistors typically are non-bandgap based reference circuits, relying on threshold voltages, and hence require trimming to achieve low spread.

This paper presents a sub-1 V bandgap voltage reference that circumvents the power-area trade-off of conventional sub-1 V bandgap voltage reference, aiming at local reference voltage generation wherever a reference voltage is needed in a die [9]. To break the power-area trade-off, no resistive averaging or subdivision can be used to get sub-1 V operation, while a drive to minimum area results in avoiding any topology using opamps, high ohmic resistors, or multiple diodes. The topology of the bandgap voltage reference by Annema et al. [9] is shown in Figure 8. The PMOS transistors M_{P1} and M_{P2} are biased in subthreshold region. M_{P1} is wider than M_{P2}, which is the necessary condition for PTAT voltage generation if currents are equal in both branches. Along with this condition, Annema et al. have used shorter-length M_{P1} compared to M_{P2}. By this technique, they have exploited reverse-short channel effects and yielded temperature-independent offset voltage ΔV_{th}.

$$V_{\rm REF} = V_T \ln(A)N + V_{\rm BE} - N\Delta V_{th} = V_{\rm REF_{conven}} - N\Delta V_{th}. \quad (13)$$

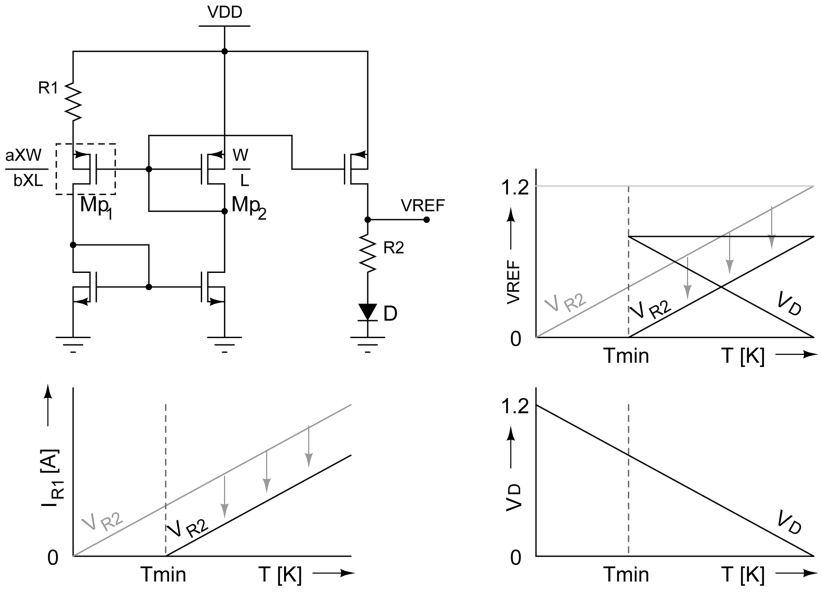

Figure 8. Principle of Annema's voltage reference: 2012.

The proposed circuit operates at supply voltage of 1.1 V over temperature range of -45 to 135°C for the reference voltage value of 944 mV. The most attractive aspect of this circuit is it consumes only 1.4 μW of power along with 0.0025 mm^2 of silicon area and produces 30 ppm/°C of accuracy with lesser spread in reference voltage across process variations. Due to these unique low area and power consumption combination along with process tolerance quality, it coins a new concept as local generation of reference voltage.

4.6. Najafizadeh's voltage reference using Filanosky's ZTC: 2004

A conventional band-gap voltage reference is generally used since its output voltage is stable against temperature and process variations. Banba and other researchers have figured out the solutions for sub-1 V bandgap reference circuit, which also operates at below 1 V. However, It was predicted in the ITRS road map that in year 2010, the mainstream power supply voltage would be around 0.6 V. Therefore, to solve this issue, many researchers have moved towards MOS based voltage reference. MOS based voltage references are not very much process-friendly, but good in terms of power and area consumption. Among the many topologies of CMOS based voltage reference circuits, ZTC based reference design is a quite uncommon but innovative concept.

As in the study of Filanosky et al. [10], if MOSFET is biased at a specific gate-source voltage and drain current (i.e. bias point), the bias point does not change irrespective of change in temperature. It is called a ZTC point. Figure 9 shows the ZTC point. ZTC point arises due to the effect of mutual compensation of mobility and threshold voltage. This technique is implemented by Najafizadeh along with Filanosky in 2004 [11]. The presented voltage reference circuit is shown in Figure 10.

Low-voltage standard PTAT current generator is

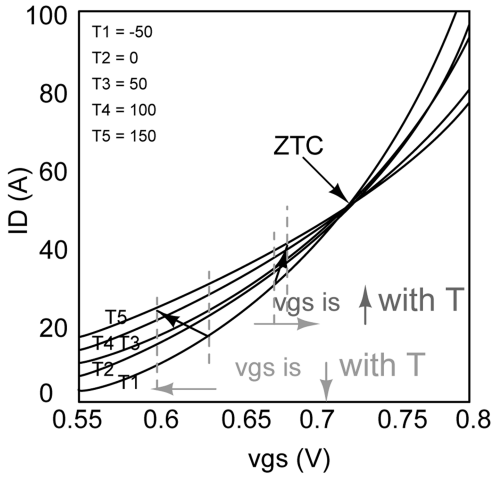

Figure 9. Filanosky's concept of ZTC: 2001.

implemented using $M_1 - M_4$ and R_B. The reference core circuit consists two diode connected transistors M_7 and M_8 operating below the ZTC point, and two resistors, R_1 and R_2. Transistors M_5 and M_6 supply PTAT PTAT currents to the transistors M_7 and M_8. The output reference voltage is given by:

$$V_{\mathrm{REF}} = \frac{V_{\mathrm{GS}_7}}{1 + R_1/R_2} + \frac{V_{\mathrm{GS}_8}}{1 + R_1/R_2}. \tag{14}$$

4.7. Leung and Mok's voltage reference: 2003

In their paper, Leung and Mok presented a voltage reference based on weighted gate-source voltage difference between an NMOS and a PMOS [12]. The proposed CMOS voltage reference is shown in Figure 11. The circuit has 3 sections:

i. A bias circuit ($M_1 - M_4$ and R_B);
ii. Start-up circuit ($M_{S1} - M_{S3}$);
iii. Reference core (M_P, M_N, R_1, and R_2).

Long channel lengths are selected for eliminating the channel modulation effect and biasing the transistors in saturation region at lower V_{GS} values.

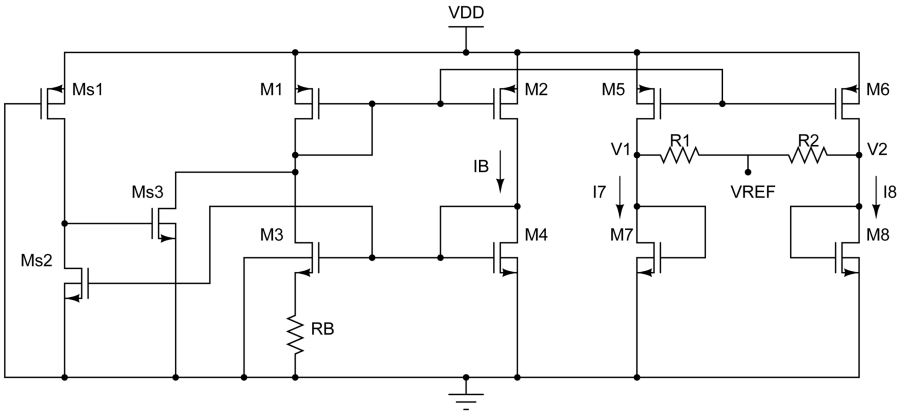

Figure 10. Najafizadeh voltage reference: 2004.

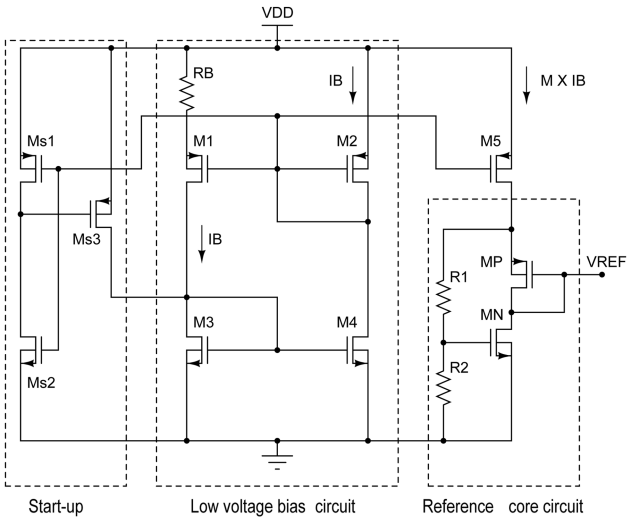

Figure 11. Leung and Mok's voltage reference: 2003.

Assume the current flowing through R_1 and R_2 is negligible; the bias current to M_P and M_N is M times I_B. The reference voltage is given by:

$$V_{\mathrm{REF}} = \left(1 + \frac{R_1}{R_2}\right) V_{\mathrm{GS}_n} - V_{\mathrm{GS}_p}. \tag{15}$$

A key factor in designing reference is keeping both M_P and M_N in deep saturation region. Therefore, the gate-source voltage is governed by the fundamental equation of MOS transistors in saturation region.

The minimum supply voltage should be considered at the minimum operable temperature as threshold voltages are at maximum. The minimum supply voltage $V_{DD_{\min}}$ is given by:

$$V_{DD_{\min}} = \left(1 + \frac{R_1}{R_2}\right) V_{\mathrm{GS}_n} + |V_{DS_{5,\mathrm{sat}}}|. \tag{16}$$

The minimum supply voltage is 1.4 V and it can be reduced if lower threshold voltage devices are used. Iannaccone and his research group have presented a series of articles from 2005 to 2014.

These papers are the extended version of the topology, which was presented by Leung and Mok in 2003.

5. Iannaccone's series of voltage references

Iannaccone has significantly contributed to reference circuits. He has proposed few important topologies, which span almost over a decade, i.e. from 2005 to 2014. We have tried to study his work in this section.

5.1. Reference voltage: CICC-2005

In CICC'2005, Iannaccone and Vita presented a voltage reference, which could be implemented in any standard CMOS technology, based on the weighted gate-source voltage difference between two NMOS transistors [13].

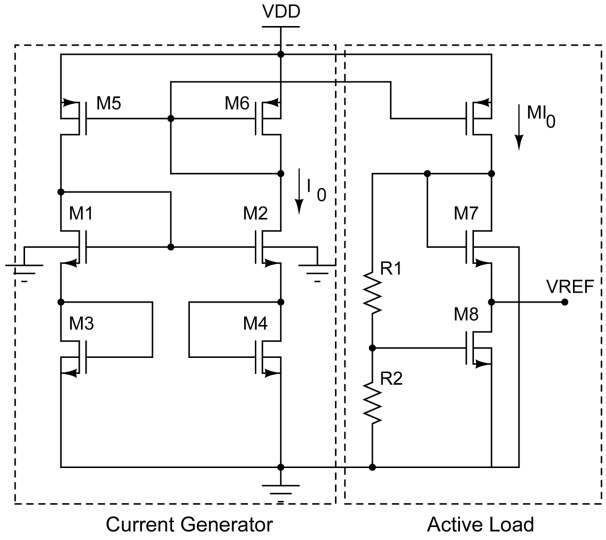

Figure 12. Vita-Iannaccone voltage reference: CICC-2005.

Such solution leads to a perfect cancellation of the effect of the temperature dependence of carrier mobility, which was a drawback in Leung and Mok's topology.

The presented voltage reference generator is shown in Figure 12. It has a supply-independent current generator, I_0; such current is then amplified and injected into an active load to generate the reference voltage. A temperature-invariant voltage reference is obtained by compensating the temperature dependence of the generated current with the temperature dependence of the NMOS threshold voltage. The final reference voltage is:

$$V_{\mathrm{REF}} = \left(1 + \frac{R_1}{R_2}\right) V_{\mathrm{GS}_8} - V_{\mathrm{GS}_7}. \tag{17}$$

The minimum supply voltage limitation is imposed by the V_{DD} independent current generator circuit. The minimum allowable supply voltage is:

$$V_{DD_{\min}} = |V_{\mathrm{GS}_6}| + V_{DS_{2,\min}} + V_{\mathrm{GS}_4}. \tag{18}$$

The supply voltage must be larger then 1.5 V for the used AMS 0.35 μm CMOS process.

Unfortunately, in this design, the temperature coefficient degrades due to non-ideal effects, i.e. channel length modulation and body effect. An experimental temperature coefficient of 25 ppm/°C is achieved.

5.2. Reference voltage: VLSI Symposium-2006

As the battery-operated systems have gained popularity after 2005, the reference circuit must consume low power and area with reasonable accuracy. The series of De Vita and Innaccone [13] consumes 2.25 μW of power at the supply voltage of 1.5 V with the consumption of 0.08 mm^2 chip area. The major reason behind this performance is power and area trade-off due to presence

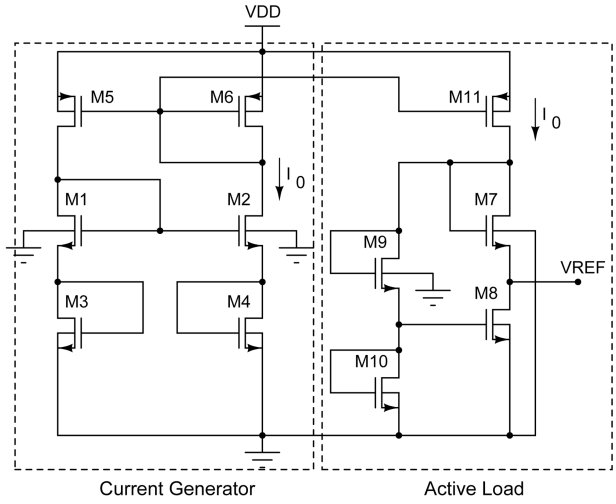

Figure 13. Vita-Iannaccone voltage reference: VLSI Symposium-2006.

of resistors. Therefore, De Vita et al. [14] have replaced the resistors with MOSFETs to break the power and area trade-off. The enhanced reference circuit is given in Figure 13.

Similar to De Vita and Iannaccone [13], the active load is used to generate the reference voltage in this study. It consists of two NMOS transistors, M_7 and M_8, biased by I_0, and a voltage divider formed by M_9 and M_{10}. All transistors in the active load operate in the saturation region. The final reference voltage is:

$$V_{\mathrm{REF}} = V_{th} + \left[\frac{1}{\sqrt{k_8}}\left(1+\sqrt{\frac{W_{10}/L_{10}}{W_9/L_9}}\right) - \frac{1}{\sqrt{k_7}}\right]\sqrt{2I_0}, \tag{19}$$

where, $k = \mu CoxW/L$ and I_0 is supply independent current.

This reference circuit consumes 0.12 μW of power at the supply voltage of 1.5 V with the consumption of 0.015 mm^2 chip area. The improvements are 5 and 18 times with regards to power and area, compared to the topology of De Vita and Iannaccone [13]. Moreover, this design provides both a complete suppression of the temperature dependence of mobility and a compensation of non-ideal effects, i.e. channel length modulation and body effect. Hence, temperature insensitivity is also enhanced twice, i.e. ≈ 12 ppm/°C. Unfortunately, the minimum supply voltage is still quite high, that is, larger than 1.5 V, and thus it is not suitable for low-voltage applications.

5.3. Reference voltage: JSSC-2007

In their paper, De Vita and Iannaccone [15] presented a CMOS voltage reference with a minimum supply voltage smaller than 1 V, really enabling low-voltage operation, which still provides a very good temperature coefficient. Let us consider the active load of the proposed reference voltage generator, shown in Figure 14.

Assuming that all transistors of the active load work in the saturation region, the output reference voltage would be given by:

$$V_{\mathrm{REF}} = V_{th_{10}} + \frac{\eta V_T}{N-1}\sqrt{\frac{W_4/L_4}{W_{10}/L_{10}}}\ln\left(\frac{W_3/L_3}{W_1/L_1}\right). \tag{20}$$

The minimum supply voltage is imposed by the current generator circuit. It is given as:

$$V_{DD_{\min}} = |V_{\mathrm{GS}_5}| + V_{DS_{1,\min}}. \tag{21}$$

The minimum supply voltage is 0.9 V in the AMS 0.35 μm CMOS process. The accuracy achieved in this architecture is 10 ppm/°C along with improvement in power consumption. Power consumption is limited to only 0.0036 μW.

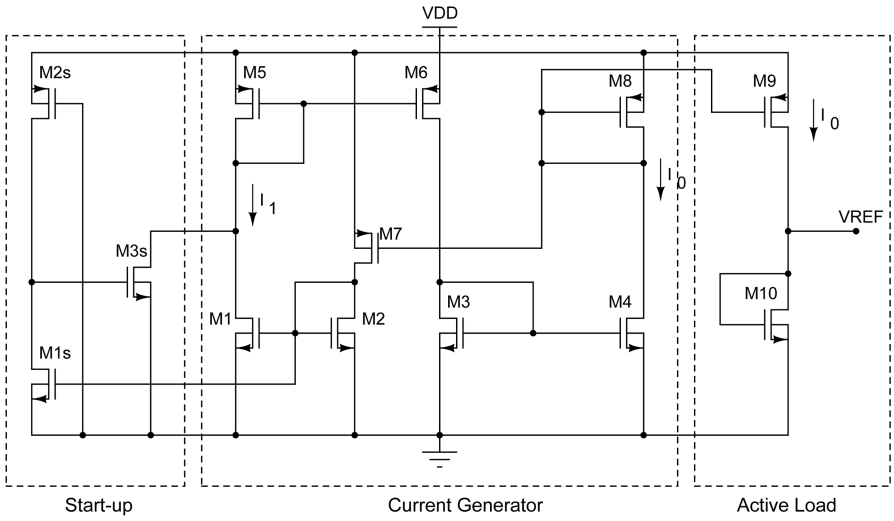

Figure 14. Vita-Iannaccone voltage reference: JSSC-2007.

5.4. *Reference voltage: JSSC'2011 and journal of circuit theory and applications, i.e. JCTA'14*

An ultra-low voltage and ultra-low power voltage reference circuit was presented by Magnelli et al. in JSSC'2011 [16]. They fabricated the circuit in the UMC 180 nm CMOS process. Importantly, the circuit works with all transistors in subthreshold region, thus allowing a drastic reduction of minimum supply voltage and power consumption. The proposed solution represents a significant advance in low-power, low-voltage reference circuit design, which chooses a new milestone for extremely low power operation. The power consumed by the circuit is only 2.6 nW, which is about one order of magnitude lower than that of the best results found in the literature at the time, and the minimum supply voltage for correct operation falls to 0.45 V. However, across the process, the circuit is a little vulnerable; thus, external trimming is required to achieve the specified accuracy and DC voltage level.

Even after achieving power dissipation down to 2.6 nW, Iannaccone and his group were working aggressively on reduction of power dissipation. Iannaccone et al. [17] presented a voltage reference consisting of only two nMOS transistors with different threshold voltages. Measurements performed on 23 samples from a single batch show a mean reference voltage of 275.4 mV. The subthreshold conduction and the low number of transistors enable us to achieve a mean power consumption of only 40 pW. The minimum supply voltage is 0.45 V, which is considered with one of the ultra-low power reference topologies. The mean TC in the temperature range of 0 to 120°C is 105.4 ppm/°C. The occupied area is 0.018 mm^2. The power supply rejection rate without any filtering capacitor is -48 dB at 20 Hz and -29.2 dB at 10 kHz.

6. Voltage reference circuits based on subthreshold MOSFETs

During 1995 to 2000, the demand for analog integrated circuits that had to operate under lower supply voltages and ultra-low power rapidly increased, especially in applications like portable equipment (e.g., watches, handheld gadgets, smart phones, etc.). Fortunately, for the analog engineer, the sub-threshold voltage characteristics of MOSFET devices mimic the characteristics of Bipolar devices. Therefore, subthreshold-based MOSFET was an potential replacement for BJTs. Therefore, the nanopower regime opened up a wide perspective for reference circuits using a subthreshold transistor. Even though these transistors are quite dependent on process, they have become famous due to their ultra-low power and low area consumption capabilities. We will see some reference circuits based on subthreshold biasing principle.

6.1. *Ytterdal's voltage reference: 2003*

As discussed in Section 4.6, Najafizadeh and Filanovsky [11] have designed MOSFET-based reference circuit to solve the problem of supply voltage reduction due to shrinking technology. Ytterdal [18] also solved a similar supply-related problem using MOS devices; however, he used subthreshold biased MOS transistors for replacing BJTs, where Najafizadeh used a concept of ZTC.

Ytterdal basically used the technique presented by Banba. However, he replaced bipolar devices with subthreshold-based MOSFETs. As a consequence, Ytterdal was able to reduce the supply voltage well below 1 V. He also used low-threshold voltage NMOS transistors to reduce $V_{DD_{min}}$. Moreover, he also reduced the threshold voltages of PMOS by bulk-biasing. The proposed topology is given in Figure 15.

Due to these techniques, the reference voltage circuits operate at 0.6 V for 0.13 μm digital CMOS

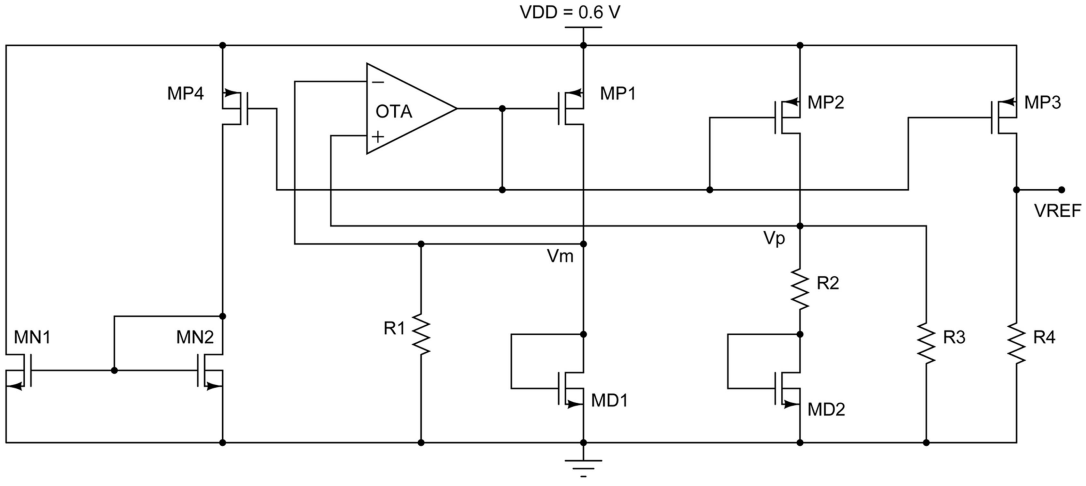

Figure 15. Ytterdal voltage reference: 2003.

technology. The reported temperature coefficient is 93 ppm/°C.

6.2. Reference voltages by Giustolisi et al., 2003, and Huang et al., 2006

Similar to Ytterdal, Giustolisi et al. [19] have also used identical principle to develop a reference circuit. They exploit the fact that the gate-source voltage decreases linearly with temperature, if it is biased with a constant drain current.

As shown in a Figure 16, the current I_{R_1} is the minimum supply voltage imposed by the current generator circuit. It is given as:

$$I_{R_1} = \frac{V_{\mathrm{GS}_1}}{R_1}. \tag{22}$$

This current is then provided for the second sub-circuits M_5 and M_6 and the output voltage is given by:

$$V_{\mathrm{REF}} = K_1 V_{\mathrm{GS}} + K_1 V_T, \tag{23}$$

where K_1 and K_2 are the combinations of transistor aspect ratios and resistor ratios. After selection of proper values for resisters and MOSFETs, the proposed architecture achieves an output voltage of 0.2953 ± 0.0108 V and a temperature coefficient of 119 ± 35.7 ppm/°C for the temperature range of -25 to 125 °C. Operable minimum supply voltage is 1.2 V with line regulation of 2 mV/V. The current consumption is 3.6 μA.

The circuit presented by Giustolisi et al. is complex and consumes larger area and power compared to the reference circuit proposed by Huang et al. [20]. The circuit by Huang et al. is given in Figure 17. The comparison is done on the basis of identical working principle, i.e. gate-source voltage compensated by thermal voltage (core transistors are operating in subthreshold region). The presented circuit by Huang

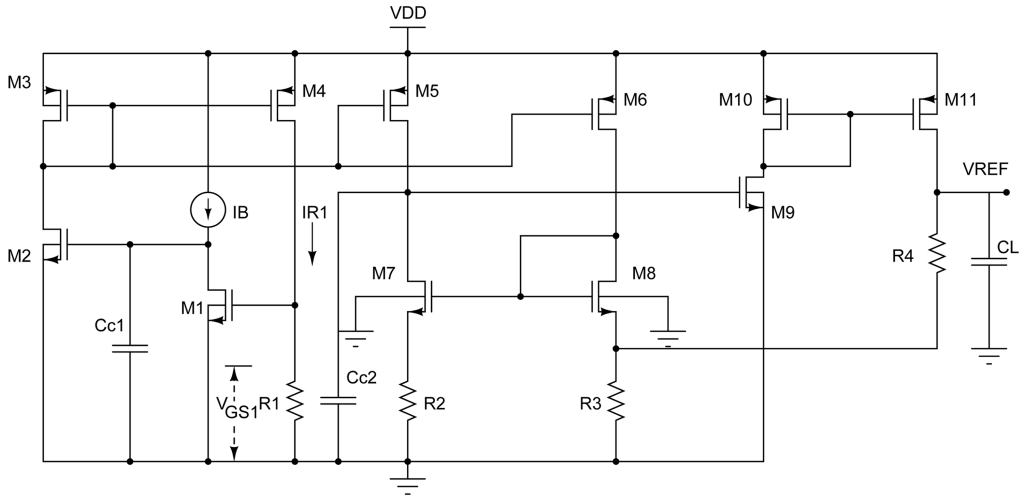

Figure 16. Giustolisi et al.: voltage reference, 2003.

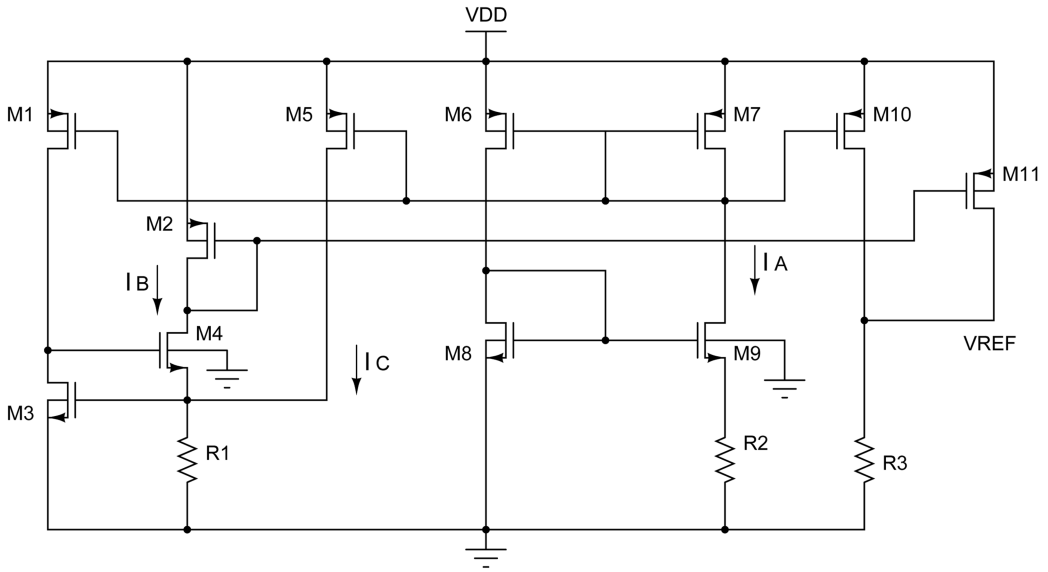

Figure 17. Huang et al.: voltage reference 2006.

et al. is a less complicated low-voltage, low-power CMOS reference circuit using subthreshold biasing concept.

They have also compensated the channel-length modulation effect to improve the performance. The mean reference voltage is ≈ 222 mV with line regulation of 2 mV/V (for V_{DD} varies from 0.9 to 2.5 V). Peak-to-peak variation of 6 mV is reported for temperature from -20°C to 120°C. The chip area is less than 0.0238 mm^2 with minimum power consumption of 3.3 μW.

7. High-order curvature correction

Precision bandgap references are significantly necessary for many applications ranging from solely analog, to mixed-mode and purely digital circuits, such as data converters, digital data RAMS, power converters, and memory controlling circuits. They are known for their high accuracy and temperature-independent behavior. The reference voltage is required to be stable over the supply voltage and temperature variations. It should also be implemented without any modification of the standard fabrication process.

A conventional bandgap reference circuit is first-order temperature compensated. Basically, it is an appropriately scaled sum of negative TC voltage $V_{\rm BE}$ and positive TC voltage V_T, which is the thermal voltage. With regard to nonlinearity of the voltage $V_{\rm BE}$, TC of first-order temperature compensated references is always limited between 20 and 100 ppm/°C. Therefore, to overcome this limitation, many high-order temperature compensation approaches have been presented. Compensation of the high-order temperature dependent terms of the reference voltage (nonlinear terms) is therefore referred to as curvature correction or curvature compensation. The primary curvature correction techniques used in practice are, for example, the quadratic temperature compensation proposed by Song and Gray [21], the exponential temperature compensation developed by Lee et al. [22], the piecewise linear curvature correction presented by Rincon-Mora and Allen [23], and the temperature dependent resistor ratio with a high resistive poly resistor and a diffusion resistor proposed by Leung et al. [24]. The accuracy of bandgap references has been enhanced with these techniques; however, they also increase the requirements of precise matching of the current mirror. Some of the popular curvature correction techniques will be discussed in the next subsections.

7.1. Song's voltage reference: 1983

The nonlinear relationship between $V_{\rm BE}(T)$ and temperature is expressed as:

$$V_{\rm BE}(T) = V_{\rm BG} - [V_{\rm BG} - V_{\rm BE}(T_r)]\frac{T}{T_r} - (\eta - m)V_T \ln\left(\frac{T}{T_r}\right), \quad (24)$$

where $V_{\rm BG}$ is the bandgap voltage of Si as a function of temperature, T_r is the reference temperature, η is a temperature constant dependent on technology, and m is the order of the temperature dependence of the collector current. The third term of Eq. (24) is proportional to PTAT^2 voltage.

Song et al. proposed to add a PTAT^2 term to the linear PTAT term to compensate for the junction curvature. The concept is clearly demonstrated by Song et al. The optimum values of the PTAT^2 correction voltage, the first-order corrected $V_{\rm REF}$, and second-order corrected $V_{\rm REF}$ at 25°C were measured and recorded 61 mV, 1.256 V and 1.192 V, respectively.

7.2. BJT current subtraction - Gunawan's voltage reference: 1993

As discussed by Gunawan et al. [25], a current source with second-order temperature dependency can be conveniently obtained by the BJT in the same way as that in the output stage of the opamp based beta-multiplier bandgap voltage reference circuit. (The second-order temperature dependent nature of the BJT $V_{\rm BE}$ voltage is one of the major reasons for the need to implement second-order temperature compensation to obtain a low TC reference voltage over a wide temperature range.) The presented circuit is shown in Figure 18. When this BJT current source is appropriately connected to the voltage reference circuit, it forms a current sink and, hence, functions as second-order current subtraction circuit to achieve second-order curvature correction. Consider the schematic of Banba's opamp based bandgap voltage reference circuit with the BJT current subtraction. This topology is an extension of Banba's concept. The resistors in the

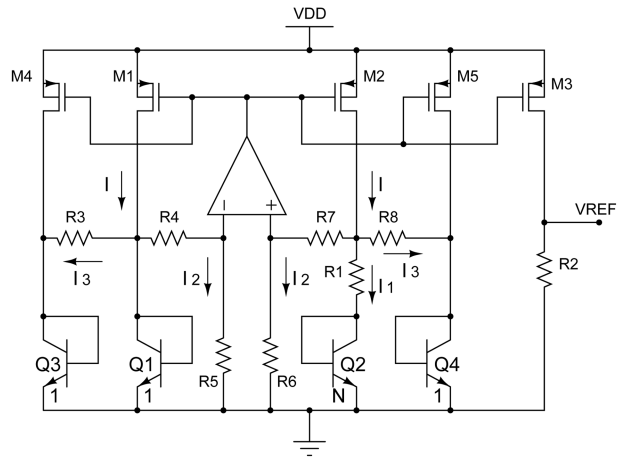

Figure 18. Gunwan's voltage reference topology: 1993.

circuit satisfy $R_3 = R_8$, $R_4 = R_7$, and $R_5 = R_6$. The emitter areas of Q_1, Q_2, Q_3, and Q_4 are in the ratio of $1 : N : 1 : 1$. Note that the negative feedback configured opamp will bias the input voltages to be the same; therefore, we write:

$$V_A = V_B. \tag{25}$$

Therefore, with $R_5 = R_6$, the currents that flow through R_5 and R_6 will be the same and equal to I_2. Assume the opamp is ideal; no current will be flowing in/out of $V+$ and V. As a result, the currents that flow through R_4 and R_7 will be the same; hence:

$$I_1 = \frac{V_T \ln(N)}{R_1}, \tag{26}$$

and:

$$I_2 = \frac{V_{\mathrm{BE}_1}}{R_4 + R_5}, \tag{27}$$

and:

$$I_3 = \frac{V_T \ln(T/T_{\mathrm{nom}})}{R_3}. \tag{28}$$

The KCL at node C implies $I = I_1 + I_2 + I_3$, and the current mirror pair formed by M_2 and M_3 copies the current to the output branch. By selecting $S_2 = S_3$, we shall obtain:

$$V_{\mathrm{REF}} = K_1(V_{\mathrm{REF}_{\mathrm{conven}}} + K_3 \ln(T/T_{\mathrm{nom}})V_T), \tag{29}$$

where:

$$K_1 = R_2/(R_4 + R_5), \quad K_2 = (R_4 + R_5)/R_1,$$

and:

$$K_3 = (R_4 + R_5)/R_3.$$

Furthermore, it is clear that when $T = T_{\mathrm{nom}}$, the voltage reference obtained by Eq. (29) will have the same form as that of the conventional bandgap voltage reference circuit at T_{nom} (as studied in the previous sections).

At other temperatures, the high-order temperature dependent term $K_3 \ln(T/T_{\mathrm{nom}})VT$ will compensate the second-order temperature dependent term of $V_{\mathrm{BE},1}$. This is achieved by appropriate selection of the resistor R_3 to drive Q_3.

7.3. Piecewise curvature correction - by Rincon-Mora and Phillip E. Allen: 1998

Around the year 1998 and onwards, the demand for low voltage references appeared, especially in mobile battery-operated products such as cellular phones, pagers, camera recorders, and laptops. Consequently, low-voltage and low-quiescent current flows are intrinsic and required characteristics for increased battery efficiency. Along with that, financial considerations also require these circuits to be realized in relatively simple processes, such as standard CMOS. Owing to this requirements, Rincon-Mora and Phillip E. Allen have designed and fabricated a low-voltage, micropower, curvature-corrected bandgap circuit in a relatively inexpensive process, MOSIS CMOS 2 μm N-well technology with an added P-base layer [23]. The P-base layer is used to create NPN transistors. However, a vanilla CMOS version of the circuit can also be designed by using lateral PNP transistors. The circuit implements a novel current-mode piecewise-linear curvature-correction technique.

Piecewise-linear curvature-correction is a novel concept implemented by Rincon-Mora and Phillip E. Allen. Afterwards, many researchers have used enhanced techniques based on this concept. Operation principle is given in Figure 19(a) and (b).

The curvature correction is based on the addition of a nonlinear component to the output of a first-order bandgap reference. This is used to offset the nonlinear behavior of V_{BE} with respect to temperature. The nonlinear component, in this case, is realized by I_{NL} in the current-mode topology of the circuit described in Figure 19(a). It is basically a current-mode piecewise-linear form of compensation. The essence of the circuit centers on current subtraction and the characteristics of non-ideal transistors. Figure 19(b) graphically illustrates the operation of the circuit throughout the temperature range. The I_{NL} behavior is described by:

$$I_{\mathrm{NL}} = 0 \qquad \text{if,} \quad I_{V_{\mathrm{BE}}} > I_{\mathrm{PTAT}}, \tag{30}$$

or:

$$I_{\mathrm{NL}} = K_1 I_{\mathrm{PTAT}} - K_2 V_{\mathrm{BE}} \qquad \text{if,} \quad I_{V_{\mathrm{BE}}} < I_{\mathrm{PTAT}}, \tag{31}$$

where K_1 and K_2 are constants and defined by current mirroring ratios.

$$\begin{aligned} V_{\mathrm{REF}} &= K_1(K_2 + V_{\mathrm{BE}_1} + K_3 \ln(T/T_{\mathrm{nom}})V_T) \\ &= K_1(V_{\mathrm{REF}_{\mathrm{conven}}} + K_3 \ln(T/T_{\mathrm{nom}})V_T), \end{aligned} \tag{32}$$

where K_3 is multiplication constant.

Finally, the reference voltage (V_{REF}) is temperature compensated to exhibit a behavior that is graphically described by Figure 19(c) and (d). The lower temperature range is essentially a first-order bandgap, since the nonlinear component (I_{NL}) is zero. At higher temperatures, the resulting behavior is similar to that of the lower temperatures, but the operation is not. The nonlinear behavior of I_{NL} attempts to cancel non-linearity of $I_{V_{\mathrm{BE}}}$. Therefore, addition of $AI_{V_{\mathrm{BE}}}$, BI_{PTAT}, and CI_{NL} gives the curvature correction operation as shown in Figure 19(d). The measured results show that the achieved accuracy is less than 20 ppm/°C and minimum operable supply voltage of 1.1 V.

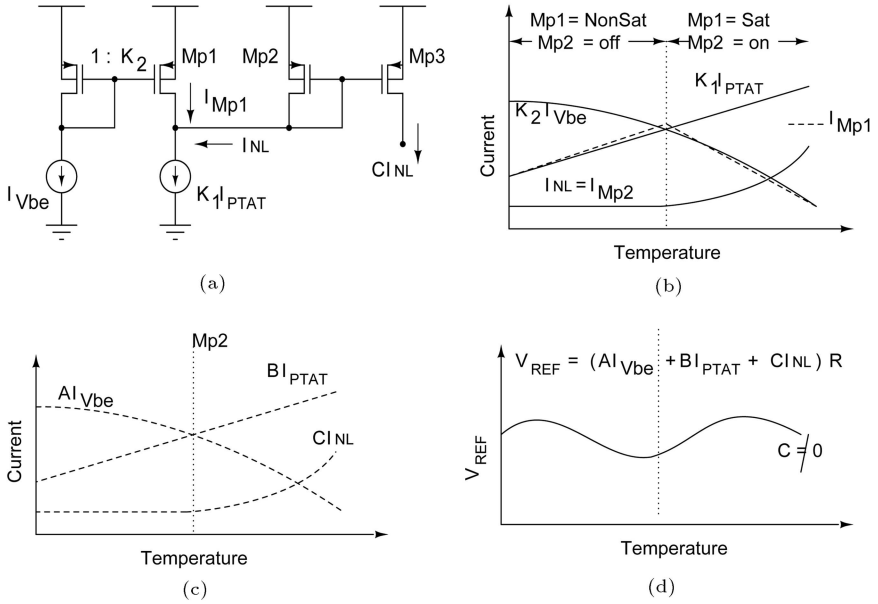

Figure 19. (a) and (b) Generation of the nonlinear current component. (c) and (d) Temperature dependence of the curvature-corrected bandgap reference.

7.4. Curvature correction - by Malcovati's: 2001

The circuit proposed by Malcovati et al. [26] is shown in Figure 20. It is one of the classic voltage references for curvature correction. Different values of $V_{\rm BE}$ can be obtained by different temperature-dependent collector currents. In this circuit, Q_2 is biased by a PTAT current:

$$V_{\rm BE_2} = V_{\rm BG}(T_r) + \frac{T}{T_r}[V_{\rm BE}(T_r) - V_{\rm BG}(T_r)] + (\eta - 1)\frac{kT}{q}\ln\left(\frac{T_r}{T}\right), \quad (33)$$

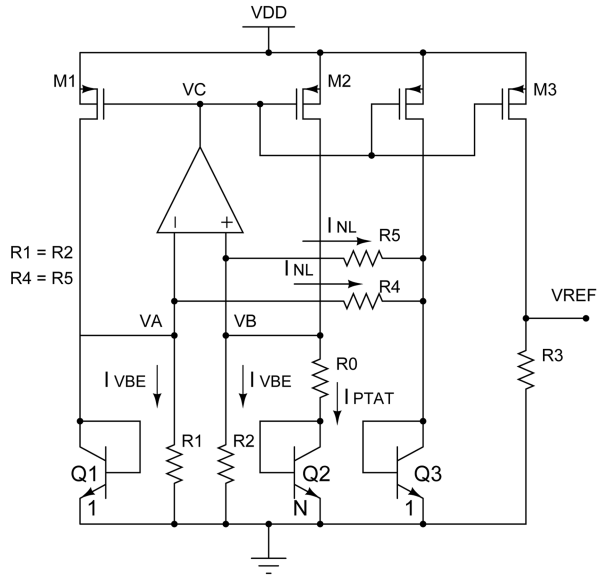

Figure 20. Schematic of the proposed bandgap circuit with curvature compensation by Malcovati.

while Q_3 is biased by a temperature-independent current and $V_{\rm BG}$ is bandgap voltage of silicon:

$$V_{\rm BE_3} = V_{\rm BG}(T_r) + \frac{T}{T_r}[V_{\rm BE}(T_r) - V_{\rm BG}(T_r)] + \eta\frac{kT}{q}\ln\left(\frac{T_r}{T}\right). \quad (34)$$

A non-linear current $I_{\rm NL}$, which is the current flowing through R_4, is generated and given by:

$$I_{\rm NL} = \frac{V_{\rm BE_2} - V_{\rm BE_3}}{R_4} = \frac{V_T}{R_4}\ln\left(\frac{T}{T_r}\right). \quad (35)$$

Therefore, $V_{\rm REF}$ is given by:

$$V_{\rm REF} = (I_1 + I_2 + I_3)R_3 = \frac{R_3}{R_1}V_T\ln(N) + \frac{R_3}{R_2}V_{\rm BE_2} - \frac{R_3}{R_4}V_T\ln\left(\frac{T_r}{T}\right). \quad (36)$$

When the easy-control resistor ratio $R_2/R_4 = \eta - 1$, the non-linear voltage in $V_{BE,2}$ is canceled. A theoretical zero TC $V_{\rm REF}$ can be obtained. However, it cannot always be achieved due to the non-ideal PTAT and temperature-independent currents from the temperature dependence of resistors. In addition, errors due to mismatch of current mirrors worsen the accuracy.

The proposed bandgap reference circuit by Malcovati et al. was fabricated in a 0.8 μm Bi-CMOS technology. It achieved a temperature coefficient of 7.5 ppm/°C. The line regulation was 212 ppm/V, with a power consumption of only 92 μW at room temperature.

7.5. Brief discussion of curvature correction techniques after 2001

In 2003, Leung et al. [24] presented a low-voltage CMOS high-order curvature compensated bandgap reference based on a temperature-dependent resistor ratio. The proposed bandgap reference utilizes the negative temperature-coefficient high-resistive poly resistor in the CMOS process and the positive temperature- coefficient diffusion resistor to implement a temperature-dependent resistor ratio. This resistor ratio can effectively reduce the temperature drift of the bandgap reference voltage. The achieved temperature coefficient is 5.3 ppm/°C at a 2 V supply voltage, which consumes 23 μA current. In 2005, Mitrea et al. [27] proposed a curvature-correction technique based on compensation of the base-emitter voltage nonlinearity, using it to correct the drain current of a MOS transistor working in weak inversion. Cancellation of the first- and second-order terms of the polynomial expansion of the base-emitter voltage allows the reduction of the temperature coefficient of the bandgap reference. The measured temperature coefficient is about 10.5 ppm/°C over a temperature range of 10°C to 90°C, while power consumption is subtly at higher side, i.e. $\approx$ 1.4 mW. In 2006, Ker and Chen [28] proposed a curvature-compensation technique, which had two output reference currents. These currents were generated by two current-mode bandgap references (the similar architecture to that of Leung and Mok in 2002 [7]). Both currents acted with concave and convex curves. Addition of these curves gave curvature compensated performance. The experimental results showed that the minimum operable supply voltage was 0.9 V and the output reference voltage was 536.7 mV with a temperature coefficient of 19.55 ppm/°C from 0°C to 100°C. In 2010, Guan et al. [29] presented an advanced version of Malcovati's design. They used current-mode curvature compensation technique. The circuit delivered an output voltage of 1.09 V and achieved the lowest reported temperature coefficient of 3.1 ppm/°C over a temperature range of -20°C to 100°C. However, power dissipation was 110 μW. Nowadays, many researchers use derived versions of the abovementioned curvature correction technique with minor modifications.

8. Conclusion

Bandgap/non-bandgap based voltage reference is an important building block in analog circuit design. Evolution of voltage reference circuits is explicitly provided in chronological order to build-up a better understanding of reference circuit. We have drafted an in-depth survey of classic and recent reference topologies. The design trend and current design methodologies of bandgap voltage reference have been discussed. This survey will give insight to designers while building voltage references.

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