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Research Note

MOSCAP linearization and its application in low-power electrocardiogram amplifier

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CMRR;
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Abstract. Considerable area occupied by capacitors is one of the main issues in the design of many ICs, especially in biomedical applications. MIM capacitor can be replaced by the MOSCAP to reduce the chip area and cost. Although the MOSCAP shows a non-linear behavior, linearization can be performed to some extent using serial and parallel compensation. In this paper, a new approach is presented, by which the impact of MOSCAP non-linearity on the THD of the circuit is reduced. The proposed technique is used in an electrocardiogram amplifier. The appropriate structure for each MOSCAP of the amplifier is selected by analyzing the non-linear effect of the MOSCAPs on the amplifier's output linearity. The non-linear effect of MOSCAP is reduced by choosing the appropriate slopes in the MOSCAP capacitance-voltage curve. As a result, the occupied area of the amplifier is reduced to less than 10 percent of the area of the amplifier with MIM capacitors, while the THD is not changed considerably. The output THD is 0.65% at 60 Hz and the total power consumption is 72 nW.

1. Introduction

Capacitors are one of the bulky and area consuming elements in integrated circuits. Metal-oxide-metal capacitors have high quality factor and linearity range and low sensitivity to temperature. The density of standard Metal-oxide-metal capacitors is very low because of the relatively thick oxide layer. Poly-Isolation-Poly (PIP) and Metal-Isolation-Metal (MIM) capacitors have a thinner oxide layer and, hence, the density of these capacitors is higher. These capacitors have high quality factor and good linearity, but the fabrication process needs additional masks and more fabrication steps. Applying additional layers and steps increases the cost and, therefore, MIM capacitors are not utilized in the standard digital CMOS fabrication process.

The bulk-gate capacitor of the MOSFET transistor, called MOS Capacitor (MOSCAP), is used in standard digital technology to serve as a capacitor with a high density. MOSCAP has low linearity and high capacitance per unit area in comparison with MIM capacitor. The main problem of using MOSCAP is high dependency of the capacitance value on the corresponding voltage. MOSCAP capacitance changes in different operating regions due to the change in Gate-Bulk voltage (V_{gb}). Figure 1 shows the capacitance-voltage curve in accumulation, depletion, and inversion regions. The variations of capacitance are not significant in accumulation and inversion regions, but they are very noticeable in the depletion region. The needed voltage for the MOSCAP to work in the accumulation and inversion regions is high and in many low-voltage applications, this voltage is not applicable. Therefore, using depletion region is inevitable [1].

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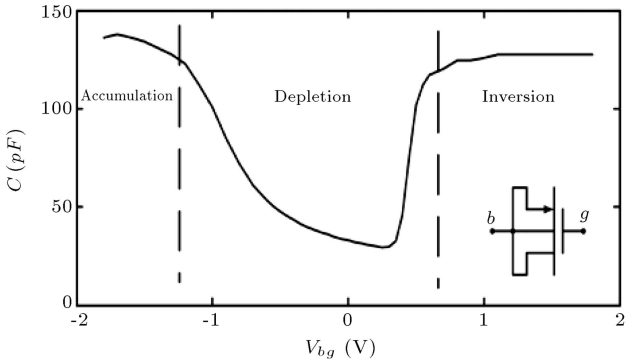

Figure 1. Capacitance-voltage curve of the P-type MOSFET ($W = 500$ μm, $L = 30$ μm).

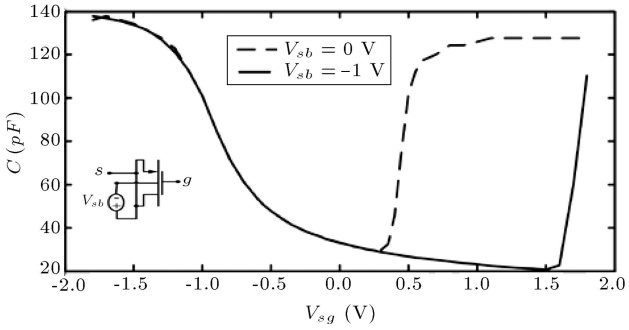

Figure 3. Schematic and capacitance-voltage curve of P-type MOSCAP with substrate bias ($W = 500$ μm, $L = 30$ μm).

2. MOSCAP compensation methods

Analog compensation methods are used for reducing nonlinear behavior of the MOSCAP in depletion region. Parallel and serial MOSCAP linearization methods in depletion region are illustrated in Figure 2. Parallel Compensated Depletion Mode (PCDM) saves more area, but it is less linear than Serial Compensated Depletion Mode (SCDM). Bias point (c) (Figure 2) in SCDM is because of extending the linear range and making the capacitance-voltage curve symmetric to zero voltage [1].

Negative bias voltage of the substrate (V_{sb}) is applied between source/drain node and bulk node to extend the usable voltage range of the MOSCAP in depletion mode (Figure 3). Depletion region is extended due to shifting of the threshold voltage as the threshold voltage (V_T) is related to bulk voltage through Eq. (1) [1]:

$$|V_T - V_{T0}| = \gamma\sqrt{|2\Psi_f + V_{\rm SB}|} - \gamma\sqrt{|2\Psi_F|}. \quad (1)$$

This technique can be used in both parallel and serial compensated depletion modes. Figure 4 shows the schematic and capacitance-voltage curve of PCDM for different bias voltages of the substrate. Note that the drain/source-bulk diodes should be kept reverse biased.

Negative bias voltage of the substrate can be applied in serial compensated, too. The linear range of SCDM can be increased by increasing the absolute value of the negative voltage of the substrate.

In 0.18 μm technology, capacitance density of the MOSCAP in the depletion mode is four times more than MIM capacitor and this ratio increases to sixteen times when the MOSCAP is in accumulation or

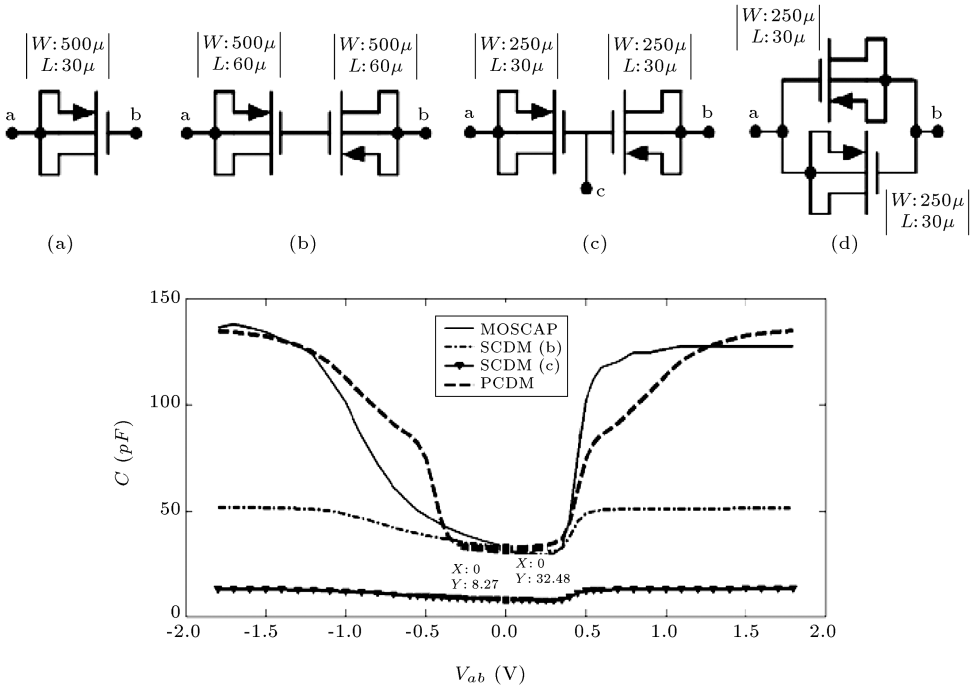

Figure 2. Schematic and capacitance-voltage curve for MOSCAP, PCDM, and SCDM methods.

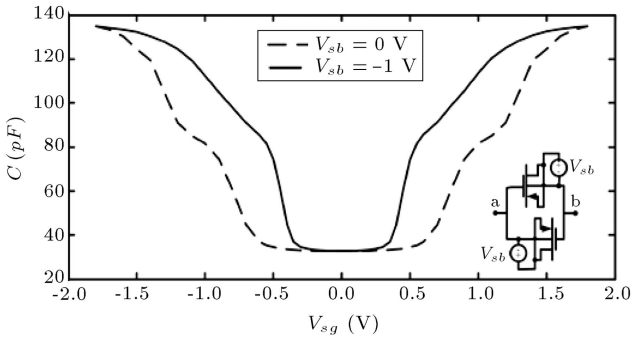

Figure 4. Schematic and capacitance-voltage curve of PCDM for different V_{sb} voltages ($W = 250$ μm, $L = 30$ μm).

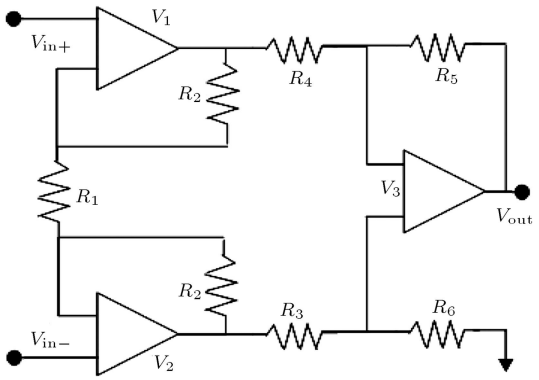

Figure 5. Schematic of the instrumentation amplifier circuit.

inversion regions. PCDM method presents capacitance density of unit area almost four times more than MIM capacitor, and SCDM method presents capacitance density of unit area almost equal to MIM. In addition, SCDM method is more linear than PCDM.

MOSCAP has been used in integrated circuits. Capacitors are implanted using PCDM techniques in low-voltage analog to digital converter, and nonlinear effect of the capacitor on the output has been evaluated [2]. PCDM and SCDM methods, using substrate bias, have been used in $\Delta\Sigma$ modulator for MOSCAP linearization and area reduction in low voltage applications [1]. In this paper, MOSCAP is used in electrocardiogram amplifier.

3. Electrocardiogram amplifier

Nowadays, portable medical equipment is widely used and issues like power consumption and area reduction are among the critical design issues. One of the common medical equipments is electrocardiogram system, which receives and displays the heart signal. The electrocardiogram signal is less than 5 mV and the frequency ranges from less than 0.5 Hz to above 200 Hz. The low amplitude signal should be amplified, while signals such as noise, offset and common-mode signals should be omitted [3].

Different structures with different advantages and disadvantages have been proposed for electrocardiogram amplifier. Chopper amplifiers decrease flicker noise, but their power consumption is high since the required bandwidth of the amplifier should be more than the chopping frequency [3,4].

One of the common structures of biomedical amplifier is the instrumentation amplifier. Gain is provided by a resistive divider in this structure (Figure 5). Noise and power consumption are high and Common-Mode Rejection Ratio (CMRR) is low due to resistors' mismatches, but the input impedance is large in this structure and common-mode voltage is obtained without any peripheral circuit [5,6]. In an ECG amplifier, a right leg drive circuit is used to eliminate common-mode signals. The noise and area can be reduced slightly if the resistors are implemented by transistors, but the power dissipation remains high [7]. It is possible to reduce noise and power dissipation in the instrumentation if resistors are replaced by the capacitors [5], but the occupied area of the MIM capacitors increases since the low cut-off frequency needs to be less than 1 Hz. MOSCAP can be used for the chip area reduction.

3.1. Instrumentation amplifier design

The first stage of the instrumentation amplifier is performed to obtain high input impedance. The common-mode voltage is also obtained at the output of this stage. This stage is not intended to provide a large gain. The second stage is performed for high and variable gain. As mentioned above, it is possible to use capacitors instead of resistors to reduce noise and power consumption. Such an amplifier is shown in Figure 6. In this amplifier, the offset voltage cannot affect the output because of the capacitor C_{5-6}, which exists in the input to output path and common-mode voltage is gained at the central node (V_{cm}) [5].

In the amplifier of Figure 6, the following points are worth explaining:

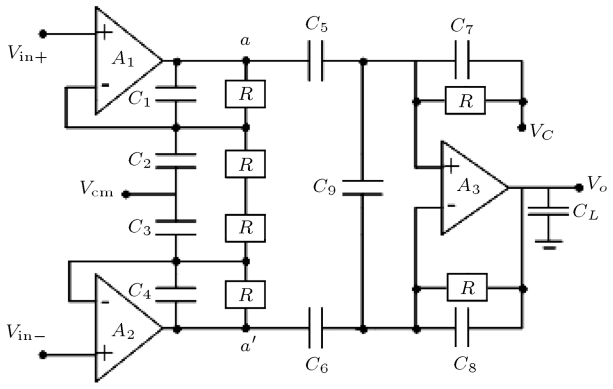

Figure 6. Schematic of the instrumentation amplifier with capacitors replacing resistors.

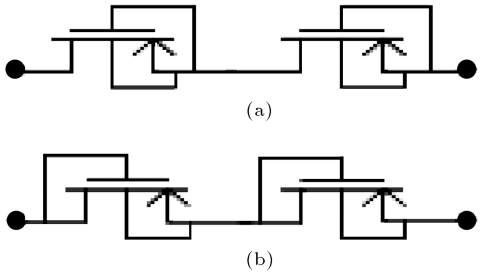

Figure 7. Structures of the pseudo-resistors.

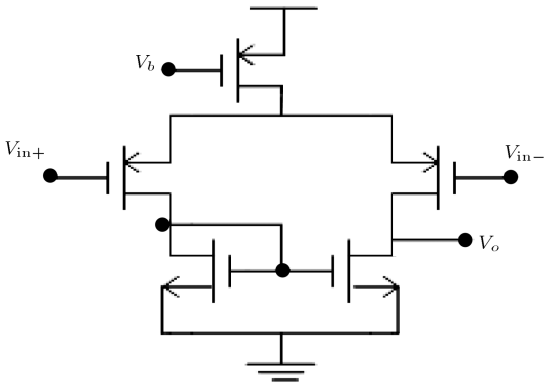

Figure 8. OTA structure.

- R blocks in Figure 6 are pseudo-resistors. Different structures are proposed for the pseudo-resistors. The diode connected structure, illustrated in Figure 7(b), is more linear than gate-source short-circuited structure. Resistance value of the order of 10^{12} Ω can be achieved if the gate-source voltage is near zero in the diode structure [8];
- Instrumentation amplifier is built by three Operational Transconductance Amplifiers (OTA). OTA structure is illustrated in Figure 8. PMOS transistors are selected for the input since the flicker noise of the PMOS transistor is one to two orders of magnitude less than NMOS transistor. Input transistors with large dimensions are selected and biased in the sub-threshold region to have low noise and power consumption [5]. The main portion of the power consumption is dedicated to the first stage as it highly affects the circuit noise;
- The driven-right-leg circuit omits the common-mode signal using common-mode feedback and, hence, prevents the amplifier from being saturated due to the large amplitude of the common-mode signal. The driven-right-leg circuit is made of a buffer and an OTA as it can be seen in Figure 9. A class AB buffer is used in driven-right-leg circuit to reduce power consumption, so the CMRR does not reduce in low power consumption. The class AB buffer structure is shown in Figure 10; this structure is chosen because of the very low distortion [9]. High CMRR can be achieved with much low power consumption in comparison to the case of using a class A buffer.

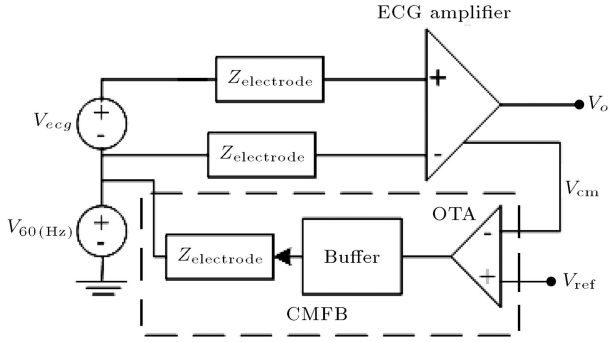

Figure 9. Driven-right-leg circuit.

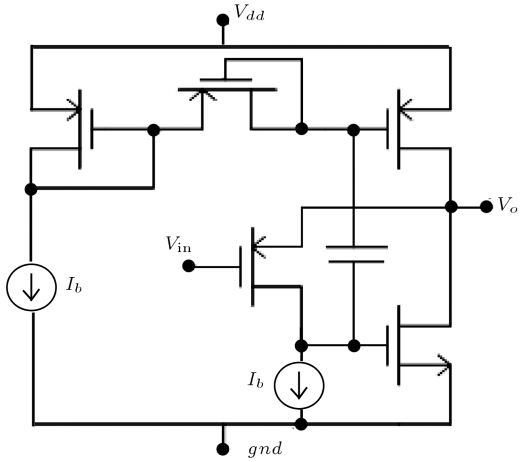

Figure 10. Class AB buffer structure.

4. Using MOSCAP in the instrumentation amplifier

The low cut off-frequency of the ECG amplifier needs to be less than 0.5 Hz as it is both an amplifier and a filter. Therefore, capacitance values increase, which lead to large circuit area. MOSCAP can be used instead of MIM capacitor in order to reduce the area of capacitor. However, the MOSCAP has a very nonlinear behavior and it affects the amplifier THD. Here, we analyze the effect of nonlinearity of capacitors on the amplifier output. Based on the provided analysis, the compensated structure of each MOSCAP is selected next.

4.1. Total harmonic distortion analysis

We need to calculate the effect of each nonlinear MOSCAP of the instrumentation amplifier (block C of Figure 6) on the output nonlinearity.

Simplified single ended schematic of the instrumentation amplifier is illustrated in Figure 11. OTAs are supposed to be completely linear and the effect of the capacitor of each stage on the output nonlinearity is evaluated.

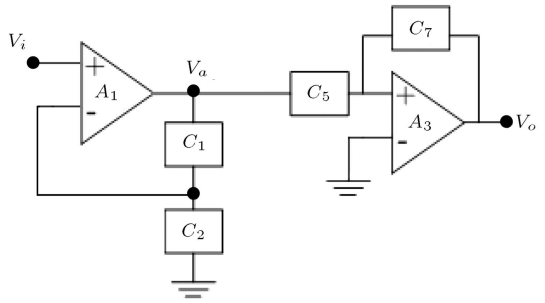

Figure 11. Simplified schematic of the instrumentation amplifier.

We assume that the input signal is a single frequency sine wave, $v_i = A.\cos(\omega.t)$, and the MOSCAP is a first-order nonlinear capacitor, i.e. $C_i = c_i(1 + \alpha_i.v_i)$ with non-linearity factor of α_i;

- We have calculated the effect of capacitors of the first-stage amplifier (C_1 and C_2 in Figure 11) on the THD of the amplifier's first-stage output. THD is calculated from Eq. (2) according to the relation between input and output and calculating the harmonic of the first-stage output wave:

$$\text{THD}_1 \approx \frac{\frac{A.c_2}{2c_1}\left(\alpha_2 - \frac{c_2.\alpha_1}{c_1}\right)}{1 + \frac{c_2}{c_1}}. \tag{2}$$

  Assuming that the first stage is linear and the nonlinearity comes from the second stage, Eq. (3) can be obtained for the THD of the second stage:

$$\text{THD}_2 \approx (\alpha_5 + \alpha_7.G)\frac{A}{2}, \qquad G = \frac{c_5}{c_7}. \tag{3}$$

  As you can see in Eq. (3), nonlinearity of C_7 has a very important effect on the THD, as its nonlinearity factor (α_7) is multiplied by the second-stage gain. Nonlinearity of first-stage capacitors does not affect the output nonlinearity, since the values of C_1 and C_2 are equal.

- Nonlinearity of C_7 has the most important effect on the amplifier's output according to Eq. (3) and it needs to be reduced as much as possible. The technique that we have used to reduce the nonlinearity of C_7 is to implement it by x% MOSCAP and $(1-x)$% MIM capacitor, as shown in Figure 12. The value of the overall capacitor is then given by Eq. (4). Eq. (5), then, gives THD of the second-stage output.

$$C_7 = x.c_7(1 + \alpha_7.V_7) + (1 - x)c_7, \tag{4}$$

$$\text{THD}_2' \approx (\alpha_5 + x^2.\alpha_7.G)\frac{A}{2}, \qquad G = \frac{c_5}{c_7}. \tag{5}$$

  Assuming the area of C_7 implemented, completely, by MOSCAP to be "Δ", the area of C_7 implemented by the parallel combination of MIM and MOSCAP is then given by Eq. (6). THD and area characteristics for different values of x are illustrated in Figure 13.

$$\text{Area}(C_7) = x.\Delta + (1 - x).4\Delta. \tag{6}$$

  For example, THD decreases by half in case we implement 70% of C_7 by MOSCAP and the rest of it by MIM capacitor; but, the area increases by a factor of two in comparison to the case in which all of the C_7 is implemented by MOSCAP.

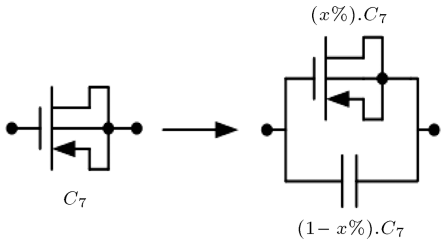

Figure 12. Implementation of C_7 for reducing its overall nonlinearity.

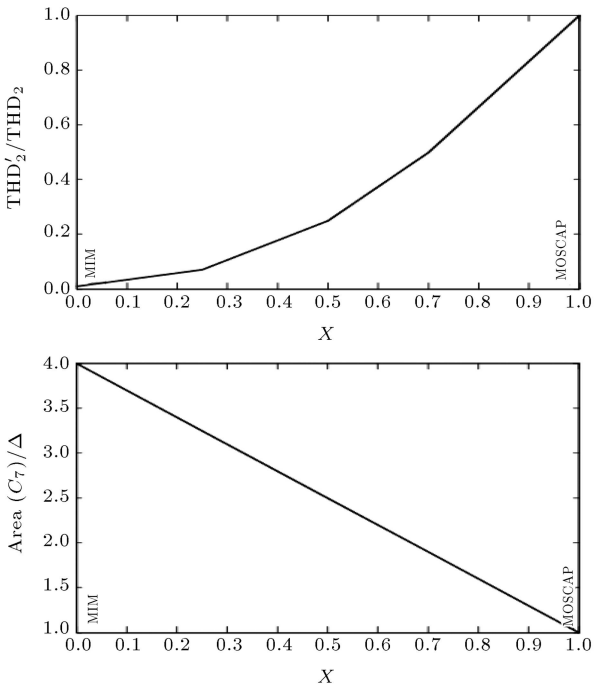

Figure 13. THD and area versus the percentage (x) of MOSCAP used in the implementation of C_7.

4.2. Choosing the MOSCAP structure which fits best with the circuits

The non-linearity of capacitors C_7 and C_8 of the instrumentation amplifier, illustrated in Figure 6, has the biggest impact on the output linearity according to Eq. (3). Due to the resistive feedback path between the input and output of the second-stage OTA and capacitive coupling of the two stages of the amplifier (Figure 6), the DC voltage differences across C_7 and

C_8 are zero. Therefore, according to Figure 2, PCDM MOSCAP is used for these capacitors.

In our design, $C_1 = C_2$, which leads to a gain of 2 for the first stage. Note that the first stage is mainly in charge of high input impedance and low noise, and extracting the common-mode voltage and the overall gain is mainly obtained at the second stage. According to Eq. (2), THD1 is approximately equal to zero since $C_1 \approx C_2$. On the other hand, the voltages across C_{1-4} are not around zero and, hence, PCDM cannot be used for them; thus, single MOSCAP structure is used for these capacitors.

Capacitance values of C_5 and C_6 are 45 pF, which lead to the low cut-off frequency of less than 1Hz. Hence, these capacitors occupy a large area even if we use MOSCAPs. Therefore, it is better to try to use accumulation or inversion regions of the MOSCAP to reduce the area to 1/16 of its MIM capacitor counterpart (refer to Figure 1).

As mentioned before, the threshold voltage shifts by the source-bulk voltage. In this method, we apply a positive source-bulk voltage to decrease the depletion region width and, hence, increase the inversion region width. However, high positive voltage cannot be applied to the source-bulk since the source/drain-bulk diode conducts and consumes a large value of current. In our design, the voltage difference of the source-bulk is adjusted around 0.3 V to prevent the source-bulk diode from conduction. Bulk is connected to the ground via a large resistor to produce this voltage difference. Large resistor can be implemented by a transistor which is biased in the sub-threshold region (Figure 14). Dimension of this transistor needs to be much smaller than the MOSCAP dimension, so the parasitic capacitors do not affect the MOSCAP.

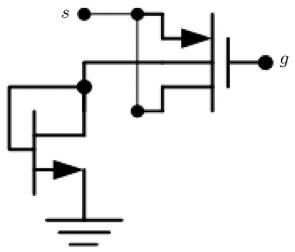

Figure 14. MOSCAP schematic and positive source-bulk voltage.

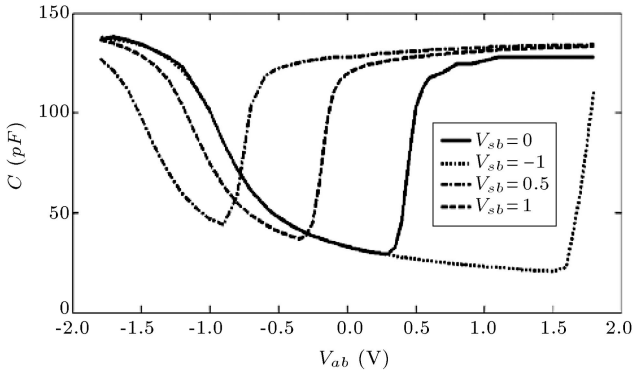

Figure 15. Capacitance variations due to source-gate voltage variation and source-bulk voltage variation ($W = 500$ μm, $L = 30$ μm).

As it was mentioned earlier, inversion region of the MOSCAP increases if a positive voltage is applied to the source-bulk (Figure 15). Hence, we can achieve the inversion region of MOSCAP by applying appropriate voltage difference between source and gate.

The output voltage of the second-stage amplifier (Figure 6) is adjusted to be 0.45 V to have the maximum swing at the output of the amplifier. The input voltage of the second-stage OTA (the voltage at node g in Figure 14) is 0.45 V, too, because of the second-stage pseudo-resistor and capacitor feedback. Buffers are used at node a and a′ of Figure 6 (and node s of Figure 14) to produce voltage difference of almost 0.5 V between C_{5-6} source-gate (to achieve inversion region with $V_{sb} = 0.3$V); hence, the appropriate voltage shift (around 0.95 V) is applied to the first-stage output voltage.

The inversion region of MOSCAPs C_5 and C_6 is obtained by a positive source-bulk voltage (0.3 V) and a voltage of 0.5 V across their source-gate terminals. In this way, the maximum value of the capacitor is obtained. Table 1 summarizes how each capacitor is implemented in our design of the ECG amplifier as well as the sizes of MOSCAPs.

4.3. MOSCAP nonlinearity effect cancellation

The MOSCAPs C_5 to C_8 are not completely linear in their operating voltage ranges. For cancelling the nonlinearity of C_5, according to Eq. (3), α_5 can be set to $-G\alpha_7$. This makes THD_2 equal to zero.

Table 1. Implementation of the MOSCAPs capacitors.

Capacitors	Way of implementation	Size of MOSCAPs
C_1-C_4	MOSCAP in depletion mode	$W = 83$ μm, $L = 10$ μm
C_5-C_6	MOSCAP in inversion mode with $V_{sb} > 0$	$W = 154$ μm, $L = 30$ μm
C_7-C_8	PCDM	($W = 11$ μm, $L = 8.6$ μm), ($W = 3$ μm, $L = 8.6$ μm)

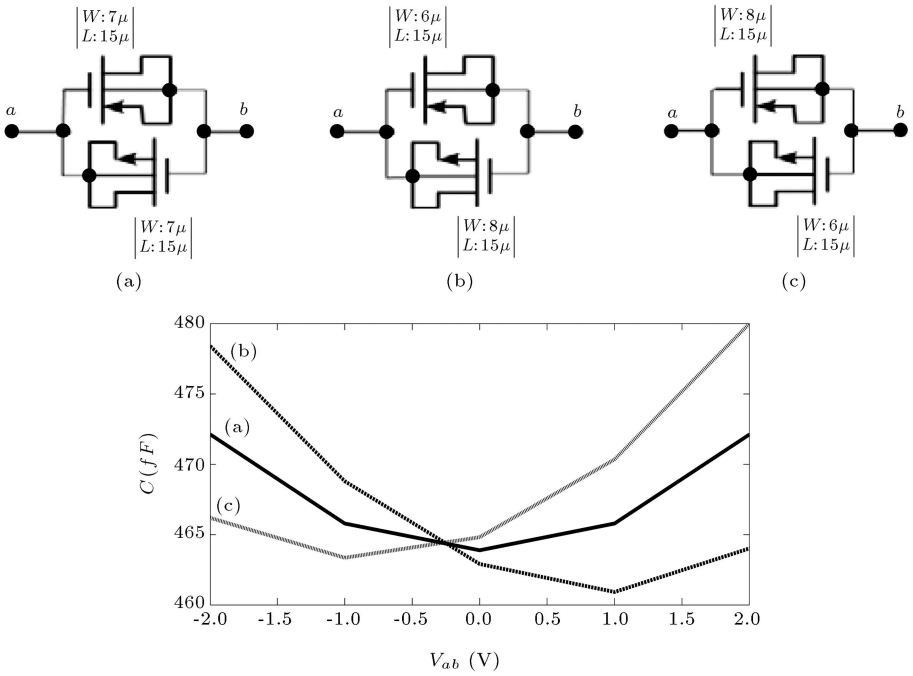

Figure 16. Slope changes around zero voltage due to changes in the sizes of transistors in PCDM structure.

Referring to Figure 15, it is clear that a MOSCAP has a slight positive slope in the inversion region. This allows the designer to cancel the nonlinearity of the MOSCAPs of the second stage by setting the slopes of the capacitance-voltage curve of C_7 and C_8 equal to $-\frac{\alpha_5}{G}$. Now, the question is that how we can adjust the slope of the capacitance-voltage curves of these capacitors. We have implemented C_7 and C_8 using parallel combination of two MOSCAPs as shown in Figure 16. Depending upon the size of the two parallel MOSCAPs, the slope of the capacitance-voltage curve can be changed. This is illustrated in Figure 16. Using this technique, we have been able to reduce the THD of the amplifier from 0.87% to 0.68% at 60 Hz.

It is worth mentioning that the above technique of adjusting the slopes of the capacitance-voltage curve can be used in the case of circuits with lower supply voltages, where it is not possible to use any other technique (like the one presented in the previous section) to reduce the non-linearity of MOSCAPs.

5. Results

Simulation is carried out in TSMC 0.18 μm technology with 1 V supply voltage. The overall circuit specifications are presented in Table 2.

Table 2. Circuit specifications.

Gain	Bandwidth	Total power consumption	Noise
46.18 dB	0.3-150 Hz	72 nW	7.8 μV_{rms}

Table 3. Power dissipation of each stage.

Stages	Power	Power percentage for each stage
First stage	42 nW	58.3%
Second stage	22 nW	30.5%
The OTA used in the right-leg driver	1 nW	1.38%
Right-leg drive buffer	5nW	6.9%

Power consumption of each stage can be determined by the properties and requirements of the stage. The power consumption of different parts of the ECG amplifier is presented in Table 3. The largest power budget is considered for the first stage as it has the dominant effect on noise. The right-leg driver consumes the least percentage. A class AB buffer is used in this block to achieve the low power operation.

Figure 17 compares the CMRRs of the overall amplifiers for two different cases, i.e. with a class A buffer and with a class AB buffer with the same power consumption. As can be seen in this figure, class AB buffer has a CMRR at least 30 dB higher than the CMRR corresponding to the class A. The THDs in different frequencies are presented in Table 4.

In order to have a variable gain for the amplifier, the capacitors of the second-stage feedback path (C_7, C_8) are replaced by the structure shown in Figure 18. All the capacitors are implemented by the PCDM method with proper capacitance-voltage curve slopes. The frequency response of the amplifier is illustrated in the same figure.

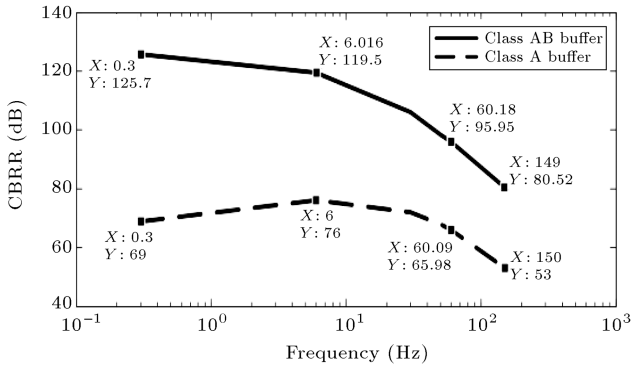

Figure 17. CMRR curves of class AB and A buffers in different frequencies.

Table 4. THD at different frequencies.

$[V_{\text{in}-} = 2$ mV, $f_{\text{in}} = 30$ Hz]	THD = 1.16%
$[V_{\text{in}} = 2$ mV, $f_{\text{in}} = 50$ Hz]	THD = 0.83%
$[V_{\text{in}} = 2$ mV, $f_{\text{in}} = 60$ Hz]	THD = 0.68%
$[V_{\text{in}} = 2$ mV, $f_{\text{in}} = 100$ Hz]	THD = 0.31%

Table 5. THD at temprature and process corners.

Corners	THD ($f = 100$ Hz)
TT	0.31%
FF	0.44%
SS	0.17%
FS	0.21%
SF	0.36%
TT at 0°C	0.19%
TT at 45°C	0.4%

The frequency response of the amplifier at different temperatures and process corners is illustrated in Figure 19. The THD is also presented in Table 5.

The performance of this design is compared with that of a few other ECG amplifiers in Table 6. In our design, the noise and THD are remained within acceptable ranges while the power consumption is reduced, considerably. This is achieved by using capacitors instead of resistors in the instrumentation amplifier. To avoid excessive chip area taken by the amplifier,

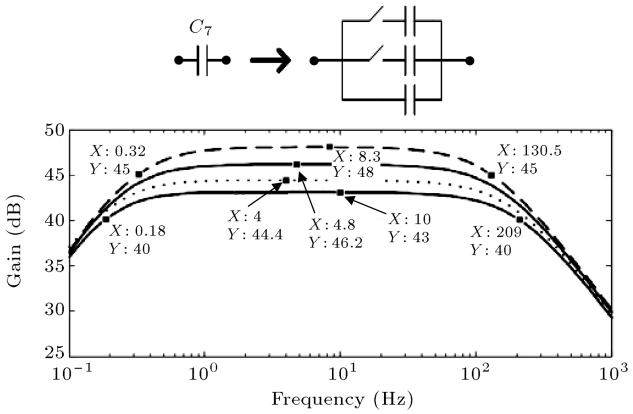

Figure 18. Switch and capacitor network and the circuit frequency response in case of having variable gains.

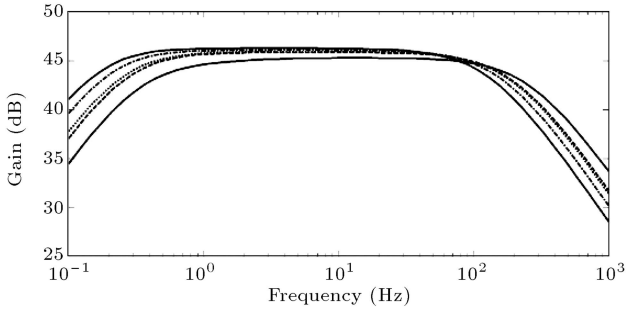

Figure 19. Circuit frequency response at temperature and process corners.

MOSCAPs are used. Two techniques are employed to reduce the impact of the non-linearity of MOSCAPs.

6. Conclusion

In this paper, MOSCAP is used in the instrumentation amplifier of an electrocardiogram application to reduce the area. Inversion region of the MOSCAP is used in a novel way to reduce the area of capacitors to 1/16 of that of the MIM capacitors. New techniques have been employed to reduce the impact of the MOSCAP nonlinearity. Therefore, the area of the amplifier's capacitors is about 10 percent of the area of the same amplifier with MIM caps. The total power consumption of the amplifier and the right-leg drive

Table 6. Comparison between this work and the previous works.

	Power (W)	Gain (dB)	Noise (μV_{rms})	BW (Hz)	CMRR (dB)	Technology
[3]	2.1 μ	20	6.7	0.5-100	110	65 nm
[5]	2.8 μ	45.3	8.1	290	90 at 60 Hz	0.5 μm
[4]	46.8 μ	46	0.68	0.1-150	107	0.18 μm
[6]	138 μ	45	0.27	0.2-200	127	0.18 μm
[8]	233 n	48-59	42	7-280	> 80	0.13 μm
This work	72 n	43-48	8.2	0.3-150	96 at 60 Hz	0.18 μm

circuit are 72nW due to using class AB buffer and using the transistors of OTA in the sub-threshold region. The referred input noise of the amplifier is equal to 48.2 μV_{rms}.

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