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Research Note

Read stability and power analysis of a proposed novel 8 transistor static random access memory cell in 45 nm technology

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Abstract. This paper presents analysis of the Static Noise Margin (SNM), power dissipation, access time and dynamic noise margin of a novel low power proposed 8T Static Random Access Memory (SRAM) cell for read operations. In the proposed structure, two voltage sources are used, one is connected with the bit line and the other is connected with the bitbar line in order to reduce the voltage swing at the output nodes of the bit and the bit bar lines. Simulation results for the read static noise margin, read power dissipation, read access time and dynamic noise margin have been compared to those of other SRAM cells, reported in different literatures. It is shown that the proposed SRAM cell has better static noise margin and dissipates less power in comparison to other SRAM cells. Analog and schematic simulations have been done in a 45 nm environment with the help of Microwind 3.1, using the BSimM4 model.

1. Introduction

Technology gets faster day by day. But, the faster the circuits are, the more is the power consumption and, hence, the battery life of many of the portable devices is reduced. As technology scales down, the leakage power starts to dominate. Memory circuits, such as SRAM, occupy considerable amounts of area in any digital Integrated Circuit (IC). To maximize power saving, designs that operate in sub-threshold regions have been proposed [1,2]. It has been proved that sub-threshold region operation leads to a reduction in operational energy for logic [3]. But, when technology scales down to as low as 45 nm, there is a possibility that the other above-threshold SRAMs may also be used for successful sub-threshold operations, thereby, entering into ultra low-power operation. So, development of a memory technology with higher stability, i.e. higher static/dynamic noise margins and lower leakage power consumption characteristics, is, therefore, highly desirable. The common approach to meet the objective of low power design is to add more transistors to the original 6T cell. In the 7T cell model proposed in [4], the activity factor is reduced by adding one more transistor, which reduces the dynamic power dissipation. In another approach, a single ended 6T SRAM with only one bit or bitbar line is used for the read operation [5]. Aly et al. [6] proposed a novel 7T SRAM cell for low power cache design. In that design, an extra transistor is used for the read operation. Other approaches, like 8T yield-

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driven near sub-threshold SRAM [7], 9T SRAM [8], and a symmetric and balanced 11T SRAM [9], have also been proposed to improve the performance of the SRAM cell. In [10], a 9T SRAM cell has been proposed in which a separate read/write operation is performed for improving power dissipation. A 7T SRAM cell proposed in [11] shows the reduction in the bit line capacitance to improve the power dissipation. Charging and discharging the SRAM cell depends on the bit line capacitance value. So, by improving the charging and discharging of the SRAM cell, power dissipation can also be decreased. A charge sharing technique for reducing power dissipation has been proposed in [12]. Due to the charge sharing technique, the bit line voltage swing is reduced and results in a reduction in the dynamic power dissipation of the SRAM cell. A low power cache design is proposed [13], where two separate bit lines are used for performing the write operation. A negative word line scheme is shown in [14] to minimize the leakage current of the cell access transistors. In another approach, a supply voltage feedback technique has been proposed [15]. By using the feedback supply, the pull-up current during the write cycle is reduced, which enables a low voltage write operation. In [16], a conscious SRAM cell design for low static energy dissipation is discussed. In this cell design, a body bias concept is used for reducing static power dissipation. In [17], a robust dual threshold SRAM has been described in which the dual threshold concept has been used for reducing both static and dynamic power dissipations. Sub-threshold current is also an important factor in power dissipation, but, reducing the sub-threshold current also affects the stability, readability and writability of the cell. In [18], an ultra low power sub threshold SRAM cell with higher stability has been proposed. A statistical design of the 6T SRAM bit cell has been described in [19]. This method is based on the widths and lengths of the CMOS transistors used in SRAM cell design. A new current mode sense amplifier is discussed in [20]. In this SRAM model, a low power current mode sense amplifier is used for reduction of the read power dissipation. In another symmetric 11T SRAM cell model, both read and write powers are reduced [21]. A hybrid SRAM cell shown in [22] uses double gate MOS technology to minimize power dissipation. In [23], a low power 7T SRAM design has been presented, which considers performance variations due to process, voltage and temperature. This SRAM design increases the read/write stability at the cost of extra transistors. A popular approach for leakage reduction is data retention with a gated ground [24]. A voltage reduction technique, called stacking, to reduce SRAM leakage power during the standby mode, is discussed in [25]. An offset voltage sense amplifier is used to reduce deterioration of the read speed and cell stability at low supply voltage in [26]. In [27], sub-threshold and near-threshold SRAM designs have been discussed, where only one bit line is used for the write/read operation. An 8T SRAM that allows an efficient bit-interleaving and can achieve soft-error tolerance is presented in [28]. In [29], a P-P-N based 10T SRAM cell for low power has been discussed in which a cross coupled P-P-N pair is used.

Row and column decoders have been used for selecting the word lines and bit lines, respectively, in the memory design. When the column is not accessed, the leakage current flowing through the extra transistor may cause a severe voltage drop in the Read Bit Line (RBL), thus, errors may appear at the output. Since it may not be possible to design a high-density SRAM using 8T cells, this conclusion leads to an investigation of other cells, such as 10T and 9T structures [30,31]. Other cell architectures are proposed in [32,33], where dynamic Forward Body Bias (FBB) is used in active mode. Here, super high-Vt transistors are used, together with FBB, to dynamically reduce the active leakage in SRAM cells. In [34], the authors propose a cell-level implementation of power gating in which a sleep transistor is added to the supply or the ground path of a SRAM cell. Power gating sensibly reduces leakage with the help of the stacking effect of self reverse-biasing series-connected transistors. The extra transistor produces the stacking effect in conjunction with the SRAM cell transistors, when the gated transistor is turned off. Gating can be coupled with a dual-threshold voltage process technology to achieve even larger reduction in leakage. SRAM cells use low-Vt transistors to keep high performance, and the sleep transistors are used to achieve additional leakage reduction. The main limitation of this basic cell-level power gating is the persistence of the stored data. In order to address the problems associated with data retention, possible solutions are presented in [35] and [36]. In [37,38] a more complicated arrangement for threshold voltage control, called the Auto-Back gate-Controlled Multi-Threshold CMOS (ABC-MT-CMOS), is proposed. The approach shown in [39] exploits the stacking effects and body biasing.

In this paper, a novel 8T SRAM cell is proposed for read operation. Read static margin, read power, read access time and dynamic noise margin are calculated for the proposed SRAM cell and compared to those of other existing SRAM cells. In the proposed SRAM cell, one voltage source is used at each output node. These voltage sources reduce the voltage swing at the output nodes during switching activity. Reduction in voltage swing causes a reduction in dynamic power dissipation. Voltage sources also improve the static noise margin and dynamic noise margin of the proposed SRAM cell.

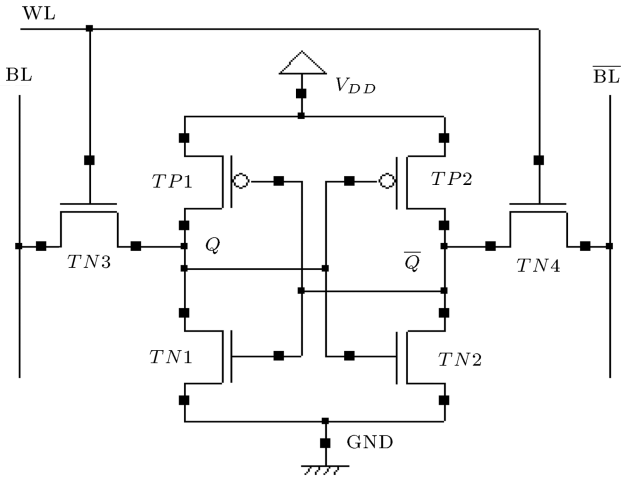

Figure 1. Conventional 6T SRAM cell.

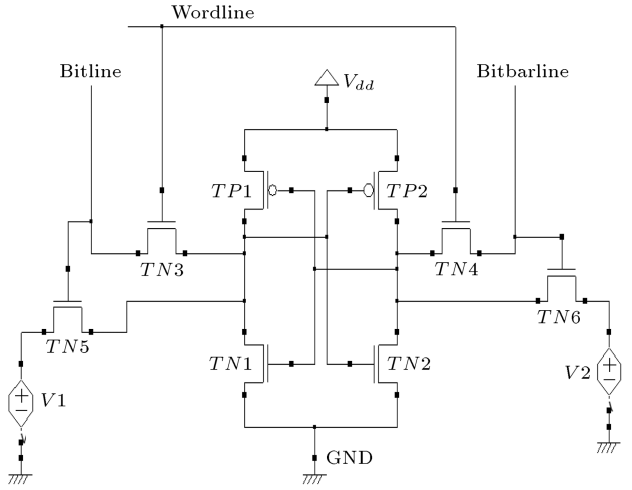

Figure 2. Proposed 8T SRAM cell.

The paper is organized as follows: Section 2 shows the design of the conventional 6T SRAM cell. Section 3 describes the circuit design and working principle of the proposed 8T SRAM cell for read operation. Section 4 elaborately discusses the simulation results of the proposed SRAM cell for Dynamic Noise Margin (DNM), Static Noise Margin (SNM), access time and power dissipation during the read operation, and, finally, Section 5 concludes the paper.

2. Conventional 6T SRAM cell

Figure 1 shows the circuit diagram of a conventional SRAM cell. Before the read operation begins, the bit line, BL, and the bitbar line, $\overline{\text{BL}}$, are pre-charged to as high as V_{dd}. When the word line (WL) is selected, the access transistors are turned on. This causes a current to flow from V_{dd} through the pull-up transistor $TP1$ of the node storing "1". On the other side, current will flow from the pre-charged BL to ground, thus, discharging the $\overline{\text{BL}}$ line. Thus, a differential voltage develops between the BL and $\overline{\text{BL}}$. This small potential difference between the bit lines is sensed and amplified by the sense amplifiers at the data output. A conventional 6T SRAM cell works on a full voltage swing. This means that if the operating frequency of the SRAM cell is increased, then, the dynamic power dissipation will also be increased. Hence, for high speed CMOS operation, the conventional SRAM cell is not a good choice. Also, a conventional 6T SRAM cell has been found to be unstable beyond below 130 nm technology, and results in a low read Static Noise Margin (SNM).

3. Proposed 8T SRAM cell

In order to overcome the problem associated with conventional 6T SRAM, this paper proposes a novel 8T SRAM architecture to achieve very low power dissipation and better stability. In the proposed design, two voltage sources, $V1$ and $V2$, are connected to the outputs of the bit line and the bitbar line, respectively. Two NMOS transistors, $TN5$ and $TN6$, are used. One is connected with the bit line and the other is connected with the bitbar line directly to switch ON and switch OFF the power source during write/read operations. The proposed design has been illustrated in Figure 2. These power sources reduce the voltage swing at the output node when the write/read operation is being performed.

The dynamic power may be expressed as:

$$P_{\text{dynamic}} = \alpha C V_{dd} V_{\text{Swing}} f, \tag{1}$$

where:

C	Load capacitance;
α	Activity factor;
f	Clock frequency;
V_{Swing}	Voltage swing at the output node;
V_{dd}	The power supply voltage.

So, in the conventional VLSI design, as the frequency increases, the dynamic power dissipation also increases, because the dynamic power depends on the operating frequency [40]. The two voltage sources, $V1$ and $V2$, reduce the swing voltage, which is used during the switching activity from "0" to "1" and vice-versa.

For performing the read operation in the proposed SRAM cell, a precharge circuit and sense amplifier are used. Precharge circuits perform the precharge operation before the read operation starts. The sense amplifier will produce the potential difference between the bit line and the bitbar line and also amplify the signal during the read operation.

3.1. Precharge circuit

The circuit arrangement for the precharge circuit is shown in Figure 3. When an equalizing pulse is given

to the PMOS transistors, $TP3$ and $TP4$, it precharges the bit line and bitbar line to V_{dd}. In the schematic of precharging, $TP3$ and $TP4$ are the load transistors and $TP5$ is used to equalize the voltage equally to the bit line and bitbar line. The purpose of the precharge circuit is to charge the bit line and bitbar line to supply voltage before the starting of the read operation. The precharging enables the bit-lines to be charged to V_{dd} for the entire time period, except during the write operation.

3.2. Sense amplifier

Sense amplifiers are used to detect small currents that flow through the access transistors or the small voltage differences that occur during charge sharing. For designing the sense amplifiers, cross-coupled inverters are used to sense a small change of voltage on the bit line and the bitbar line. The arrangement for the sense amplifier is shown in Figure 4.

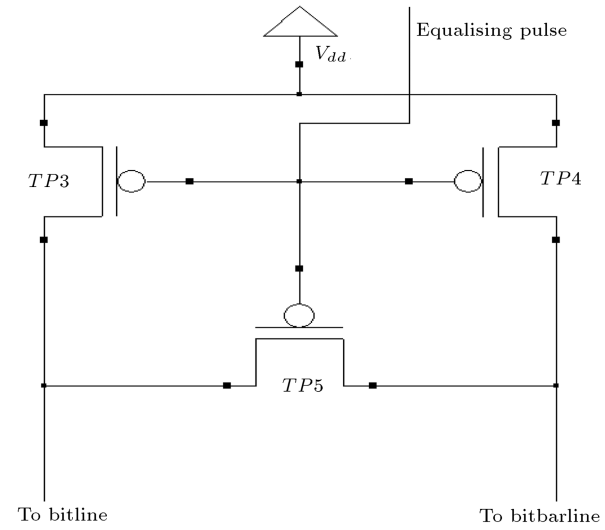

Figure 3. Precharge circuit.

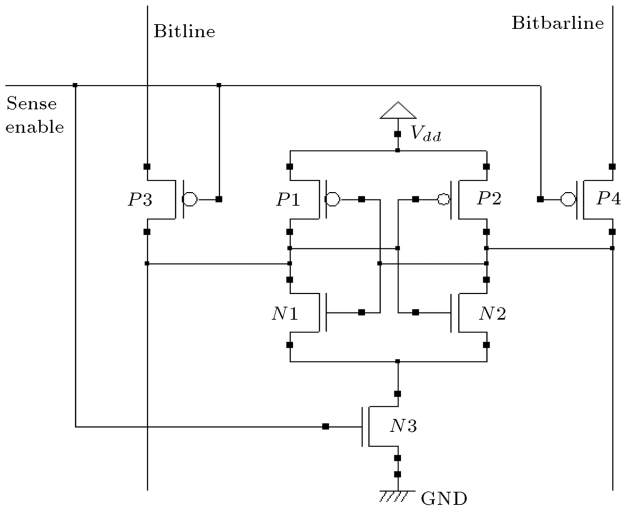

Figure 4. Sense amplifier.

The sense amplifiers are active only during the read operation. During the read cycle, the read circuit is enabled, the cross-coupled inverters of the sense amplifiers sense the difference in voltage between the bit line and the bitbar line, and the output of the inverters is either '1' or '0', depending on the voltage levels sensed. The read circuit and the sense amplifier are isolated from the remaining circuits by the two PMOS transistors, $P3$ and $P4$, connected between the bit line, the bitbar line and the sense amplifier, respectively. The sizings of the transistors are done using the same ideology as that of the SRAM cell discussed earlier.

To perform the read operation in the proposed SRAM cell, firstly, the bit line and the bitbar line are charged to V_{dd}. The operation of precharging is performed by the precharge circuit, shown in Figure 3. After that, the sense amplifier is enabled to sense the voltage difference between the bit line and the bitbar line. The sense amplifier takes the difference voltage or current of the bit line and the bitbar line and, finally, produces either '1' or '0' output, according to the voltage stored on the bit line and the bitbar line. Figure 5 shows the waveform during the read operation of the proposed 8T SRAM cell.

During switching activity from '0' to '1' or '1' to '0', the swing voltage is required at the bit line or the bitbar line. This extra voltage increases dynamic power dissipation. In the proposed 8T SRAM model, voltage sources, $V1$ and $V2$, reduce the voltage swing and improve the switching activity during write/read operation. As the frequency increases, the switching activity also increases, and this increases the dynamic power dissipation. But, the voltage source reduces its voltage swing simultaneously at the output. So, at higher frequency, the dynamic power dissipation

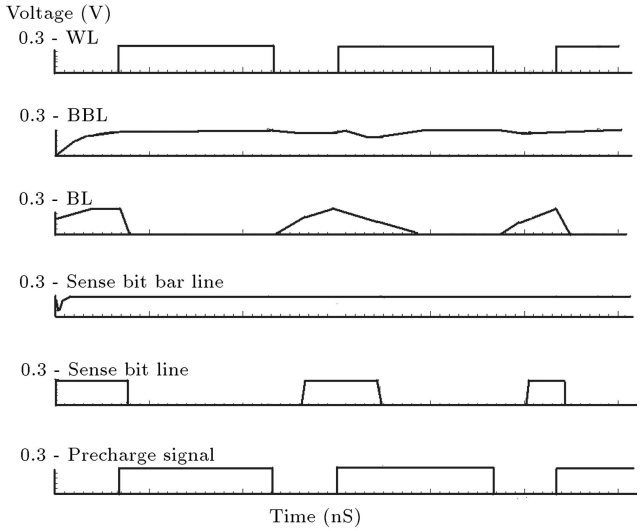

Figure 5. Read operation waveform of the proposed SRAM cell with sense amplifier.

is found to be much less compared to other SRAM models reported in different literature. These two voltage sources also provide extra voltage during the write/read operation on the bit line, the bitbar line and the word line. The extra voltage will also provide a low voltage swing for the sense amplifier during the read operation. Stability is also improved, due to the better switching capability of the proposed SRAM cell, as compared to other SRAM cells.

4. Simulation results and discussions

In this section, read static noise margin, read power dissipation, read access time and dynamic noise margin are calculated, and the simulated results are compared to those of other SRAM cells. Analog and schematic simulations have been done in a 45 nm environment, with the help of Microwind 3.1, by using the BSimM4 model.

4.1. Read Static Noise Margin (SNM) analysis

The stability of the SRAM cell is usually defined by the Static Noise Margin (SNM), which is the maximum value of DC noise voltage that can be tolerated by flipping the internal state. The read SNM of the proposed SRAM cell at 0.6 V is calculated and compared to that of different SRAM cells. For calculating the read static noise margin, the following equations are used [41]:

$$\mathrm{SNM} = \left[(\mathrm{NM_H})^2 + (\mathrm{NM_L})^2\right]^{1/2}, \tag{2}$$

$$\mathrm{NM_H} = \mathrm{V_{OH}} - \mathrm{V_{IH}}, \tag{3}$$

$$\mathrm{NM_L} = \mathrm{V_{IL}} - \mathrm{V_{OL}}, \tag{4}$$

where:

V_{IH} Minimum high input voltage;
V_{IL} Maximum low input voltage;
V_{OH} Minimum high output voltage;
V_{OL} Maximum low output voltage.

Table 1 shows the SNMs of different SRAM cells for the read operation. The read SNM for the proposed SRAM cell is 407 mV. From Figure 6, it is evident that the read SNM of the proposed SRAM cell has a higher value, as compared to the other SRAM cells. This justifies the fact that the proposed SRAM cell is more stable for read operations than that of other cells.

4.2. Read power dissipation analysis

The proposed SRAM is simulated using 45 nm CMOS technology with a 0.3 V power supply, and the results for read power dissipation are compared to those of other existing SRAM cells. Comparison of the read powers of the proposed SRAM for read '0' and read '1' is shown in Table 2. From Figure 7, it is evident that the proposed SRAM cell dissipates 0.093 nW, 0.326 nW of power for read "1" and read "0" operations, respectively. That means the proposed SRAM dissipates less power in comparison to all existing SRAM cells.

Table 1. Read static noise margin for different SRAM cell.

Cell	Read static noise margin (mV)
6T SRAM [5]	146
8T SRAM [7]	310
9T SRAM [8]	315
10T SRAM [1]	357
Proposed SRAM	407

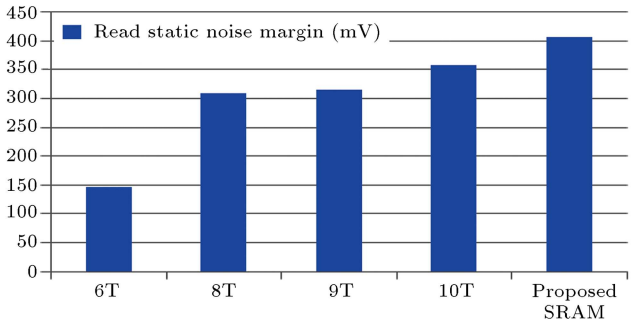

Figure 6. Static noise margin comparison for read operation.

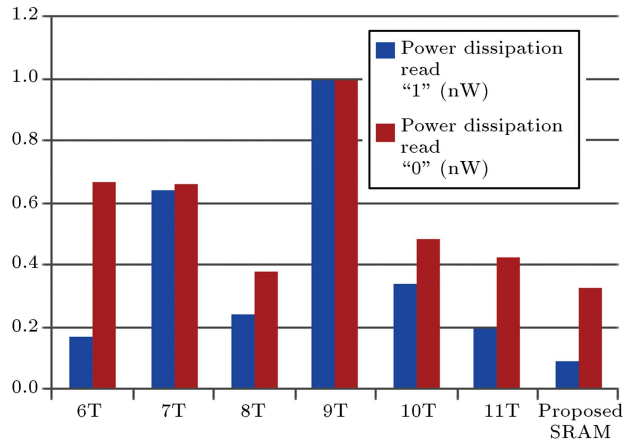

Figure 7. Read power dissipations in different SRAM cells.

4.3. Read access time analysis

In this section, the read access time of the proposed SRAM cell is calculated and compared to that of existing SRAM cells. Access time has been calculated in a 45 nm technology environment with a 0.3 V power supply. Read access times for different SRAM cells are shown in Table 3. Table 3 shows that the read access time of the proposed SRAM cell is 359 pico seconds for the read operation.

Table 2. Power dissipation during read operation.

Cell	Power dissipation read "1" (nW)	Power dissipation read "0" (nW)
6T SRAM [5]	0.171	0.665
7T SRAM [6]	0.640	0.659
8T SRAM [7]	0.241	0.379
9T SRAM [8]	0.998	0.998
10T SRAM [1]	0.338	0.482
11T SRAM [9]	0.195	0.424
Proposed SRAM	0.093	0.326

Table 3. Read access times for different SRAM cells.

Cell	Read access time (ps)
6T SRAM [5]	4.094
7T SRAM [6]	240
8T SRAM [7]	210
9T SRAM [8]	466
10T SRAM [1]	6.05
11T SRAM [9]	203
Proposed SRAM	359

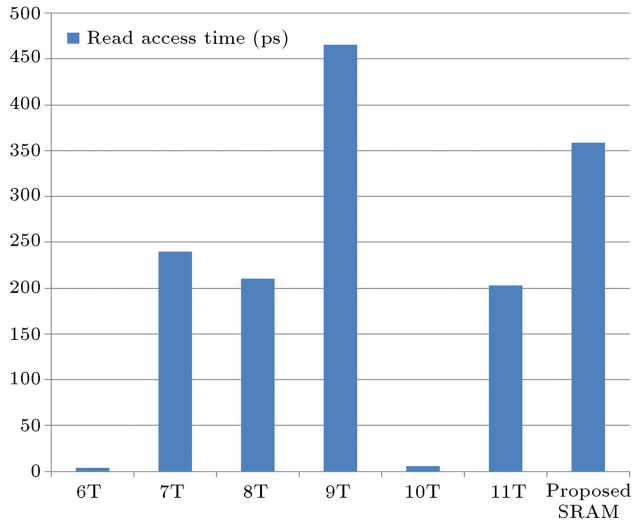

Figure 8. Access time comparison for read operation.

Figure 8 shows that the read access time for the proposed SRAM cell is very much higher than that of the 6T and 10T SRAM cells. This is because the access time depends on the voltage swing, and, in the proposed SRAM cell, the voltage swing is reduced during the read operation. So, access time for the proposed SRAM cell is poorer than that of the other SRAM cells. But, the proposed 8T SRAM results in better access time than that of the 9T SRAM model proposed in [8].

4.4. Dynamic noise margin analysis

This section introduces the write Dynamic Noise Margin (DNM) approach for measuring the stability of the proposed 8T SRAM cell. To define the DNM, the first concern is the criterion for a write failure. A write failure occurs when the write time is larger than the word line pulse width. The word line pulse width depends on a number of factors, such as the number of drivers of bit lines and the word line. Write time is defined as the time when the node storing '1' is pulled down from V_{DD} to a critically low value. This write failure definition is valid for most of the reasonable write cycles. Analysis of the DNMs for logic gates has shown that both noise amplitude and noise duration are critical for dynamic stability [42].

Static noise is pulsed noise with an infinitely long pulse length. In general, it is found that the dynamic noise margins are larger than the static ones, because, during short pulses, higher noise amplitudes may be applied. Dynamic stability analysis was applied to the SRAM cell, which resulted in an analytical model for evaluating its dynamic noise margin while in the standby mode. This model assumes that the noise source is a current noise pulse injected into the node storing '0'. For a given noise amplitude, the model estimates the critical pulse width, i.e. the minimum pulse duration for the noise to flip the cell's state. Dynamic instability occurs when the injected noise causes the cell's state to follow a trajectory that crosses the boundary of attraction regions. In order to evaluate the write ability and read ability of a cell more precisely, a metric which takes the dynamic write/read behaviour into account must be used. On a successful write, Q and $\overline{Q}$ cross over and eventually settle at V_{DD} and 0V, respectively. The word line pulse width (T_{wl}) determines whether the two waveforms cross and the write is successful or not. This proposed 8T SRAM model uses the minimum world line pulse width (T_C) for the cell to flip ultimately to the correct new state as a metric for the dynamic write margin. Figure 9 shows the Trajectory for Write "1" Operation.

In order to understand T_C as a useful metric, let us relate it back to the dynamic stability analysis. Figure 10 shows the trajectories of Q and $\overline{Q}$ for writing '1', when T_{wl} is equal to $T_C - 1$ ps, T_C, and $T_C + 1$ ps. The trajectories all overlap each other as they approach the separatrix, but they diverge at that point, because the word line pulses end at slightly different times. The two trajectories for $T_{\text{wl}} \geq T_C$, then, overlap again, as they converge to the newly written value, but, the trajectory for $T_{\text{wl}} < T_C$ falls back to the starting state. This simulation clearly shows that T_C is the word line pulse width that causes the state of the cell $(\overline{Q}, Q)$ to cross over the separatrix when the word line drops to 50% of V_{dd}. It may also be noted that variation has pushed the separatrix off the line, $Q = \overline{Q}$. Process

Table 4. Dynamic noise margin variation with noise pulse width.

Word line pulse width	Dynamic noise margin (mV)		
	Conventional 6T SRAM cell [5]	10 SRAM cell [43]	Proposed 8T SRAM cell
10 ps	820	1460	1712
100 ps	198	390	540
1 ns	197	388	539.4
10 ns	197	388	539.1
100 ns	196.5	387.7	538.8

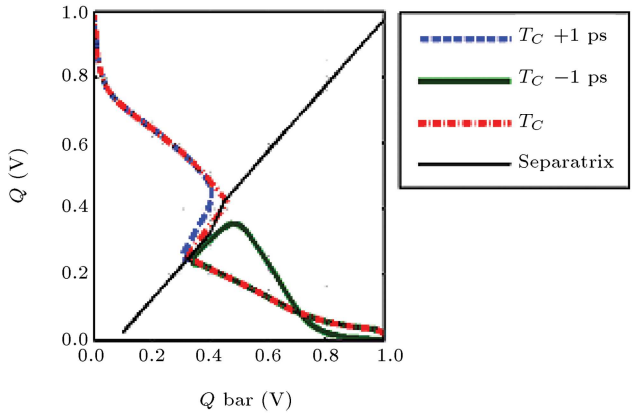

Figure 9. Trajectory for write "1" operation.

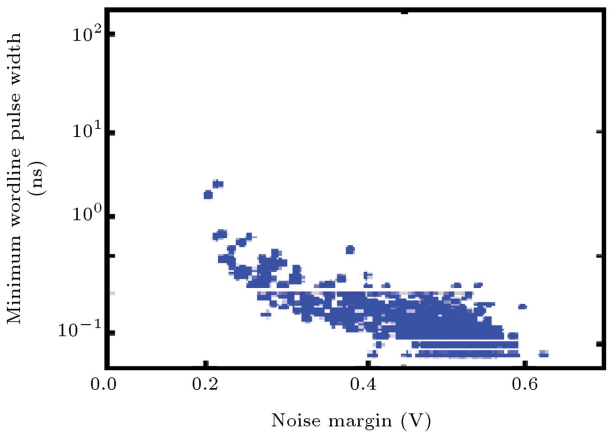

Figure 10. Monte-Carlo simulation curve for proposed SRAM cell.

variations will make T_C difficult to predict, since both the trajectories of the cell state during the word line pulse, and the separatrix of the cell, will vary with the device parameters.

The DNM of the proposed SRAM cell is 0.54 V at 100 ps wordline pulse width and its value at 100 ns is 0.538 V. So, the DNM value is almost constant as the wordline pulse increases. From Figure 10, it is evident that the density of the blue dots is higher in between 0.45 V and 0.6 V. This justifies the fact that the stability of the proposed 8T SRAM cell is better between these voltage values. Reduction in swing voltage causes a reduction in dynamic power dissipation. Improvement in switching activity also improves the dynamic noise margin.

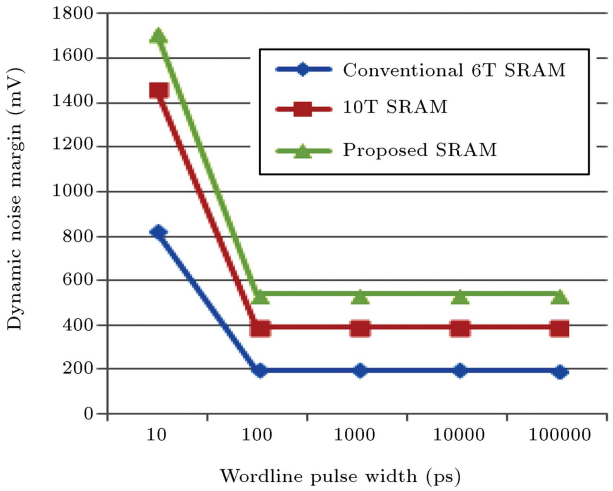

Figure 11. Dynamic noise margin comparison of SRAM cells.

Table 4 shows the variation of DNM with respect to wordline pulse width time. Table 4 shows that when the pulse width time goes from 10 ps to 100 ps, the DNM goes down to 70% of its original value. After 100 ps of time, as the width time still increases, the DNM becomes almost constant. At this point, the DNM values get saturated and approach their SNM values. This affirms that the proposed design is more stable compared to the conventional 6T and 10T SRAM cells. The comparison of DNMs among 6T, 10T cells and the proposed SRAM cell has been shown in Figure 11. Figure 11 shows that after 100 ps, all SRAM cells reach static conditions.

5. Conclusions

Power dissipation and stability will be major issues as the demand for high speed battery operated devices increases. In this paper, the dynamic noise margin, the read static noise margin, access time and power dissipation are analyzed during the read operation of the proposed 8T SRAM cell. These values are compared to those of different existing SRAM cells.

The proposed SRAM cell has a higher read static margin of 407 mV, which shows the better stability for read operation as compared to the other SRAM cells. Similarly, the proposed 8T SRAM cell dissipates 0.093 nW and 0.326 nW of power during read '1' and read '0' operations, respectively, which is much less than those of other existing SRAM cells. The dynamic noise margin for the proposed SRAM cell is 1712 mV at 10 ps, which shows that the proposed SRAM cell has better stability than the other compared SRAM cells. The read access time for the proposed SRAM is 359 ps, which is poorer than that of the other SRAM cells. This is because of the reduction in voltage swing. But, low power dissipation and higher stability can easily overcome this drawback. The proposed SRAM provides low power solution for high speed battery operated devices like laptops, biomedical equipment etc.

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