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Novel spatially arranged mixed carbon nanotube bundle interconnects - Impact on delay and power

M.K. Majumder*, **B.K. Kaushik and S.K. Manhas**

Microelectronics and VLSI Group, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee, Uttarakhand, India.

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Equivalent Single Conductor (ESC) model;
Propagation delay;
Power dissipation;
VLSI interconnects.

Abstract. This research paper introduces novel structures of Mixed CNT Bundle (MCB) based non-conventional arrangements of single- and multi-walled carbon nanotubes. A hierarchical Equivalent Single Conductor (ESC) model is used to analyze the propagation delay and power dissipation of CNT bundles. The hierarchical model of MCB considers two types of CNT: one Single-Walled CNT (SWCNT) and other Multi-Walled CNT (MWCNT). The ESC model of MCB is a combination of ESC models of bundled SWCNT and bundled MWCNT. Initially, simple ESC models of bundled SWCNT and bundled MWCNT are derived, considering parasitic elements like resistance, capacitance and inductance. Later, these two equivalent models are combined to build up the final ESC model of novel MCBs. It has been observed that the overall delay and power dissipation are reduced by 48.1% and 20.9%, respectively, for the novel MCB which has a horizontal arrangement of SWCNTs and MWCNTs in equal halves.

1. Introduction

Interconnect delay is a major factor in determining the performance of VLSI circuits. As technology is scaled down, interconnect delay dominates gate delay. This is because, in deep submicron technologies, interconnect can no longer be seen as a simple resistor, but the associated parasitic, such as capacitance and inductance, also needs to be considered [1]. In nanoscale VLSI technologies, it has become increasingly difficult for conventional copper based electrical interconnects to satisfy the design requirements of delay, power and bandwidth. Therefore, researchers are forced to find an alternative solution for future global VLSI interconnects.

In recent years, carbon nanotubes (CNTs) have aroused much research interest in the area of microelectronics/nanoelectronics, due to their unique physical properties, such as higher thermal stability [2], mechanical strength [3], higher current carrying capability [4] and ballistic transport phenomenon [5]. CNTs, known as allotropes of carbon [5], are made by rolling graphene sheets into a cylindrical form. Depending on the number of rolled up graphene sheets, CNTs are categorized as Single-Walled CNT (SWCNT) and Multi-Walled CNT (MWCNT). Double-Walled CNT (DWCNT) is a special type of MWCNT, wherein two concentrically rolled up graphene sheets are present. Bundled SWCNT is formed by a number of SWCNTs. Due to their structural simplicity, SWCNTs have attracted more attention than DWCNTs and MWCNTs [6].

*. *Corresponding author. Tel.: 01332 286448, +919458947091*
E-mail addresses: manojbesu@gmail.com (M.K. Majumder), bkk23fec@iitr.ac.in (B.K. Kaushik), samanfec@iitr.ac.in samanfec@iitr.ernet.in (S.K. Manhas)

However, significant progress has been achieved in characterization of the interconnect performance for bundled SWCNT and MWCNT [6,7].

Modeling and simulation of SWCNT and MWCNT interconnects have already become popular in addressing the effect of propagation delay, power dissipation, crosstalk, etc. [8-11]. Several research works [12,13] based on CNT fabrication demonstrate that a realistic nanotube bundle contains not only SWCNTs but also MWCNTs. In this scenario, recent research work [14,15] has focused on the geometry and modeling of Mixed CNT Bundle (MCB) based VLSI interconnects. The arrangements of MCBs are more complex than those of bundled SWCNTs and bundled MWCNTs. Thus, modeling such a bundle is not as easy as simple SWCNT or MWCNT bundles. This research paper introduces the unique modeling aspects and evaluation of interconnect performances for MCBs. Based on the placements of SWCNTs and MWCNTs in a bundle, three different MCB arrangements are proposed. The hierarchical model [14] is developed considering bundled SWCNT and bundled MWCNT arrangements. Based on the transmission line theory [16-23], an Equivalent Single Conductor (ESC) model is presented for bundled SWCNT and bundled MWCNT. Furthermore, the ESC model of MCB is build up with a combination of bundled SWCNT and bundled MWCNT. Using the ESC model of bundled and mixed CNTs, propagation delay and power dissipation are analyzed at global interconnect lengths. A Driver-Interconnect-Load (DIL) system employing a CMOS driver is used to analyze the performance. The interconnect line is modeled by equivalent bundled CNTs to study the effect of propagation delay and power dissipation.

The organization of this paper is as follows: Section 1 introduces recent research and briefs about the work carried out. Section 2 provides a detailed description of the spatial arrangements of bundled CNTs. The proposed ESC model and simulation details are described in Section 3. Based on the simulated results, propagation delay and power dissipation are analyzed for different CNT bundles in Section 4. Finally, Section 5 draws a brief summary of this paper.

2. Hierarchical model and spatial arrangement of MCBs

The hierarchical modelling of MCB is shown in Figure 1. The ESC model of MCB consists of one ESC model of bundled SWCNT and other ESC of bundled MWCNT [5,6]. Initially, the ESC expressions for coupling capacitance and tunneling conductance [16] are derived. The coupling capacitance in bundle interconnects arises because of the difference in the potential of each CNT in the bundle. Therefore, it is desirable

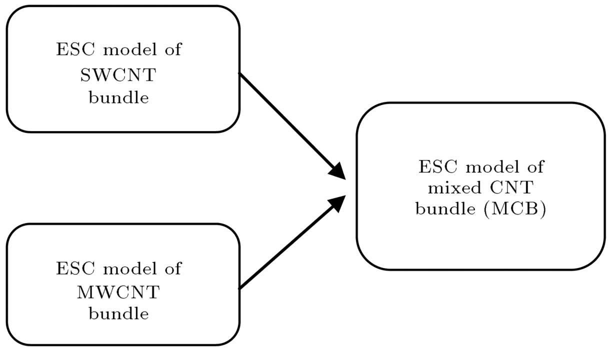


Figure 1. Hierarchy of ESC modeling for MCB structures [18].

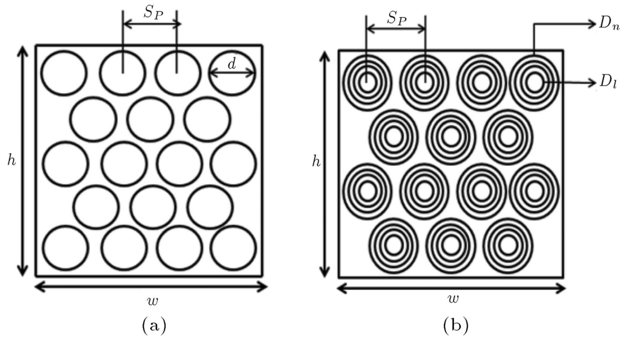


Figure 2. (a) Bundled SWCNT, and (b) bundled MWCNT.

to include the coupling capacitance in the ESC model of MCBs. This capacitance contributes to the overall delay of the interconnect line [17]. On the other hand, tunneling conductance appears between two shells in MWCNT, which primarily represents the intershell tunnel transport phenomenon, and exhibits a value of (3.7-20 kΩ)$^{-1}$/μm [16]. Due to the extremely small value, it actually does not affect the delay and power performance at global interconnect lengths [6,14,21,23].

The arrangements of bundled SWCNT and bundled MWCNT are shown in Figure 2(a) and (b), respectively. A SWCNT bundle consists of numbers of SWCNTs with diameter, d, and spacing, S_p. The total number of SWCNTs in a bundle can be expressed as [6,19]:

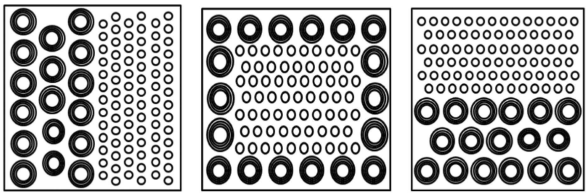
$$n_{\text{CNT}} = \begin{cases} n_W n_H - (n_H/2) & n_H \text{ is even} \\ n_W n_H - [(n_H-1)/2], & n_H \text{ is odd} \end{cases} \tag{1}$$

where:

$$n_W = \lfloor (w-d)/S_p \rfloor + 1,$$

$$n_H = \lfloor (h-d)/S_p \rfloor + 1. \tag{2}$$

n_H and n_W represent the number of rows and columns, respectively, n_{CNT} is the total number of SWCNTs in a bundle, and w and h are the bundle width and height, respectively. Similarly, a bundled MWCNT



(a) (b) (c)

Figure 3. Spatial arrangements of SWCNT and MWCNT in (a) MCB-I, (b) MCB-II and (c) MCB-III.

of width, w, and height, h, considers large numbers of MWCNTs in a bundle, as shown in Figure 2(b). Each MWCNT has a different number of shells, with diameters $d_1, d_2, d_3, \cdots, d_n$, where d_1 and d_n are the innermost and outermost shell diameters, respectively. It is assumed that the spacing between each shell is fixed, while the diameter of the outermost nanotube can change over a fixed interval. Intershell spacing, S_i, can be expressed as [7,20]:

$$S_i = \frac{D_n - D_{n-1}}{2} \approx 0.34 \quad \text{nm}. \tag{3}$$

Based on the specified placements of SWCNTs and MWCNTs in a bundle, three different MCB arrangements are proposed, as shown in Figure 3. SWCNTs and MWCNTs occupy equal halves with horizontal arrangement in MCB-I, as shown in Figure 3(a). However, for MCB-II, MWCNTs are placed peripherally to the centrally located SWCNTs, as depicted in Figure 3(b). MCB-III has a similar structure to MCB-I, except for the horizontal arrangement of SWCNTs and MWCNTs, as in Figure 3(c).

3. ESC model and DIL setup

The ESC model of MCB is a combination of the ESC models of bundled SWCNT and bundled MWCNT. Initially, simple ESC models of bundled SWCNT [21,22] and bundled MWCNT [8,23] are derived considering the parasitic elements like resistance, capacitance and inductance. Later, these two equivalent circuit models are combined to build up the final ESC model of the proposed MCB.

The ESC model of bundled CNTs primarily depends on the multi-conductor transmission line theory. The general ESC circuit model of a multiconductor nanoline is sketched in Figure 4, in which the effective

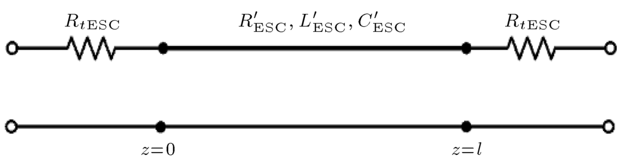


Figure 4. ESC of an SWCNT bundle or an MWCNT bundle.

$p.u.l.$ inductance and capacitance are as follows [21]:

$$L'_{\mathrm{ESC}} = L'_{k-\mathrm{ESC}} + L'_{e-\mathrm{ESC}}, \tag{4}$$

$$C'_{\mathrm{ESC}} = \left(C'^{-1}_{q-\mathrm{ESC}} + C'^{-1}_{e-\mathrm{ESC}}\right)^{-1}. \tag{5}$$

For bundled SWCNT and MWCNT, the equivalent kinetic inductance, $L'_{k-\mathrm{ESC}}$, originates from the kinetic energy of electrons [8], whereas quantum capacitance, $C'_{q-\mathrm{ESC}}$, represents the finite density of states at the Fermi energy. The effective $p.u.l.$, $L'_{k-\mathrm{ESC}}$ and $C'_{q-\mathrm{ESC}}$, are expressed as Eqs. (6) and (7), respectively in which n_{tot} represents the total number of SWCNTs and MWCNTs in the bundle:

$$L'_{k-\mathrm{ESC}} = \frac{L'_{k0}}{2n_{\mathrm{tot}}},$$

where:

$$L'_{k0} = \frac{h}{2e^2 \nu_F}, \tag{6}$$

$$C'_{q-\mathrm{ESC}} = 2n_{\mathrm{tot}} C'_{q0},$$

where:

$$C'_{q0} = \frac{2e^2}{h\nu_F}, \tag{7}$$

where $\nu_F \approx 8 \times 10^5$ m/s represents the Fermi velocity of CNT and graphene [19], and $L'_{k0} = 16.1$ mH/m and $C'_{q0} = 96.8$ pF/m are the $p.u.l.$ kinetic inductance and quantum capacitance of a spinless single conducting channel, respectively [24]. At both ends, the tube is terminated by lumped resistance, $R_{t-\mathrm{ESC}}$, as [21]:

$$R_{t-\mathrm{ESC}} = \frac{R_0}{2n_{\mathrm{tot}}} + R_{mc}, \tag{8}$$

where $R_0 = 12.9$ kΩ [25] is the intrinsic dc resistance of SWCNT and MWCNT and R_{mc} represent metal-nanotube imperfect contact resistance. Depending upon the fabrication process, the value of contact resistance ranges from a few ohms to hundreds of kilo-ohms.

The effective $p.u.l.$ external capacitance, $C'_{e-\mathrm{ESC}}$, is computed as its electrostatic capacitance circumscribes the bundle using Expression (9). Apart from this, the effective $p.u.l.$ magnetic inductance, $L'_{e-\mathrm{ESC}}$, is the stored energy for a given amount of current flow and can be expressed as (10):

$$C'_{e-\mathrm{ESC}} = \frac{2\pi\varepsilon}{\ln(H/d)}, \tag{9}$$

$$L'_{e-\mathrm{ESC}} = \frac{\mu}{2\pi} \ln\left(\frac{H}{d}\right), \tag{10}$$

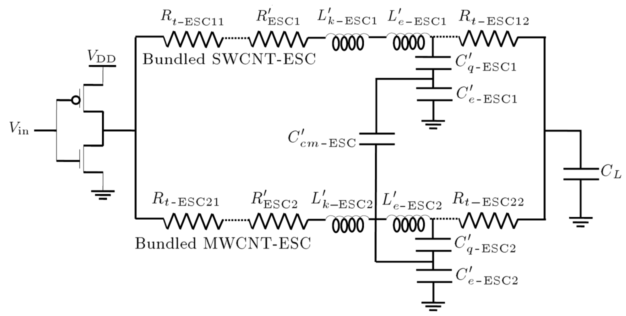


Figure 5. ESC model of mixed CNT bundle interconnects.

where d is nanotube diameter and H is the distance of the bundle from the ground plane. For $d = 1$ nm and $H = 1$ μm, calculated values for $C'_{e-\text{ESC}}$ and $L'_{e-\text{ESC}}$ are 30 aF/μm and 1.4 pH/μm, respectively [24].

On the basis of the ESC transmission line model parameters, the equivalent RLC model of MCB is presented in Figure 5. In the equivalent RLC model, it is assumed that all shells of MWCNTs are parallel and connected at both ends [23]. By considering equal potential across components of each shell, a simplified equivalent RLC model is build up for MWCNTs with different numbers of shells.

Tubes within the same or different bundles experience a coupling effect due to coupling capacitance, $C'_{cm-\text{ESC}}$, as shown in Figure 5. The $C'_{cm-\text{ESC}}$ plays an important role in determining the interconnect performances and can be expressed as [15]:

$$C'_{cm-\text{ESC}} = \frac{\pi \varepsilon l}{\ln\left[\left(\frac{d_{c-c}}{2r}\right) + \left(\sqrt{\left(\frac{d_{c-c}}{2r}\right)^2 + 1}\right)\right]}, \quad (11)$$

where d_{c-c} is the distance between the centres of any two CNTs, l is nanotube length and r is the mean radius of the two CNTs.

Propagation delay and power dissipation are analyzed for different CNT bundles using a Driver-Interconnect-Load (DIL) system, as depicted in Figure 6. A CMOS driver with supply voltage $V_{dd} = 1$ V [19] is used for accurate estimation of delay and power dissipation. The ESC models of bundled SWCNT, bundled MWCNT and MCB represent the interconnect line of the DIL system. The interconnect line is terminated by a load capacitance, $C_L = 10$ aF [19]. Propagation delay and power dissipation are observed at different global interconnect lengths ranging from 100 μm to 1000 μm.

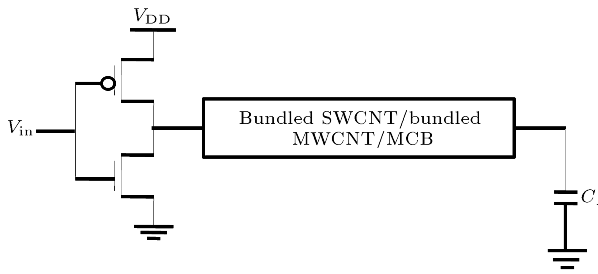


Figure 6. Driver Interconnect Load (DIL) system.

The quantitative values of interconnect parasitics for different bundled CNTs are placed in Table 1, which represents the parasitic values of the ESC model in Figure 5. These parasitic values are obtained using the spatial arrangements of SWCNTs and MWCNTs in a bundle, as shown in Figures 2 and 3.

4. Delay and power analysis

Using the above mentioned DIL setup and ESC models, propagation delay and power dissipation are observed. For different interconnect lengths, Figure 7 through Figure 11 represents the propagation delay and power dissipation of bundled SWCNT, bundled MWCNT, MCB-I, MCB-II and MCB-III, respectively. It is observed that the power and delay performance are considerably reduced using MCBs in comparison to the bundled SWCNT and bundled MWCNT. This reduction is more significant for MCB-III in comparison to the MCB-I and MCB-II due to their structural differences. The percentage reductions in delay and

Table 1. Equivalent parasitics associated with different bundled CNTs.

Interconnect parasitics	**Bundled SWCNT (SWCNT Num=6438)**	**Bundled MWCNT (MWCNT Num=551)**	**MCB-I (SWCNT Num=3193; MWCNT Num=276)**	**MCB-II (SWCNT Num=3188; MWCNT Num= 285)**	**MCB-III (SWCNT Num=5251; MWCNT Num=102)**
$R_{t-\text{ESC}}$ (Ω)	2.06	2.05	2.05	2.04	2.01
R'_{ESC} (Ω/μm)	2.01	1.27	1.26	1.21	1.18
$L'_{k-\text{ESC}}$ (pH/μm)	1.89	1.87	1.87	1.84	1.81
$L'_{e-\text{ESC}}$ (fH/μm)	0.48	0.21	0.29	0.21	0.21
$C'_{q-\text{ESC}}$ (fF/μm)	886.66	831.12	855.60	841.89	831.12
$C'_{e-\text{ESC}}$ (fF/μm)	1.12	0.42	0.78	0.42	0.42

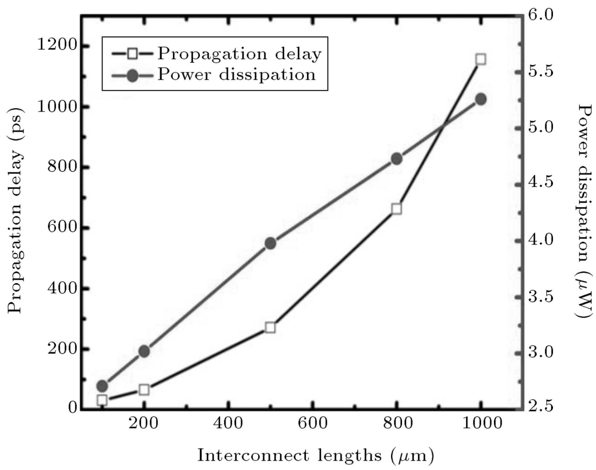


Figure 7. Propagation delay and power dissipation of bundled SWCNT for different interconnect lengths.

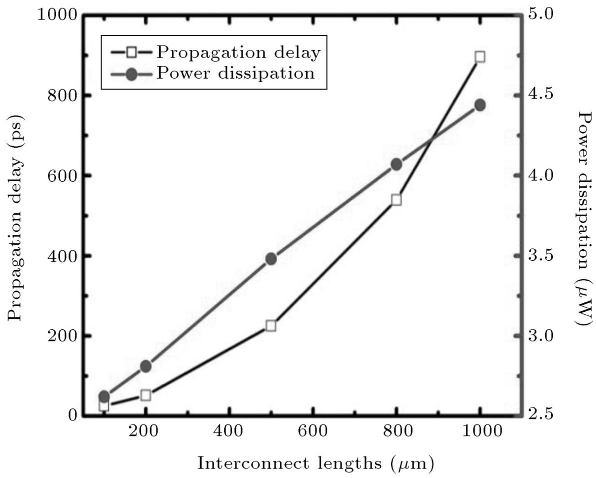


Figure 8. Propagation delay and power dissipation of bundled MWCNT for different interconnect lengths.

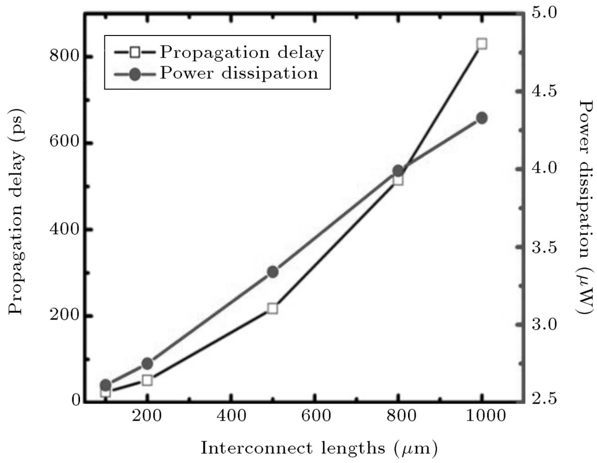


Figure 9. Propagation delay and power dissipation of MCB-I for different interconnect lengths.

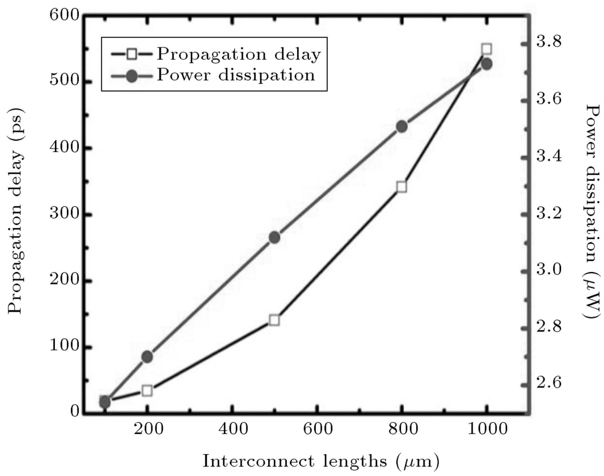


Figure 10. Propagation delay and power dissipation of MCB-II for different interconnect lengths.

power dissipation for MCB-III compared to other bundle arrangements are summarized in Tables 2 and 3, respectively.

Propagation delay and power dissipation are primarily influenced by the parasitic capacitance, apart from resistance and inductance too. The parasitic capacitances associated with each CNT are categorized into: (1) electrostatic and (2) quantum. Between these two, electrostatic capacitance mostly influences the delay and power performance. The quantitative values of these parasitics primarily depend on the geometry and number of SWCNTs and MWCNTs in a bundle. It is observed that for a higher number of SWCNTs and/or MWCNTs in a bundle, the equivalent resistive and inductive parasitic reduces, whereas capacitive parasitic increases, as presented in

Table 2. Percentage reduction in propagation delay for MCB-III as compared to other bundled CNTs.

Interconnect lengths (μm)	**Percentage reduction in delay for MCB-III with respect to**			
	Bundled SWCNT	**Bundled MWCNT**	**MCB-I**	**MCB-II**
100	43.72	29.35	27.05	6.69
200	50.29	36.27	35.69	5.69
500	53.36	43.75	41.78	10.16
800	58.32	48.80	46.39	19.23
1000	62.70	51.86	48.04	21.53

Table 3. Percentage reduction in power dissipation for MCB-III as compared to other bundled CNTs.

Interconnect lengths (μm)	**Percentage reduction in delay for MCB-III with respect to**			
	Bundled SWCNT	**Bundled MWCNT**	**MCB-I**	**MCB-II**
100	7.01	3.82	3.45	0.79
200	12.58	6.05	4.00	2.22
500	24.12	13.22	9.58	3.21
800	29.18	17.69	16.04	4.59
1000	32.51	20.05	18.01	4.83

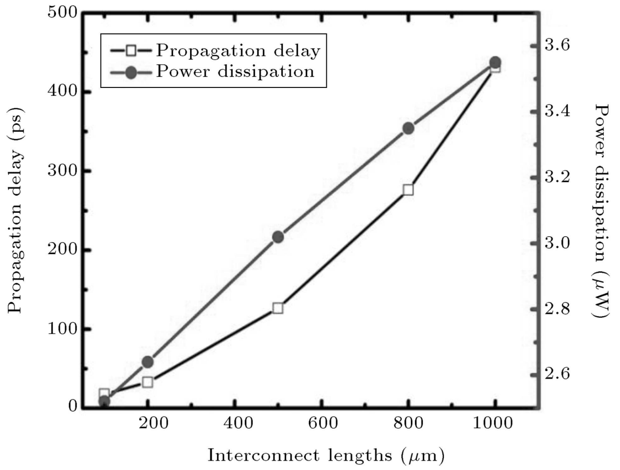


Figure 11. Propagation delay and power dissipation of MCB-III for different interconnect lengths.

Table 1. Furthermore, the number of SWCNTs and/or MWCNTs facing the ground plane decides the value of $C'_{e-\mathrm{ESC}}$ which essentially affects the performance. Lower parasitics associated with MCB-III result in a better performance in comparison to MCB-I, MCB-II, bundled SWCNT and bundled MWCNT.

5. Conclusion

Novel structures of MCBs have been proposed using the spatial arrangements of SWCNTs and MWCNTs in a bundle. Using the hierarchical approach, an ESC model of MCBs has been built up. Propagation delay and power performances have been compared for different bundled CNTs at global interconnect lengths using a DIL system. Based on the simulated results, it has been observed that the performance are significantly improved for the MCB-III spatial arrangement containing equal halves of horizontally oriented SWCNTs and MWCNTs. Using the novel MCB-III, the delay and power performance are reduced by 48.1% and 20.9%, respectively, in comparison to the bundled SWCNT interconnects.

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Biographies

Manoj Kumar Majumder received his BTech and MTech degrees in 2007 and 2009, respectively, and is currently working towards his PhD degree in Microelectronics and VLSI groups at the Indian Institute of Technology, Roorkee, India. From 2009 to 2010, he was associated with academic activities in Electronics and Communication Engineering Department in Durgapur Institute of Advanced Technology and Management (DIATM), West Bengal, India. His research interests include carbon nanotube based VLSI interconnects and circuit modeling. He has published/presented more than 35 research papers in various international journals and at conferences. He has obtained Graduate Aptitude Test Engineering (GATE) fellowship in 2007 and MHRD fellowship in 2010.

Brajesh Kumar Kaushik received his PhD degree, in 2007, from the Indian Institute of Technology, Roorkee, India, where he is currently Assistant Professor in the VLSI group. He has published/presented more than 150 research papers in various international journals and at conferences, and has received numerous awards in his field. In 1998, he joined as a lecturer at G.B.Pant Engineering College Pauri Garhwal, where he served as Assistant Professor till 2009. His current research interests include electronic simulation, and low power VLSI design.

Sanjeev Kumar Manhas received his PhD degree in 2003 from De Montfort University, Leicester, UK, and is currently Assistant Professor at the Indian Institute of Technology, Roorkee, India.

He has received numerous academic awards, and his research interests include silicon nanowire based circuit design, parasitic evaluation and fabrication technologies, MOSFET modeling and reliability, DRAM leakage mechanisms and OTFTs. He has both academic and industrial experience. such as Microelectronics best paper award in 2002, graduate merit award in 1991 and Indian National Research Scholarship award in 1993.