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Simulation of a carbon nanotube field effect transistor with two different gate insulators

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Abstract. In this paper, a novel structure for MOSFET like CNTFETs (MOSCNTs) is proposed, combining the advantages of both high and low dielectrics to improve output characteristics. In this structure, the gate dielectric at the drain side is selected from a material with low dielectric constant to form smaller capacitances, while a material with high dielectric constant is selected at the source side to improve on current and reduce leakage current. The new structure is simulated based on the Schrödinger-Poisson formulation. Obtained results show that the proposed configuration has lower off and higher on current in comparison with low-k MOSCNTs. Also, using a two-dimensional model, a wide range of new structure performance parameters is studied. It is found that transconductance, intrinsic cut-off frequency and quantum capacitance parameters are improved compared to MOSCNTs with low dielectric constant. It is clear that the proposed structure can provide DIBL and subthreshold swing near its theoretical limit, while it also profits from smaller capacitances in gate, drain and source in comparison with high-k MOSCNTs.

1. Introduction

Carbon nanotubes (CNT), with long and thin cylinders of carbon, were discovered in 1991 by Iijima [1]. A CNT is a sheet of graphite, rolled-up as a tube, which has a diameter typically in the nanometer range [2]. Nanotubes have high thermal conductivity ($\sim$ 2000 W/m/K, whereas copper has 400 W/m/K) and are able to carry electrical current at higher densities than other metals and semiconductors (maximum current density $\sim$ 1013 A/m^2) [3]. Also, their mobility is considerably larger than silicon (about 105 cm^2/V.S). These properties promote CNTs as a candidate for nanometer technologies. CNTs can be semiconducting or metallic according to the chiral vector. In semiconducting CNTs, the bandgap decreases when tube diameter increases, therefore, tubes of few nanometers in diameter can be used as a channel in Field Effect Transistors (FETs) [2].

In miniaturized transistors, whose scales are below 2 nm, leakage currents increase drastically due to tunneling. This will increase power consumption and reduce device reliability. Replacing the gate dielectric with a material with high dielectric constant will increase gate capacitance without the existence of leakage current. The low dielectric constant of SiO_2 (at 3.9) limits its use in transistors as a gate dielectric, since the gate tunneling current increases significantly [4]. However, replacing the gate dielectric with a material with low dielectric constant will reduce parasitic capacitances; make faster switching speeds and lower heat dissipation [5].

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In this paper, a new structure for MOS-CNTFET is proposed to improve the performance of MOSCNTs, combining the advantages of both high and low dielectrics in the gate (Two Different Insulator-CNTFET, TDI-CNTFET). Schrödinger-Poisson equations were solved numerically and the obtained results are compared with conventional structures. The simulation results show that the proposed transistor has higher on and lower off current, with respect to MOSCNTs with a low dielectric constant. Continuing, we use a two-dimensional model for modeling MOSCNTs. It is an attempt to extract important characteristics from MOSCNTs, in terms of transconductance, quantum capacitance, intrinsic cut-off frequency, DIBL, subthreshold swing, and created capacitances with gate, source and drain.

Section 2 presents the implementation method for the simulation of MOSCNTs and this method is used for simulation of the new structure in Section 3. In Section 4, a two-dimensional model is introduced in detail and is used to extract important characteristics from MOSCNTs, such as transconductance, quantum capacitance, intrinsic cut-off frequency, DIBL, subthreshold swing, and created capacitances with gate, source and drain. The modeling results are shown in Section 5. Finally, the paper ends with a conclusion.

2. Implementation method

CNTFETs are devices in which an intrinsic CNT is sandwiched between n^+ doped nanotubes as the source and drain (Figure 1). Simulation of CNTFET devices involves a self-consistent solution between the electrostatic potential and the charge distribution inside the devices [3]. Charge density inside the device can be obtained by solving the Schrödinger equation with NEGF formalism. The Poisson equation provides the electrostatic potential using a given charge density. Using the calculated potential via the Poisson equation, the Schrödinger equation can be solved in order to obtain the new value of the carrier density. This procedure is carried out in a loop, until convergence occurs [6].

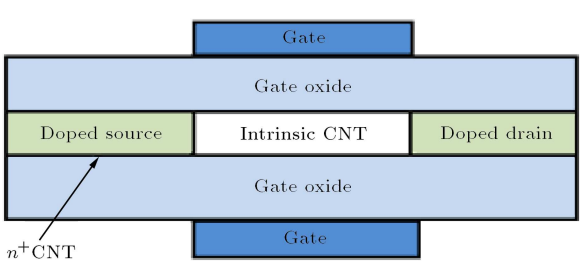

Figure 1. A coaxial CNTFET with heavily-doped, semi-infinite nanotubes as the source/drain contacts. The channel is intrinsic and the gate length equals the channel length.

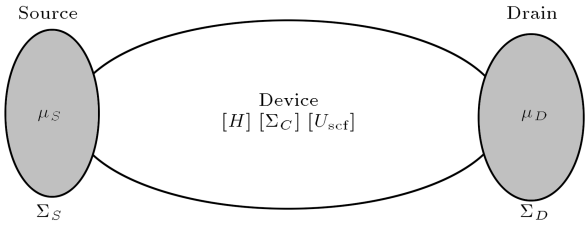

Figure 2. A generic transistor with coupled source/drain contact.

Within the NEGF formalism, the device is represented by a Hamiltonian, H, which is coupled to two infinite reservoirs of source (S) and drain (D). S/D are described by their Fermi levels, μ_S and μ_D, and are determined by applied voltage biases. Self-energy matrices, Σ_S and Σ_D, characterize the coupling between the device and S/D contacts, respectively. The matrix of self-energy (Σ_C) is used to describe the incoherent carrier transport (due to scattering) inside the device, Figure 2 [3].

Once H, Σ_S, Σ_D, μ_S, μ_D and Σ_C are determined, the retarded Green's function can be obtained from Eq. (1) [3]:

$$G(E) = [EI - H_i - \Sigma_s - \Sigma_d]^{-1}, \tag{1}$$

where 'H_i' is the Hamiltonian of the ith subband and I is the identity matrix.

The Local Density Of States (LDOS) due to source and drain can be written as [6]:

$$D_{s(d)} = G\Gamma_{s(d)}G^+, \tag{2}$$

where $\Gamma_{s(d)}$ is the energy level broadening due to the source (drain) contact:

$$\Gamma_{s(d)} = i\left(\Sigma_{s(d)} - \Sigma^+_{s(d)}\right), \qquad i \text{ is imaginary unit.} \tag{3}$$

The charge density is computed by integrating the LDOS over energy. The contributed charge, due to the accumulation of electrons, can be calculated as [3,6]:

$$Q_e = (-e)\int_{E_i}^{\infty}(D_s f(E - E_{fs}) + D_d f(E - E_{fd}))\, dE, \tag{4}$$

where $E_{fs(d)}$ is the Fermi energy in the source (drain) and E_i is the charge neutrality energy level. A similar expression holds for holes.

In order to calculate the electrostatic potential, the Poisson equation should be solved within the structure:

$$\nabla^2 V(z, r) = -\frac{\rho}{\varepsilon}, \tag{5}$$

where ρ is the charge density on the surface of the CNT and ε is the dielectric constant.

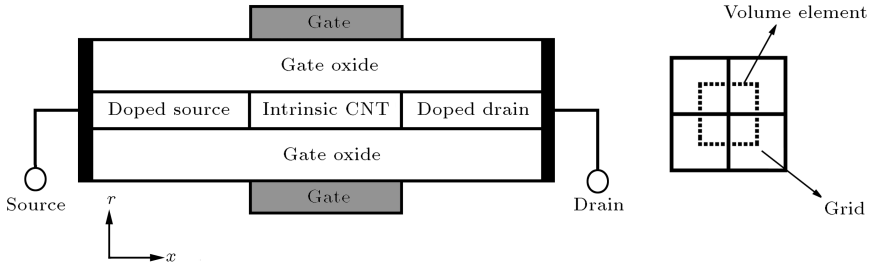

Figure 3. (a) A MOSCNT with a conventional structure. (b) A volume element near a grid point for discretizing the continuous form of the Poisson equation.

For the coaxially gated carbon nanotube transistor, the Poisson equation is solved in cylindrical coordinates. Since the potential and charge density are constant around the nanotube, the Poisson equation will be changed to a 2-D problem along the tube (x-direction) and the radial direction (r-direction) as shown in Figure 3(a) [7].

The continuous form of the Poisson equation is discretizsed by applying a second order accurate central difference scheme. A regular grid was used for the whole domain to create volumetric elements (see Figure 3(b)). Then, the integral is carried out over volume to solve the equation numerically. The discretized equation for an element at the grid point (x_i, r_j) in air can be obtained as [7]:

$$\varepsilon_0 \left(\frac{r_{j-1}+r_j}{2}\Delta x \frac{V_m^{i,j-1}-V_m^{i,j}}{\Delta r} + \frac{r_{j+1}+r_j}{2}\Delta x \frac{V_m^{i,j+1}-V_m^{i,j}}{\Delta r} + r_j \Delta r \frac{V_m^{i+1,j}-V_m^{i,j}}{\Delta x} + r_j \Delta r \frac{V_m^{i-1,j}-V_m^{i,j}}{\Delta x} \right) = e r_j \Delta x (N_D - n_{\text{net}}), \quad (6)$$

where N_D and n_{net} are impurity density and electron density, respectively.

For grid points in the gate insulator, the gate insulator dielectric constant replaces ε_0 in Eq. (6) [7].

After self-consistent computation, the current can be calculated according to Eq. (7) [6]:

$$I = (4e/h) \int T(E)(f_s(E) - f_d(E))dE, \quad (7)$$

where T is transmission coefficient and is calculated as:

$$T(E) = \text{trace}(\Gamma_s G \Gamma_d G^+). \quad (8)$$

3. Simulation results

A (17, 0) MOSCNT with gate oxide thickness of 2 nm, based on the structure of Figure 3(a), is considered as a case study. The energy band diagrams for a MOSCNT with 3.9 and 16 dielectric constants in $V_{DS} = 0.6$ V and $V_{GS} = 0.6$ V are shown in Figure 4(a) and (b), respectively. The color scaled plots indicate the number of electrons per unit energy dn/dE versus position along the surface of the carbon nanotube, considering only the first subband.

It is obvious from the figures that with increasing dielectric constant, the gate tunneling currents reduce and thermal emission current increases. Increasing thermal emission current leads to higher

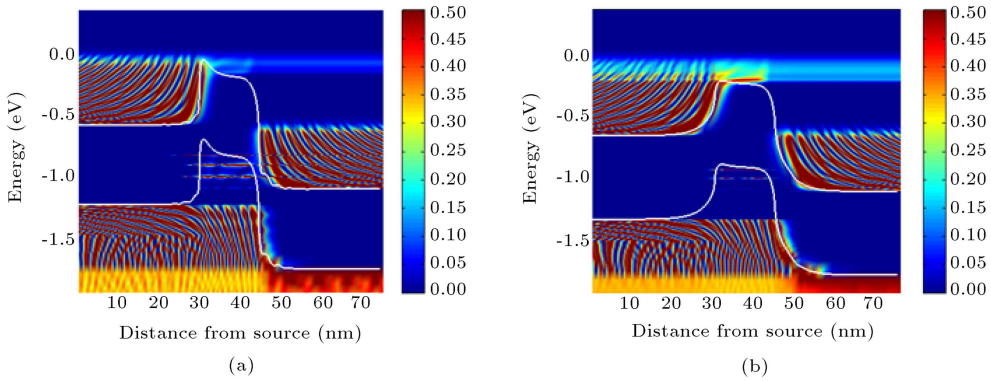

Figure 4. (a) Energy band diagrams for a conventional MOSCNT with $K = 3.9$ for the first subband in $V_{DS} = 0.6$ V and $V_{GS} = 0.6$ V. (b) Energy band diagrams for a conventional MOSCNT with $K = 16$ for the first subband in $V_{DS} = 0.6$ V and $V_{GS} = 0.6$ V.

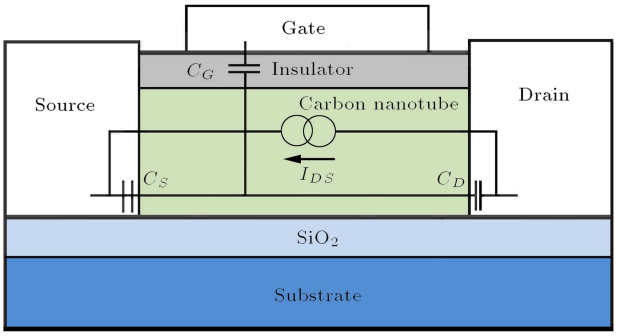

Figure 5. Capacitance model for MOSCNTs. C_G, C_D and C_S are the effect of gate, drain and source potential on the gate oxide, respectively.

on currents, and reducing tunneling currents leads to lower off currents, so I_{on}/I_{off} ratio will be increased.

Gates with high dielectric constant decrease leakage current, but on the other hand, form larger capacitances. This increase is due to the greater effectiveness of the gate potential on the channel. The capacitance model for MOSCNTs is shown in Figure 5. It consists of three capacitors, which represent the effect of gate, drain and source potential on the channel.

According to the mentioned advantages associated with high and low dielectric constants, a novel MOS-CNTFET is proposed to increase its performance. Keeping this in mind, the gate length of the transistor in Figure 3(a) is divided into two equal sections. In order to decrease the capacitance on the channel located near the drain, the gate dielectric at the drain side is selected from a material with low dielectric constant. Contrarily, the gate dielectric at the source side is selected from a material with high dielectric constant (TDI-CNTFET) to improve on current and reduce leakage current, Figure 6.

This new structure is simulated based on Schrödinger-Poisson formalism. In this case, the dielectric constant for grid points at the drain side is less than at the source side. For middle grid points, the lower dielectric constant is used for volume surfaces at the drain side, and the higher dielectric constant is used for volume surfaces at the source side. The discretized Poisson equation for an element at the middle grid point (x_i, r_j) is obtained as:

$$\begin{aligned}
&\frac{r_{j+1}+r_j}{2}\varepsilon_2 \\
&\left(\Delta x\frac{\frac{1}{2}\left(\frac{3}{4}V_m^{i,j+1}+\frac{1}{4}V_m^{i+1,j+1}-\frac{3}{4}V_m^{i,j}-\frac{1}{4}V_m^{i+1,j}\right)}{\Delta r}\right) \\
&+\frac{r_{j-1}+r_j}{2}\varepsilon_2 \\
&\times\left(\Delta x\frac{\frac{1}{2}\left(\frac{3}{4}V_m^{i,j-1}+\frac{1}{4}V_m^{i+1,j-1}-\frac{3}{4}V_m^{i,j}-\frac{1}{4}V_m^{i+1,j}\right)}{\Delta r}\right) \\
&+\frac{r_{j+1}+r_j}{2}\varepsilon_1 \\
&\left(\Delta x\frac{\frac{1}{2}\left(\frac{3}{4}V_m^{i,j+1}+\frac{1}{4}V_m^{i-1,j+1}-\frac{3}{4}V_m^{i,j}-\frac{1}{4}V_m^{i-1,j}\right)}{\Delta r}\right) \\
&+\frac{r_{j-1}+r_j}{2}\varepsilon_1 \\
&\left(\Delta x\frac{\frac{1}{2}\left(\frac{3}{4}V_m^{i,j-1}+\frac{1}{4}V_m^{i-1,j-1}-\frac{3}{4}V_m^{i,j}-\frac{1}{4}V_m^{i-1,j}\right)}{\Delta r}\right) \\
&+r_j\Delta r\varepsilon_2\frac{V_m^{i+1,j}-V_m^{i,j}}{\Delta x}+r_j\varepsilon_1\Delta r\frac{V_m^{i-1,j}-V_m^{i,j}}{\Delta x} \\
&=er_j\Delta x(N_D-n_{net}). \qquad (9)
\end{aligned}$$

For every grid point, calculated potential is given in the Schrödinger equation until the new carrier density is obtained. This step continues until convergence occurs.

As can be seen, the energy band diagram for a TDI-CNTFET is shown in Figure 7. A comparison between Figures 4 and 7 shows that the tunneling and thermal emission currents of a TDI-CNTFET increase in comparison with a MOSCNT with low dielectric constant, where thermal emission current is the dominant mechanism in electron transport. Also, it can be concluded that at negative gate voltages, the current of the TDI-CNTFET is much lower than

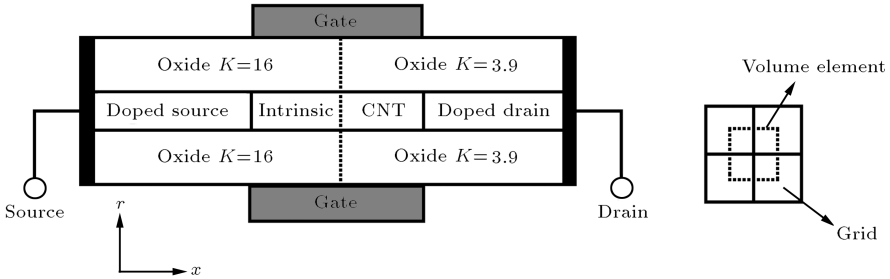

Figure 6. A MOSCNT with new structure (TDI-CNTFET).

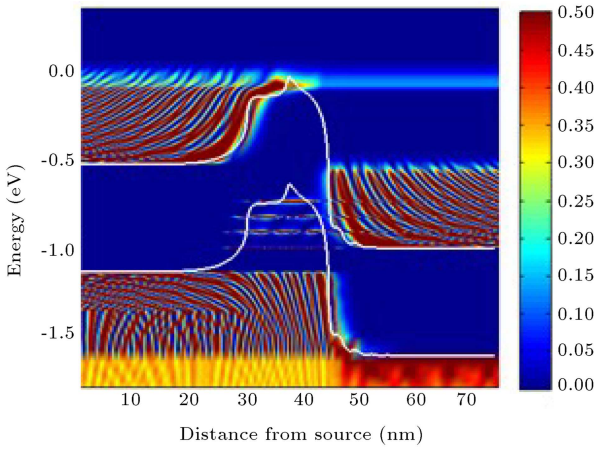

Figure 7. Energy band diagrams for a TDI-CNTFET for the first subband in $V_{DS} = 0.6$ V and $V_{GS} = 0.6$ V. The color scaled plots indicate the number of electrons per unit energy dn/dE vs. position along the surface of the carbon nanotube.

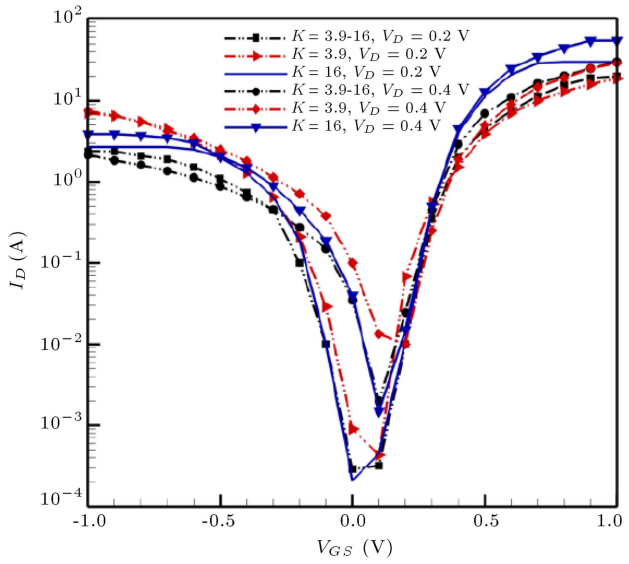

Figure 8. Simulated current I_{DS} versus V_{GS} for conventional MOSCNTs with dielectric constants $K = 3.9$ and 16 and a TDI-CNTFET at different gate voltages.

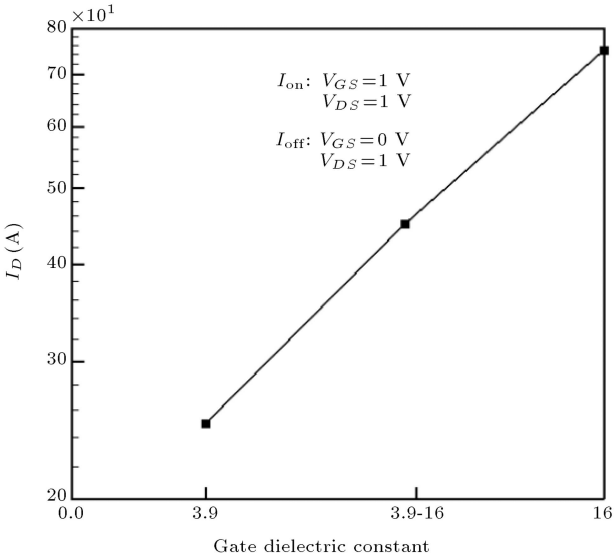

Figure 9. I_{on}/I_{off} ratio for a TDI-CNTFET and conventional MOSCNTs with $K = 16$ and 25.

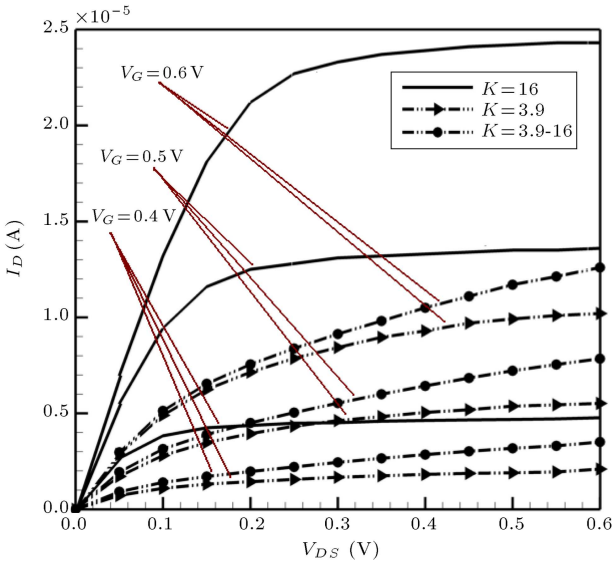

Figure 10. Simulated current I_{DS} versus V_{DS} for conventional MOSCNTs with dielectric constant $K = 3.9$ and 16 and a TDI-CNTFET at different gate voltages.

that of the conventional MOSCNTs, which makes TDI-CNTFETs suitable for logic applications.

Current-gate voltage characteristics for both new and conventional structures are depicted in Figure 8. As can be seen, TDI-CNTFET has a *higher on* current and a *lower off* current compared to MOSCNT with a low dielectric constant. The reason is due to greater thermal emission current because of the superior control of the gate potential on the channel near the source, which helps reduce the off-state current and increase the on-state current. Figure 9 illustrates I_{on}/I_{off} ratio for both new and conventional structures. Note that I_{on} is measured at $V_{GS} = 1$ V and I_{off} at $V_{GS} = 0$ V.

Output characteristics for the different gate voltages are plotted in Figure 10, which shows that TDI-CNTFET has a higher current delivering capability, due to an increase in thermal emission current, in comparison with a CNTFET with low dielectric constant.

4. A two-dimensional model

As mentioned in Section 3, simulation results show the superior characteristics of TDI-CNTFET. In this section, a two-dimensional (2-D) model is used to study other characteristics of our proposed CNTFET structure in terms of transconductance, quantum capacitance, intrinsic cut-off frequency, DIBL, subthreshold

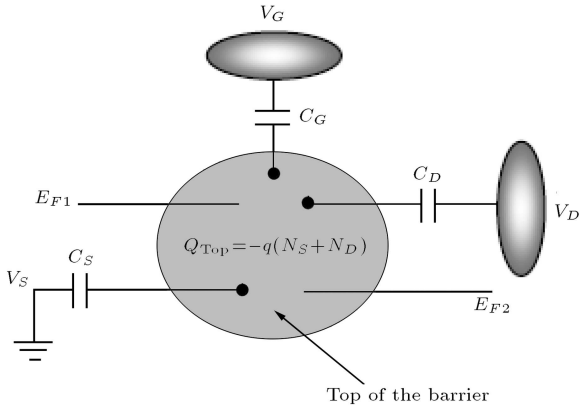

Figure 11. Two-dimensional circuit model for transistors. The potential at the top of the barrier, $U_{\rm scf}$, is controlled by the gate, drain and source potentials. The mobile charge at the top of the barrier is determined by $U_{\rm scf}$ and locations of the two Fermi levels of E_{F1} and E_{F2}.

swing, and created capacitances with gate, source and drain.

A mobile charge is induced in the nanotube when an electric field is applied between the drain and the source of a CNT transistor, as illustrated in Figure 11 [8]. In the shaded region in Figure 11, the amount of induced mobile charge at the top of the barrier is [9]:

$$Q_{\rm TOP} = -q(N_S + N_D), \tag{10}$$

where N_S and N_D are the density of positive velocity states filled by the source and the density of negative velocity states filled by the drain, respectively. When the terminal biases are zero, the equilibrium electron density at the top of the barrier is N_0. These densities are determined by the Fermi-Dirac probability distribution, as follows [8,9]:

$$N_0 = \int_{-\infty}^{+\infty} D(E) f(E - E_F) dE, \tag{11}$$

$$N_S = \frac{1}{2} \int_{-\infty}^{+\infty} D(E - U_{\rm scf}) f(E - E_{F1}) dE, \tag{12a}$$

$$N_D = \frac{1}{2} \int_{-\infty}^{+\infty} D(E - U_{\rm scf}) f(E - E_{F2}) dE, \tag{12b}$$

where $D(E)$ is the density of states at the top of the barrier, $U_{\rm scf}$ is the self-consistent voltage at the top of the barrier, E_F is the Fermi level and f is the equilibrium Fermi function. $E_{F1} = E_F$ and $E_{F2} = E_{F-q}V_{DS}$ are source and drain Fermi levels, respectively.

Defining the density of states $D(E)$ and location of source-drain Fermi levels, the value of the self consistent potential is needed to evaluate electron density at the top of the barrier, $N = N_S + N_D$. The self-consistent voltage, $U_{\rm scf}$, can be calculated in two steps, as below [5,9]:

i) Ignoring the presence of the mobile charge in the channel and calculating the Laplace potential at the top of the barrier due to terminal biases leads to:

$$U_L = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S), \tag{13a}$$

where α_G, α_D and α_S are used to control the Laplace solution and can be obtained as:

$$\alpha_G = \frac{C_G}{C_\Sigma}, \qquad \alpha_D = \frac{C_D}{C_\Sigma}, \qquad \alpha_S = \frac{C_S}{C_\Sigma}, \tag{13b}$$

where C_Σ is the parallel combination of the three capacitors in Figure 10.

ii) Grounding the three terminals and computing the potential due to the change of mobile charge at the top of the barrier, $\Delta N = (N_S + N_D) - N_0$, from:

$$U_P = \frac{q^2}{C_\Sigma} \Delta N. \tag{14}$$

The complete solution is obtained by adding the two contributions:

$$\begin{aligned} U_{\rm scf} &= U_L + U_P \\ &= -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) + U_P. \end{aligned} \tag{15}$$

Eqs. (12) and (15) represent two coupled nonlinear equations for the two unknowns, N and $U_{\rm scf}$. Then, the drain current can be obtained from Eq. (16a):

$$\begin{aligned} I_D = \int_{-\infty}^{+\infty} J(E - U_{\rm scf}) [f(E - E_{F1}) \\ - f(E - E_{F2})] dE, \end{aligned} \tag{16a}$$

where $J(E\_U_{\rm scf})$ is the "current-density-of-states", which is expressed as:

$$\begin{aligned} J(E - U_{\rm scf}) = \frac{1}{2} q \left(\frac{2}{\pi} \sqrt{\frac{2(E - U_{\rm scf})}{m^*}} \right) \\ D(E - U_{\rm scf}). \end{aligned} \tag{16b}$$

5. Modeling results

To illustrate the use of the two-dimensional model, we match the output characteristics of a CNTFET with both design methods (two-dimensional model and simulation) by adjusting α_G, α_D and α_S parameters to control the Laplace solution and by setting the

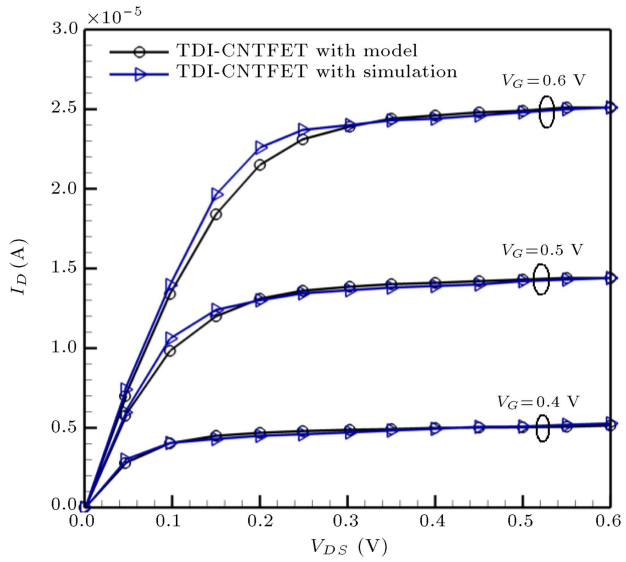

Figure 12. The matched drain current characteristics versus drain voltage for different gate voltages, for both design methods "two-dimensional model" and "simulation".

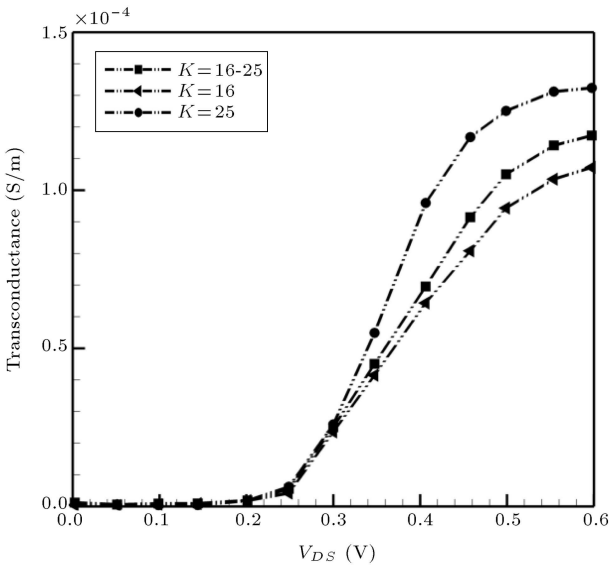

Figure 13. Transconductance versus the gate voltage for a TDI-CNTFET and MOSCNTs with $K = 16$ and 25 at $V_{DS} = 0.6$ V.

Fermi level, E_F, for the correct threshold voltage, for dielectric constants of 25 and 16, where the channel is a (17, 0) nanotube. Figure 12 presents the same operation utilized for matching the output characteristics of a TDI-CNTFET with a dielectric constant of 16 at the drain side and 25 at the source side. By this matching, other characteristics of CNTFETs can be extracted in terms of transconductance, quantum capacitance, intrinsic cut-off frequency, DIBL, subthreshold swing, and created capacitances with gate, source and drain. The results are in agreement with [3,6].

Table 1 shows the calculated capacitances for a TDI-CNTFET and MOSCNTs with 16 and 25 dielectric constants. As can be seen, gate, drain and source capacitances are smaller for low dielectric constants due to the weaker influence of the gate potential on the channel. For our proposed structure, which has a dielectric constant of 16 at the drain side and 25 at the source side, it is clear that the gate, drain and source capacitances are smaller than high-k MOSCNTs and bigger than low-k MOSCNTs, due to the stronger influence of gate potential on the channel near the source.

Transconductance, g_m, is the ratio of the current change at the output port to the voltage change at the input port. For a high transconductance, every small change in gate voltage causes a big change in drain current, which shows transistor sensitivity. In Figure 13, the transconductance (g_m) is extracted from the slope of $I_{DS} - V_{GS}$ at $V_{DS} = 0.6$ V. For our proposed structure, transconductance increases, due to the greater controllability of the gate on the channel near the source, in comparison with a MOSCNT with low dielectric constant. On the other hand, it decreases, due to the weaker controllability of the gate on the channel at the drain side, when compared with a MOSCNT with high dielectric constant.

Obtaining transconductance, we can extract another important parameter from the CNT field effect transistors, called the intrinsic cut-off frequency, f_T. The intrinsic cut-off frequency is an important parameter to determine the high frequency performance of the transistors [10]. The value of f_T can be obtained from [10]:

$$f_T = \frac{g_m}{2\pi C_G}, \tag{17}$$

where g_m is transconductance and C_G is gate capaci-

Table 1. Gate, drain and source capacitances for a TDI-CNTFET and MOSCNTs with $K = 16$ and 25.

		Capacitance		
		C_D	C_S	C_G
Dielectric	16	0.2895×10^{-10}	0.7031×10^{-10}	7.2789×10^{-10}
	16-25	0.3385×10^{-10}	0.8120×10^{-10}	7.3133×10^{-10}
	25	0.6674×10^{-10}	1.3086×10^{-10}	11.373×10^{-10}

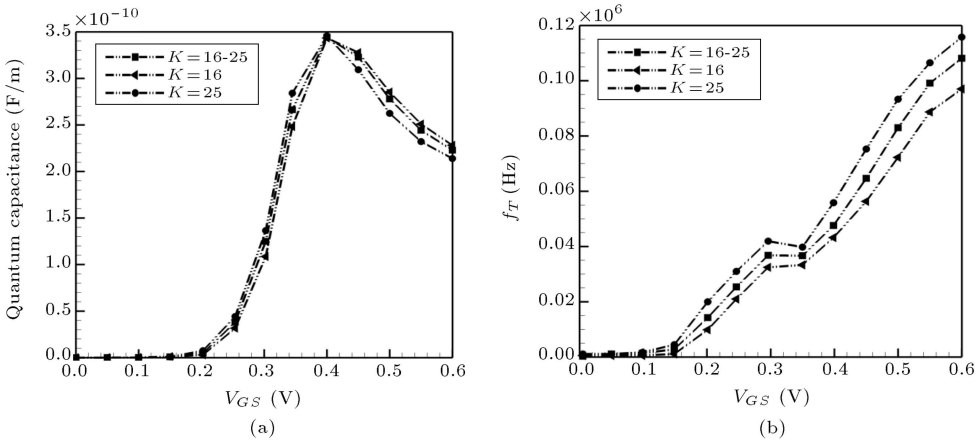

Figure 14. (a) Quantum capacitance vs the gate voltage for a TDI-CNTFET and MOSCNTs with $K = 16$ and 25 at $V_{DS} = 0.6$ V. (b) Intrinsic cut-off frequency vs the gate voltage for a TDI-CNTFET and MOSCNTs with $K = 16$ and 25 at $V_{DS} = 0.6$ V.

tance. The gate capacitance can be derived from [8]:

$$C_G^{-1} = C_{ox}^{-1} + C_Q^{-1}, \tag{18}$$

where C_{ox} is the electrostatic gate capacitance, due to gate dielectrics, and C_Q is the quantum capacitance of the nanotube, given by [9]:

$$C_Q = \frac{d(qN)}{d(-U_{\text{scf}}/q)}. \tag{19}$$

Quantum capacitance as a function of gate voltage at $V_{DS} = 0.6$ V is shown in Figure 14(a). As can be seen, until $V_{GS} = 0.4$ V, the quantum capacitance increases and then decreases. Eq. (19) shows that quantum capacitance is related to electron density, directly. Generally, electron density in the channel can be calculated as follows:

$$Q_e = (-e)\int_{E_i}^{\infty}(D_s f(E - E_{fs}) + D_d f(E - E_{fd}))dE, \tag{20}$$

where $D_{S(D)}$ is states density and is proportional to $E^{-1/2}$.

When gate-source voltage increases, barrier height between the source and the drain lessens, and more electrons can tunnel from one to the other. Thus, electron density in the channel increases. This process continues until the Fermi level reaches the level of the channel, which is, in this condition, $V_{GS} = 0.4$ V. With further increase of gate voltage, electron energy increases and leads to a decrease in $D(E)$, which causes a reduction in the value of the quantum capacitor.

Figure 14(b) shows the calculated f_T. The slope of f_T arises from transconductance and quantum capacitance slopes. f_T increases for high dielectric constant, due to a higher ratio of tranconductance to gate capacitance.

Table 2. Subthreshold swing for a TDI-CNTFET and MOSCNTs with $K = 16$ and 25.

Dielectric	16	16-25	25
Subthreshold swing	67.70754	65.3307	64.7617

Table 3. DIBL effect for a TDI-CNTFET and MOSCNTs with $K = 16$ and 25.

Dielectric	16	16-25	25
DIBL	48.1354	40.9631	30.8139

The subthreshold swing is a key parameter in transistor miniaturization. For FETs, a small subthreshold swing (S) is desired for low threshold voltage and low-power operation [5]. Subthreshold swing value at room temperature (S) is:

$$S = (k_B T/e)\ln(10) \approx 60 \text{ mV/decade}.$$

Table 2 shows that the subthreshold swing decreases and becomes close to its theoretical limit with increasing k, due to the fact that high gate insulators reduce leakage current and produce low subthreshold swing.

At a certain gate voltage, if a high drain voltage is applied, the barrier height can decrease and lead to an increased drain current. Thus, the drain current is controlled, not only by the gate voltage, but also by the drain voltage. This effect is called Drain-Induced Barrier Lowering (DIBL). For FETs, this parasitic effect by reducing the threshold voltage is defined [11]. In a high dielectric constant, DIBL effect decreases, due to the greater control of the gate effect on the channel, as can be seen in Table 3.

6. Conclusion

A novel MOS-CNTFET (TDI-CNTFET) is presented, combining the advantages of both high and low dielectrics. The high dielectric constants will increase

gate capacitance without the existence of leakage current. Replacing the silicon dioxide with a material with high dielectric constant reduces the tunneling and parasitic capacitances. In order to achieve a more efficient transistor, the gate length is divided into two equal sections. To decrease the capacitance on the channel near the drain, the gate dielectric at the drain side is selected from a material with low dielectric constant, and to improve on current and reduce leakage current, the gate dielectric at the source side is selected from a material with high dielectric constant. The obtained results, based on the Schrödinger-Poisson formulation, show that the new structure has superior characteristics, such as higher on current and lower off current, compared to a MOSCNT with low dielectric constant. Also, we used a two-dimensional model for modeling the MOSCNTs. Comparison between conventional MOSCNTs and TDI-CNTFET, in terms of different associated parameters, reveals that the new structure improves transconductance, intrinsic cut-off frequency and quantum capacitance parameters, compared to MOSCNTs with low dielectric constant. It was also clear that the proposed structure produces DIBL and subthreshold swings near to its theoretical limit, and has smaller gate, drain and source capacitances in comparison to MOSCNTs with high dielectric constant.

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