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Analysis of parametric oscillations in high power amplifiers

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Abstract. A large-signal analysis of sub-harmonic parametric oscillations in Power Amplifiers (PAs) is presented in this paper. Simplified models for current-voltage and channel charge characteristics of short-channel pseudomorphic High Electron Mobility Transistors (pHEMTs) are adopted to investigate the effects of the device transconductance and gate-source capacitance nonlinearities on the amplifier stability. A 5-W Ku-band PA is designed to demonstrate the application of the presented analysis. MMIC PA is implemented in a 0.25- μm GaAs pHEMT process. According to the measurements, the PA provides 37.5 dBm (5.6 W) of output power, 36% of Power Added Efficiency (PAE), and small-signal gain of 18 dB on the frequency band of 12-15 GHz.

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1. Introduction

Power Amplifiers (PAs) are prone to various types of instabilities which can degrade the circuit performance. The PA stability should be examined in both small- and large-signal operation conditions. The small-signal stability is carried out on the basis of linearized circuit equations around its operating point. This stability can be readily evaluated using conventional stability criteria such as μ factor. In large-signal instability, the PA unstable behavior often manifests in certain intervals of frequency and input power, while PA may be stable in the absence of input signal. Thus, large-signal analysis and simulations are required to predict the possible existence of instability prior to circuit fabrication.

There are various mechanisms considered as the origin of large-signal instability in PAs [1-4]. One of the most prevalent types of instability in PAs is parametric instability. This type of instability appears when nonlinear parameters of PA, e.g. capacitance values,

are altered by the input signal and generate negative resistances. For instance, the gate-source capacitor (C_{gs}) of a pHEMT device is nonlinear with respect to the gate source voltage. This nonlinear capacitor is pumped by input RF signal. As will be shown later, it generates a negative resistance at sub-harmonic, like $f_0/2$, which could lead to parametric oscillation at these frequencies. The parametric oscillation can occur in either odd or even mode. The odd- and even-mode parametric oscillations occur due to the presence of power-divider and combiner in PAs with multiple transistors in the amplifier internal loops. The even-mode oscillation happens when all parallel transistors in the same stage oscillate in phase. On the other hand, the odd-mode oscillations occur when two groups of transistors oscillate 180 degree out of phase [5,6].

Parametric oscillations degrade efficiency and output power of amplifier. In the presence of oscillations, the available output swing cannot be fully exploited by the main harmonic of the output signal, thus the output power is degraded. Moreover, oscillations result in power consumption to generate unwanted signals, degrading the amplifier efficiency. Furthermore, they

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introduce spurious signals that can act as interferer for other bands.

Once the instability is detected, an appropriate solution should be applied to stabilize the circuit with minimum side effects on its normal behavior. Conventional methods for elimination of PA instability include the addition of parallel or series resistors in circuit sensitive nodes or branches to suppress the parametric oscillations. Insertion of resistors between parallel branches of multi-transistor PAs can also diminish odd-mode oscillations [4]. One limitation of these techniques is that extensive simulations should be performed to determine the value of the compensation network elements. An analytical approach to determine the required values of the compensation network can substantially alleviate this process.

In this paper, a simplified model for the I-V characteristic of short-channel pHEMTs excerpted from [7] is used in the analysis. Also, a nonlinear gate charge model is adopted to describe the capacitance nonlinear behavior. The stability analysis using these models is presented in Section 2. Section 3 describes the design of a 5-W Ku-band PA to demonstrate applications of the presented analysis. Experimental results for the PA implemented in a 0.25- μm gate length GaAs pHEMT process are given in Section 4.

2. Parametric stability analysis of short-channel pHEMTs

The PA instability can be investigated by examining the real part of input impedance $[\text{Re}(Z_{\text{in}})]$ of a unit transistor cell. The circuit used in the analysis is shown in Figure 1. The simplified transistor equivalent circuit model consists of a nonlinear gate-source capacitance (C_{gs}), linear gate-drain (C_{gd}) and drain-source (C_{ds}) capacitances, and a nonlinear voltage-controlled current source. Here, $Y_L = G_L + jB_L$ is the optimum load admittance for maximizing the output power extracted from load-pull simulation.

Using the circuit shown in Figure 1, the input current (i_{in}) is composed of the currents flowing in C_{gs} (i_{gs}) and C_{gd} (i_{gd}). Currents i_{gs} and i_{gd} are given

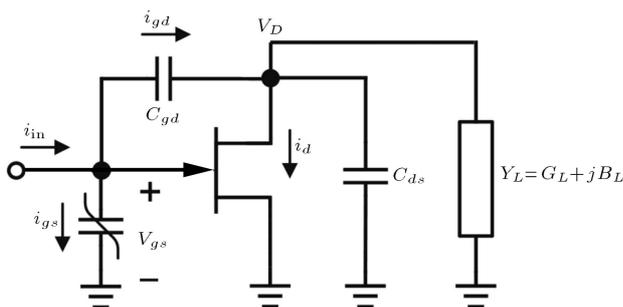


Figure 1. Unit cell of transistor model.

by:

$$i_{gs} = \frac{\partial Q_{gs}}{\partial t}, \tag{1}$$

$$I_{GD} = j\omega_0 C_{gd}(V_{GS} - V_D) = (G_L + jB_L + j\omega_0 C_{ds})V_D + I_D, \tag{2}$$

where I_{GD} is the phasor of i_{gs} . To solve these equations to find the input impedance Z_{in} , appropriate models for drain current and gate charge are needed. These models must describe instability behavior precisely, while maintaining simplicity.

Previous studies on parametric stability of pHEMT transistors have been based on square law model [3]. Although this model simplifies the analysis, it does not accurately predict the behavior of short-channel transistors. Using accurate models such as commercial EEHEMT model leads to complicated equations. Thus, a simplified form of Statz model that includes short-channel effect is used [7]. The I-V characteristic of a short-channel pHEMT in the linear mode of operation can be approximated by:

$$I_D = I_{DSS} \frac{\left(1 - \frac{V_{GS}}{V_P}\right)^2}{1 - \alpha \frac{V_{GS}}{V_P}}, \tag{3}$$

where I_{DSS} is the drain current at zero gate-source voltage, V_P is the pinch-off voltage, and α is an empirical parameter ($0 < \alpha < 1$) introduced to model short-channel effects in the current-voltage characteristic. Eq. (3) is used to model two typical pHEMTs with channel lengths of 0.25 μm and 0.15 μm . As shown in Figure 2, the model given by Eq. (3) can accurately predict the current-voltage of short-channel devices. The value of α is found to be about 0.7 and 0.8 for 0.25 μm and 0.15 μm devices, respectively. The transistors have 150 μm gate width and are biased

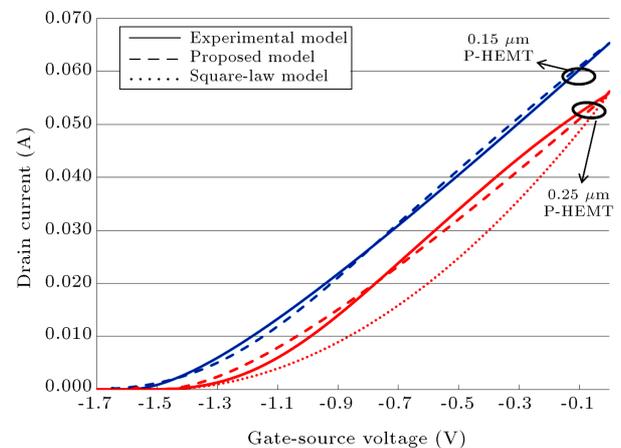


Figure 2. Comparison of short-channel pHEMT models.

with the drain-source voltage of 8 V. It is observed that the I-V characteristics of these devices exhibit significant deviation from square law model. It should be notified that Eq. (3) models nonlinear behavior of I_D as a function of V_{GS} . As the load of transistor (R_L) is much smaller than its output resistance (r_o), the effect of channel length modulation is neglected.

In the EE-HEMT model, gate charge (Q_{gs}) is represented by complex nonlinear terms, which make the equations difficult to solve. In order to simplify the analysis, the gate charge of a pHEMT transistor can be approximated by a fifth-order polynomial equation:

$$q(v_{gs}) = q_0 + q_1 v_{gs} + q_2 v_{gs}^2 + q_3 v_{gs}^3 + q_4 v_{gs}^4 + q_5 v_{gs}^5, \quad (4)$$

where q_i 's are process-dependent coefficients. The parametric oscillation commonly occurs at the sub-harmonics of the input frequency. Therefore, v_{gs} can be written as:

$$v_{gs} = v_{gs0} + v_{gs1} \cos(\omega_0 t) + v_{gs2} \cos(n\omega_0 t + \varphi), \quad (5)$$

where ω_0 is the possible sub-harmonic oscillation frequency ($\omega_0 = \omega_{in}/n$). In this definition, v_{gs} is composed of DC signal (v_{gs0}), oscillation signal [$v_{gs1} \cos(\omega_0 t)$] and pumping RF signal [$v_{gs2} \cos(n\omega_0 t)$].

The condition for the existence of sub-harmonic oscillation at ω_0 can be expressed as $Y_{in}(\omega_0) + Y_S(\omega_0) = 0$, where Y_{in} and Y_S are the input admittance of the transistor and source admittance, respectively. Even though This condition is dependent on the source admittance seen by the transistor, the sufficient condition for stability is $\text{Re}\{Y_{in}(\omega_0)\} > 0$. In order to determine the input admittance of circuit [$Y_{in}(\omega_0)$] shown in Figure 1, the following equation can be used:

$$Y_{in}(\omega_0) = \frac{I_{IN}}{V_{gs1}}, \quad (6)$$

where I_{IN} , the phasor of i_{in} , can be calculated using Eqs. (1) and (2). Substituting Eqs. (1)-(5) in Eq. (6), it can be shown that the real and imaginary parts of the input admittance are given by:

$$\begin{aligned} \text{Re}(Y_{in}) = & K_1(A_0 + A_1 \cos(\varphi)) + K_2 \\ & + (A_2 - K_3 A_1) \sin(\varphi), \end{aligned} \quad (7)$$

$$\begin{aligned} \text{Im}(Y_{in}) = & K_3 A_0 + K_4 - K_1 A_1 \sin(\varphi) \\ & + (K_3 A_1 - A_2) \cos(\varphi), \end{aligned} \quad (8)$$

where K_i 's are given by:

$$K_1 = \frac{\omega_0 C_{gd}(B_L + \omega_0 C_T) I_{DSS}}{G_L^2 + (B_L + \omega_0 C_T)^2}, \quad (9)$$

$$K_2 = \frac{G_L \omega_0^2 C_{gd}^2}{G_L^2 + (B_L + \omega_0 C_T)^2}, \quad (10)$$

$$K_3 = \frac{G_L \omega_0 C_{gd} I_{DSS}}{G_L^2 + (B_L + \omega_0 C_T)^2}, \quad (11)$$

$$K_4 = \omega_0 \begin{pmatrix} C_{gd} - \frac{\omega_0 C_{gd}^2 (B_L + \omega_0 C_T)}{G_L^2 + (B_L + \omega_0 C_T)^2} \\ - (q_1 + 2q_2 V_{gs0} + 3q_3 V_{gs0}^2 + \frac{3}{2} q_3 V_{gs2}^2) \\ - q_4 (4V_{gs0}^3 + 6V_{gs0} V_{gs2}^2) \\ - q_5 (5V_{gs0}^4 + 15V_{gs0}^2 V_{gs2}^2 + \frac{15}{8} V_{gs2}^4) \end{pmatrix} \quad (12)$$

A_0 and A_1 are derived by solving Eq. (2):

$$A_0 = \begin{pmatrix} \frac{(\alpha-2)}{V_P} + 2 \frac{(1-\alpha)^2}{V_P^2} V_{gs0} \\ + 3 \frac{\alpha(1-\alpha)^2}{V_P^3} (3V_{gs0}^2 + \frac{3}{2} V_{gs2}^2) \\ + \frac{\alpha^2(1-\alpha)^2}{V_P^4} (4V_{gs0}^2 + 6V_{gs0} V_{gs2}^2) \end{pmatrix}, \quad (13)$$

$$\begin{aligned} A_1 = & \frac{(1-\alpha)^2}{V_P^2} V_{gs2} + 3 \frac{\alpha(1-\alpha)^2}{V_P^3} V_{gs0} V_{gs2} \\ & + \frac{\alpha^2(1-\alpha)^2}{V_P^4} \left(\frac{3}{2} V_{gs2}^3 + 6V_{gs0}^2 V_{gs2} \right). \end{aligned} \quad (14)$$

A_2 is derived from the current flowing through nonlinear capacitor C_{gs} :

$$A_2 = -\omega_0 \begin{pmatrix} q_2 V_{gs2} + 3q_3 V_{gs0} V_{gs2} + \frac{3}{2} q_4 V_{gs2}^3 \\ + 6q_4 V_{gs0}^2 V_{gs2} + 12q_5 V_{gs0} V_{gs2}^3 \\ + 10q_5 V_{gs0}^3 V_{gs2} \end{pmatrix}, \quad (15)$$

where $C_T = C_{ds} + C_{gd}$, G_L and B_L are real and imaginary parts of Y_{in} , respectively. Eqs. (7)-(15) indicate that depending on the phase relations of the excitation components (φ) and the amplitude of RF signal (V_{gs2}), the oscillation condition can be satisfied at $f_{in}/2$.

These coefficients are extracted from 0.25- μm pHEMT transistor experimental model with the total gate width of 1.2 mm used in designed amplifier. The gate charge (Q_{gs}) diagram is derived based on simulations in Agilent ADS. Then it is fitted by the fifth-order polynomial equation in MATLAB. The order of the fitted polynomial is chosen based on the effective error (RMS), compared with simulated value of charge. In order to limit the RMS error to less than 10%, the fifth-order polynomial equation is used. This equation can be used to calculate i_{in} . In Figure 3, the model for $Q_{gs}(v_{gs})$ is compared with simulation results. As the gate bias voltage of the transistors is -0.8 V, and

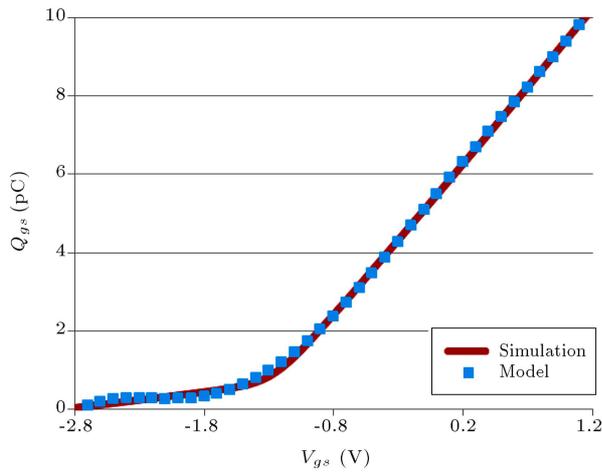


Figure 3. Comparison of simulated and modeled gate charge ($q_1 = 4.058 \text{ pC/V}$, $q_2 = -1.536 \times 10^{-1} \text{ pC/V}^2$, $q_3 = -3.083 \times 10^{-1} \text{ pC/V}^3$, $q_4 = 2.175 \times 10^{-1} \text{ pC/V}^4$, $q_5 = 7.633 \times 10^{-2} \text{ pC/V}^5$).

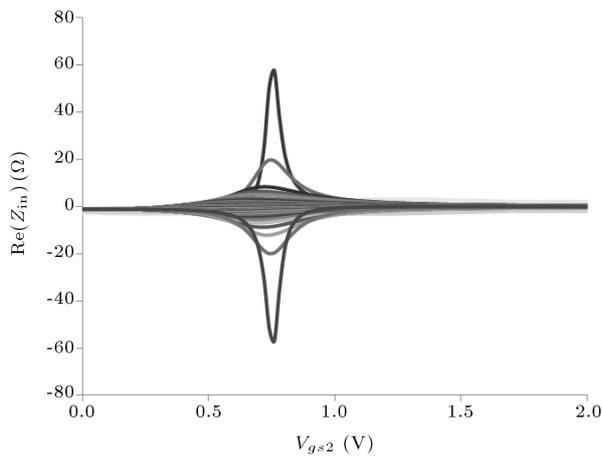


Figure 4. $\text{Re}(Z_{in})$ versus V_{gs2} for different relative phase (φ) at 13 GHz ($Y_L = 0.025 - j0.025 \text{ mho}$).

the maximum signal amplitude on the gate terminals is 2 V, the fitting is performed on the interval between -2.8 V and 1.2 V.

To investigate the instability condition of the transistor, $\text{Re}(Z_{in})$ is plotted in Figure 4 as a function of V_{gs2} for different values of φ . Here, V_{gs2} indicates the effect of input power, and φ relates to the random phase argument of oscillation signal. This diagram is plotted for $n = 2$, since $f_{in}/2$ is the most probable frequency of oscillation. The higher possibility of $f_{in}/2$ is due to short time-constant of the parametric mechanism in a pHEMT [8]. This analysis indicates that the parametric oscillation may occur in some specific intervals of input power, and disappear in higher input power levels. Therefore, the large-signal stability analysis of the PA should be performed in all input power levels. To get a clear insight about the mechanism of oscillation, it is worthwhile to investigate the effect of

circuit parameters on the location of oscillation. The effects of load admittance, gate-drain capacitance, and linear part of gate-source capacitance (q_1 coefficient) on $\text{Re}(Z_{in})$ are demonstrated in Figure 5.

The nonlinear gate-source capacitance is the main

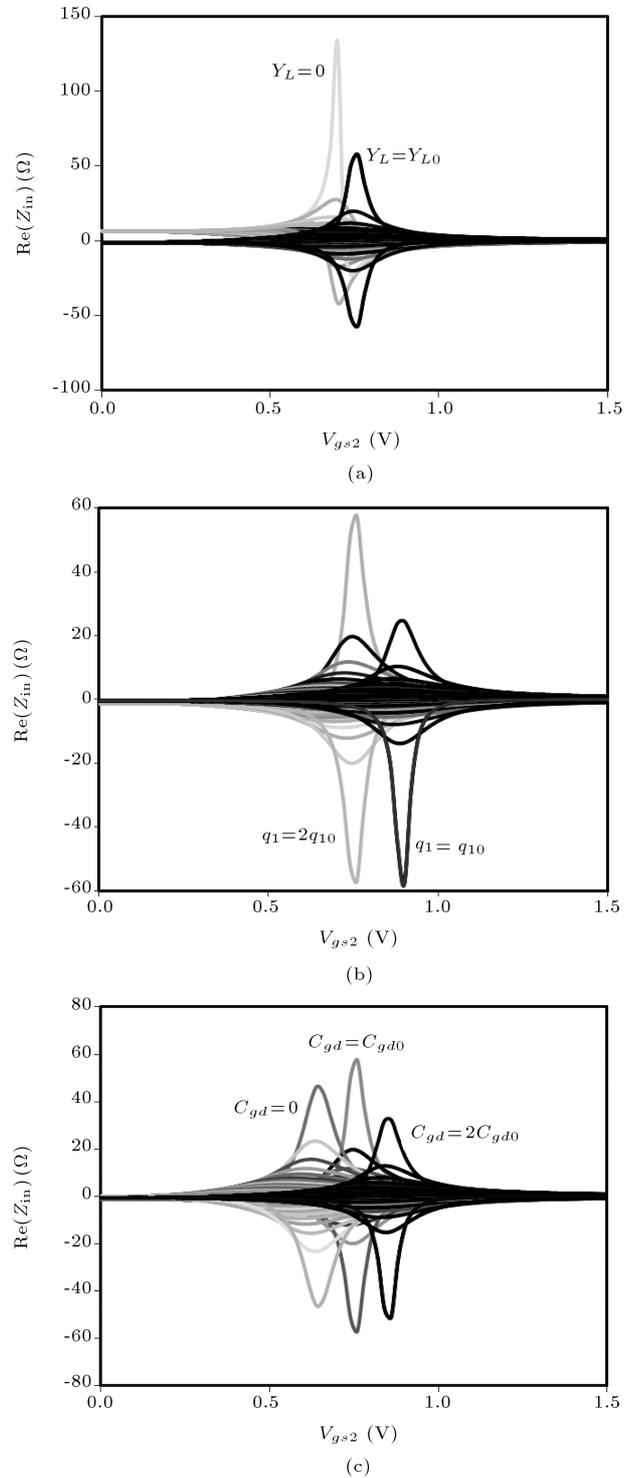


Figure 5. The effect of different parameters on $\text{Re}(Z_{in})$: (a) Load admittance; (b) q_1 (linear part of C_{gs}); and (c) C_{gd} .

source of this type of instability. Nonlinearity can be reduced by introducing a linear capacitance, in parallel with the gate-source terminals [8]. However, this capacitance causes some problems in designing high frequency circuits, including difficulty of matching network design as a result of increased input capacitance. In order to eliminate instability, a series resistance can be inserted in the gate of transistor to increase the real part of Z_{in} . Furthermore, a parallel capacitance with resistor is employed to avoid the gain degradation in higher frequencies (Figure 6).

The resistance value required to ensure stability is determined by the maximum voltage swing on the gate of transistors. Using Figure 6, it can be shown that:

$$R_{eff} = \left| \left(R \parallel \frac{1}{j\omega_{in}C} \right) \right| = \frac{\left| \frac{V_{gs2}}{V'_{gs2}(\omega_{in})} - 1 \right|}{|Y_{in}(\omega_{in})|}, \quad (16)$$

where $Y_{in}(\omega_{in})$ is the input admittance of transistor at the frequency of pumping RF signal. The values of $|Y_{in}(\omega_{in})|$ and $V'_{gs2}(\omega_{in})$ are respectively derived as 0.35 mho and 0.5 V, using ADS simulations. Figure 7 indicates the required resistance value in terms of voltage amplitude on gate of the transistor. Figure 8 indicates the comparison of $Re(Z_{in})$ before and after stabilization. As indicated in Figure 8, the stabilization network pushes the unstable region (where $Re(Z_{in})$ can

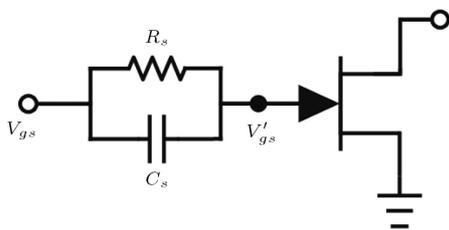


Figure 6. RC Stabilization network inserted in series with the gate terminal.

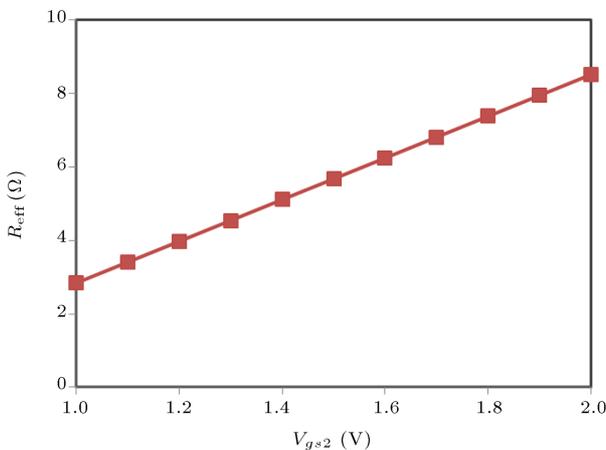


Figure 7. Required R_{eff} in order to stabilize transistor for different V_{gs2} (input signal amplitude).

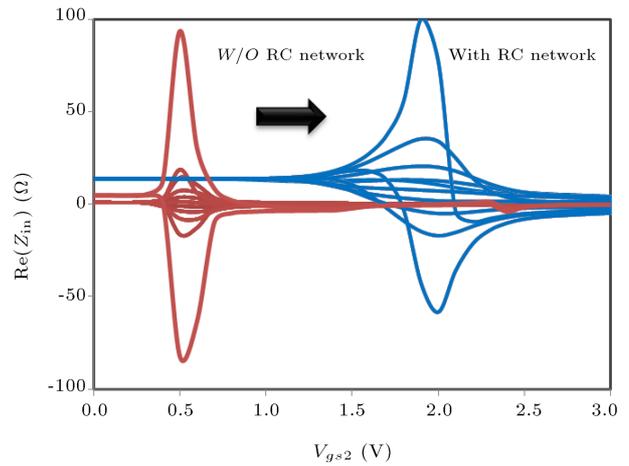


Figure 8. Comparison of $Re(Z_{in})$ before and after the stabilization at 13 GHz ($Y_L = 0.025 - j0.025$ mho).

become negative) to higher input power levels, thereby reduce the possibility of instability. It can be shown that this stabilizing network reduces the small-signal gain of PA, while it has negligible effect on the output power in saturation [9]. As indicated by Figure 5, adding a parallel resistor to the drain of device which increases G_L , decreases the effective amount of the necessary series resistance.

3. Design of Ku-band PA

The insights provided by the analysis in Section 2 are adopted in the stability analysis of a Ku-band PA in a 0.25- μm GaAs pHEMT process. Transistor cells are stabilized by parallel RC network in series with gate. The small-signal stability of transistor cells is examined through μ -factor criteria. In this design, a 20- Ω resistor in paralleled with a 2-pF capacitor providing μ factor greater than unity from 0.1 MHz to 20 GHz. These compensation network values ensure small-signal stability of the PA. To ensure large-signal stability, the effective series resistance value ($R_s / (1 + \omega_{in}^2 R_s^2 C_s^2)$) must be at least 9 Ω in the entire input frequency range. Thus, R_s and C_s are changed to 28 Ω and 1.2 pF, respectively, with a 2 Ω resistor series to them (Figure 9). Since this amplifier has broadband performance, the parametric stability has been examined on the entire frequency band.

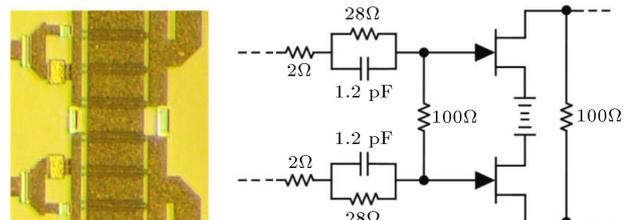


Figure 9. Layout and schematic of the stabilization network components.

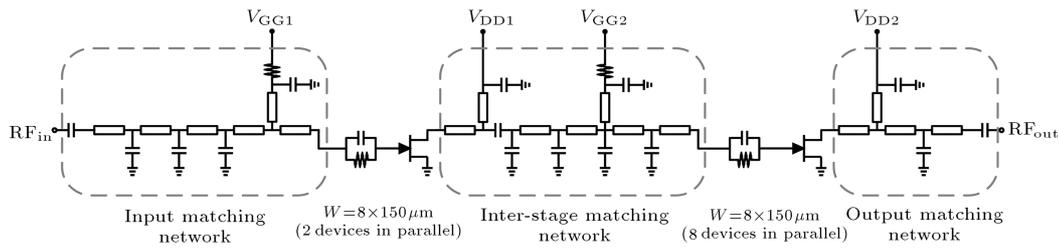


Figure 10. Simplified schematic of designed PA.

In the output stage of the PA, the output power of eight stabilized unit transistor cells are combined through a low-loss output matching network to achieve the total output power of 5 W. Meanwhile, the inter-stage matching network is designed so that the input impedance of second stage is transformed to optimum load of first stage required for maximum power and efficiency. Furthermore, the input matching circuit is used to flatten the overall gain of the amplifier, as well as achieving the input impedance matching (Figure 10).

To suppress the odd-mode oscillation, 100 Ω odd-mode suppression resistors (R_{odd}) are connected to drain and gate of the adjacent transistor cells (Figure 9). They have negligible effect on the output power in even mode, but suppress the odd-mode oscillation. As discussed earlier, in order to examine the parametric stability of the designed PA, pole-zero analysis is applied [10,11]. A small-signal perturbation current source is applied to each sensitive node of the circuit. The impedance seen at each node is then found, and it is used to extract the locations of its poles and zeros in MATLAB. The PA is designed to operate in the frequency band of 12–14 GHz. Therefore, the stability simulation and pole-zero extraction is performed at several input frequencies. The poles and zeros frequencies around $f_{in}/2$ after stabilization are depicted in Figure 11.

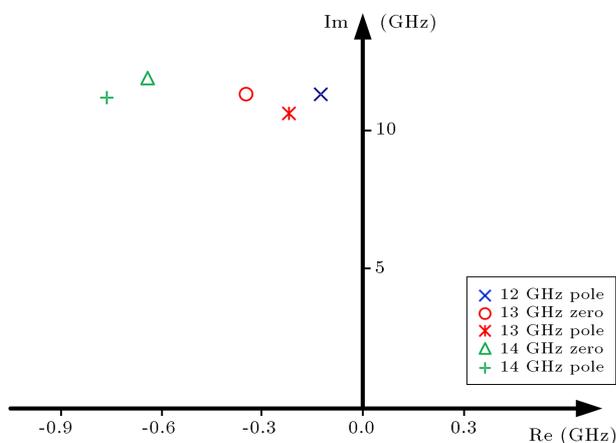


Figure 11. Pole and zero frequencies associated with auxiliary perturbation for different input frequencies ($P_{in} = 23$ dBm).

4. Experimental results

The PA is implanted in 0.25- μm pHEMT process with 100- μm substrate thickness. The die photograph of the PA is shown in Figure 12. The PA chip is connected to the test board bias and signal lines, using bondwires. The bias condition for the PA are $V_{DD} = 8$ V and $V_{gs0} = -0.8$ V. The total quiescent bias current is 1.4 A, with 0.3 A in the first stage and 1.1 A in the second stage. Figure 13 indicates the small-signal gain S parameters of the PA measured, using Agilent E5071 vector network analyzer. The PA has an average small-signal gain of 18 dB, and the input and output return losses are better than 8 and 10, respectively.

The PA output power is measured using Agilent U2000A power sensor. Figure 14 shows the output power and power added efficiency (PAE) in the Continuous Wave (CW) mode of the operation. The input power of the PA is 23 dBm. The amplifier provides an output power more than 37.5 dBm and PAE of better than 36% in the 12–15 GHz frequency band. The performance of the PA is summarized in Table 1, and compared with several similar designs. To compare the

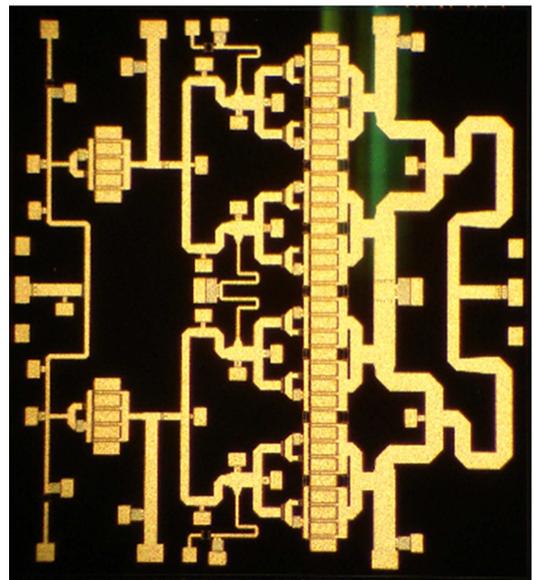
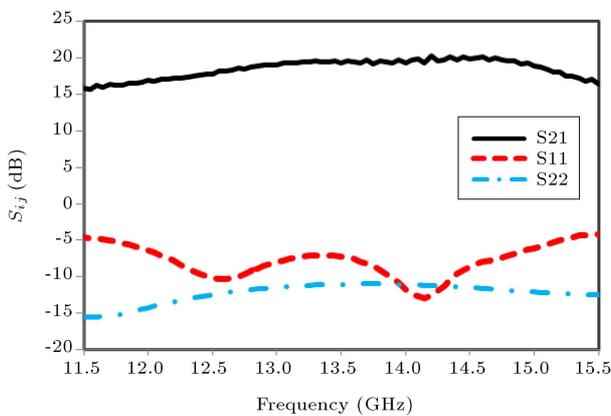
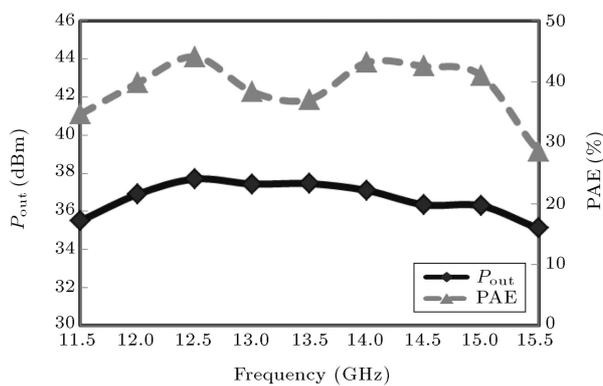


Figure 12. Die photograph of the implemented Ku-band PA.

Table 1. Comparison of the implemented PA with similar designs.

Reference	[12]	[13]	[14]	[15]	[16]	This work
Technology	0.35 μm pHEMT	0.2 μm pHEMT	0.25 μm pHEMT	0.35 μm pHEMT	0.25 μm pHEMT	0.25 μm pHEMT
Frequency (GHz)	10.7-12.7	8-14	14	13.6-14.2	13.5-15	12-15
P_{out} (dBm)	38.2	35	33	38.1	39	37.5
PAE (%)	35	40	25	24	20	36
Gain (dB)	15	17	15	10.5	22	18
V_{DD} (V)	8	8	7	8	9	8
Chip Area (mm^2)	10.5	15.78	13.44	8.55	11.21	9.15
$P_{\text{out}}/\text{Area}$ (mW/mm^2)	620	200	149	760	709	615
FOM ($\text{W}\cdot\text{GHz}/\text{mm}^2$)	43.4	48	-	10.9	21.3	66

**Figure 13.** Measured small-signal S parameters of PA.**Figure 14.** Measured output power and PAE of PA for $P_{\text{in}} = 23$ dBm.

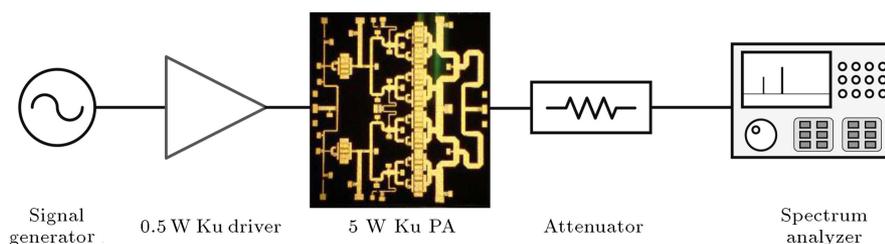
amplifiers fairly, a figure of merit is defined as:

$$\text{FOM} = \frac{P_{\text{out}} \times \text{PAE} \times \text{BW}}{\text{Area}} \quad (17)$$

To examine the stability of the implemented PA, it is driven with different levels of input RF signal. Then, the output spectrum is carefully examined for any unwanted oscillations. This test is performed throughout the operation frequency band. According to this experiment, no unwanted signal was detected in any subharmonic components of the input frequencies (Figure 15).

5. Conclusion

In this paper, the mathematical analysis of parametric oscillation in a pHEMT PA is presented. A simplified model for current-voltage characteristic and a polynomial function model for the gate charge of short-channel pHEMTs are used in the analysis. These models are adopted for large-signal stability analysis of a pHEMT device to derive conditions for sub-harmonic parametric oscillations. The insights obtained from the presented analysis are used to stabilize a Ku-band pHEMT high-power amplifier. The PA, implemented in a 0.25- μm GaAs pHEMT process, achieves an average output power of 37.5 dBm, and PAE of 38%. The PA small-signal gain is 18 dB, and its input and

**Figure 15.** Measurement setup used to detect PA instability.

output return losses are better than 8 and 10 dB, respectively.

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Appendix I

This part is devoted to clarify the approach of deriving Eqs. (7)-(15). To expand I_D to sub-harmonic components, Eq. (3) can be written as:

$$I_D = I_{DSS} \frac{\left(1 - \frac{V_{GS}}{V_P}\right)^2}{1 - \alpha \frac{V_{GS}}{V_P}} = I_{DSS} \frac{(1-x)^2}{1-\alpha x},$$

$$x = \frac{V_{GS}}{V_P}, \quad |\alpha x| < 1. \quad (A1)$$

Using Taylor series, Eq. (A1) can be simplified to:

$$\begin{aligned} \frac{(1-x)^2}{1-\alpha x} &= (1+x^2-2x) \\ &\times (1+(\alpha x) + (\alpha x)^2 + (\alpha x)^3 + \dots) \\ &= 1 + (\alpha - 2)x + (1 - \alpha)^2 x^2 \\ &+ \alpha(1 - \alpha)^2 x^3 + \alpha^2(1 - \alpha)^2 x^4 + \dots \end{aligned} \quad (A2)$$

To calculate the amplitude of sub-harmonic components, Eq. (5) should be substituted with V_{gs} . After expanding I_D , it is given by:

$$I_D = I_{DSS} A, \quad (A3)$$

where A contains components at different frequencies: DC, ω_0 , $(n-1)\omega_0$, $(n+1)\omega_0$, $(n-2)\omega_0$, $(n+2)\omega_0$, $(n-3)\omega_0$, $(n+3)\omega_0$, $n\omega_0$, $(2n-1)\omega_0$, $(2n+1)\omega_0$, $(3n-1)\omega_0$, $(3n+1)\omega_0$, $2\omega_0$, $2n\omega_0$, $3\omega_0$, $3n\omega_0$, $4\omega_0$, $4n\omega_0$, $(2n-2)\omega_0$ and $(2n+2)\omega_0$.

To find I_D at ω_0 for $n=2$, the components at ω_0 , $(n-1)\omega_0$ and $(n-3)\omega_0$ should be considered.

Therefore, the phasor of I_D at ω_0 is given by:

$$I_D = I_{DSS} \left[\begin{array}{l} \left(\begin{array}{l} \frac{(\alpha-2)}{V_P} V_{gs1} + \frac{(1-\alpha)^2}{V_P^2} (2V_{gs0} V_{gs1}) \\ + \frac{\alpha(1-\alpha)^2}{V_P^3} \left(\frac{3}{4} V_{gs1}^3 + 3V_{gs0}^2 V_{gs1} \right. \\ \left. + \frac{3}{2} V_{gs1} V_{gs2}^2 \right) + \frac{\alpha^2(1-\alpha)^2}{V_P^4} (4V_{gs0}^3 V_{gs1} \\ \left. + 3V_{gs0} V_{gs1}^3 + 6V_{gs0} V_{gs1} V_{gs2}^2 \right) \\ \left(\begin{array}{l} \frac{(1-\alpha)^2}{V_P^2} (V_{gs1} V_{gs2}) \\ + \frac{\alpha(1-\alpha)^2}{V_P^3} (3V_{gs0} V_{gs1} V_{gs2}) \\ + \frac{\alpha^2(1-\alpha)^2}{V_P^4} \left(\frac{3}{2} V_{gs1} V_{gs2}^3 \right. \\ \left. + 6V_{gs0}^2 V_{gs1} V_{gs2} \right) \end{array} \right) \end{array} \right] \angle \varphi \quad (A4)$$

The phasor of gate charge is derived using the same method from Eq. (4).

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