Design and Validation of efficient Z source breaker with voltage stress reduction for DC Microgrid

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Abstract

The integration of renewable energy generation in grid results in reduced carbon emissions in the atmosphere. Despite technical advancements, critical issues oriented to protection strategies for renewable integration in microgrid structures still remain unresolved. Foremost aspects that need to be concentrated while securing the grid includes rapid fault interruption, auto reclosing prohibition and stress on the switching devices. This paper improves the fault isolation speed and voltage stress reduction by redesigning the inductance and capacitance value of Z-source DC circuit breaker. This strategical breaker is applied and tested for various types of faults in a 7-bus microgrid system, where its efficacy in interrupting the fault in existing with proposed proves less voltage stress and fast fault interruption. In addition, the proposed LC tuned breaker is tested with adaptive algorithm for auto tripping and fast reclosing in smart microgrid environment. The experimentation of the suggested work is carried out in Opal RT control hardware in loop (CHIL) testing.

Keywords: DC microgrid, Fault detection, Z source breaker, Voltage spike, DC circuit breaker

1. Introduction

Connecting renewable energy sources through microgrid is becoming an eternally viable solution for future energy needs [1]. Incorporation of distributed energy sources are simpler in DC (Direct current) microgrid system. In addition, it is more reliable and efficient when compared to AC system. However, protection remains an essential concern in the development

of DC microgrid systems due to the following factors [2]. Due to the fact that the DC system has a lower impedance than the AC system [3], when a short-circuit fault occurs, it penetrates the system more swiftly and deeply [4]. The development of an electromechanical circuit breaker with a fast-acting switch which takes advantage of rapid response time but is inefficient for highly sensitive loads. Considering the limitations of conventional breakers paves the way for the solid-state circuit breaker, which can break fault current within 1 ms with no arc and spark [5]. The solid-state circuit breaker beneficially solves the problems in mechanical circuit breakers (MCBs), which depend on additional solid-state switch for faster fault isolation [6]. However, switching and conduction losses are substantial [7]. Adapting advanced techniques with conventional DC circuit breaker can mitigate limitations, such as moderate fault-breaking capability, prolonged auto reclosing time, and sudden voltage spikes that affect the lifespan of the protective device [8].

Corzine [9] proposed a Z-source breaker which paves the way for a new trend in making the circuit breaker that works with a simple SCR connected to crossed capacitance combination. The working principle of this circuit is during the fault occurrence, the current through the Z-source inductor stands the same. The respective voltage and current stress are 9V and 0.85A and the surge due to the fault is 48A. Though it has improved from [10] and [11], still the number of passive elements and the switching device can be reduced, and a minimum fault ramp rate should be found.

In [12], a breaker is designed that works based on precise adjustment of turns ratio of the coupled inductors ensuring optimal performance of the breaker. The operation of breaker works symmetrically during bidirectional power flow isolating the fault in 10 μs with no source fault current reflection. The voltage and current stress are 11 V and 0.9 A and the surge due to the fault is 10 A. In [13-14], a voltage spike of 102V occurs during the reclosing operation due to the presence of reverse recovery voltage by SCR. Also, an unexpected current spike of 19A occurs during the opening and closing of the breaker, which may result in serious damage to the power electronic devices connected to the circuit [15]. The bidirectional TSCB [16] attains low ON-state loss. However, this circuit breaker necessitates two substantial electrolytic capacitors, thereby escalating both costs and volume. A low-loss bidirectional T-source circuit breaker (NBTSCB) has been proposed [17], wherein integrated mechanical switches are employed to curtail the number of switching components. This design exhibits a notable reduction in on-state

conduction loss by almost 40% (181W). QZSCB [18] has extended isolation time (5000 μs) and the presence of a substantial reflected source current. The voltage and current stress are 1.2 V and 3.94A and the surge due to the fault is 22 A. Savaliya et al. [19] proposed and analyzed the performance of the breaker under step load conditions, demonstrating its robustness by remaining impervious to inadvertent triggering even under load step changes (up to five times). Additionally, the voltage stress across the Silicon-Controlled Rectifier (SCR) is at 1.33 times the supply voltage, a significantly lower magnitude as the other breakers has a voltage spike of almost 10% of the supply voltage.

A novel bidirectional Direct Current Circuit Breaker (DCCB) with fault decision-making capabilities for DC microgrids has been introduced [20]. This improvement results in a reduction in both the size and estimation of the DCCB. A synergistic integration of Cryogenic Power Electronics (CPE) with superconducting Z-source DC circuit breaker technology [21] has been proposed, demonstrating a substantial 62.1% reduction in total losses within the 2kW system. This reduction is achieved without factoring in additional fault detection modules, thereby averting time-delayed responses and unnecessary breaking actions. An integration of the Thomson coil (TC) in Zero-Current Switching Circuit Breaker (ZCB) [22] has been implemented where the Thomson coil activates, enabling the isolation of the fault in 2.5 milliseconds. A flipped τ source breaker is a modified model of τ source [23] which reduces cost, size and fault interruption time to 400 μs. Nevertheless, the fault protection is contingent at the load operational state. The hybrid configuration of IGBT and thyristor integrated with Z source [24], achieves independent active turn-off irrespective of the fault conductance. Incorporating the ultrafast mechanical switch (UFMS), attains ultralow losses and the capability for active turn-off. Yet, there is a chance for improvement in its turn - OFF speed, as highlighted in [25]. Tao Li's [26] has suggested a new z-source breaker to detect the fault with minimum detectable fault ramp rate and the fault interruption is in 600 μs. However, the voltage stress and current stress observed during the breaker's opening and reclosing phases are remarkably high (15kA) in comparison to other extant z-source circuit breakers. The voltage and current stress are 480 V and 420 A and the surge due to the fault is 410 A.

From the literature survey, it is understood that it is a significant challenge to design and implement a proper protection device for a DC microgrid as it has no natural zero-crossing current, complicating fault current breaking. Especially, proper design of L and C in the thyristor

circuit is critical to avoid the voltage stress and the subsequent voltage and current spikes during reclosing operation. These sensitive spikes may result in substantial sparking, leading to significant damage to the breaker contacts.

To mitigate the risk of sparking or flashing during reclosing events, a supplementary capacitor recharging circuit, coupled with finely-tuned inductance (L) and capacitance (C) values, proves its effectiveness in interrupting the fault. An auxiliary circuit, operating in parallel with the capacitor, offers a methodological approach to fine-tune the LC values.

The consortium of this proposed work is as follows

Inductor and capacitor Redesign: The implementation of tuned L and C values reduces the voltage stress caused and this tuned L and C values is analyzed in the circuit with 810 combinations of different inductor and capacitor values. This analysis reduces the voltage stress and make the breaker more compact than the actual design. The cost of the proposed breaker is less compared to the existing topology.

Addition of capacitor pre charging circuit and two inductors in parallel to the capacitors: When the fault current is reflected to the source, it results greater damage to the source connected to it. So, to minimize and suppress the fault magnitude, pre charging a capacitor with current flowing through it during fault. Also, an inductor in parallel with capacitor is implemented to minimize the fault current magnitude which results in smoother operation.

Application of the proposed design in seven bus DC microgrid system with adaptive protection algorithm: The proposed breaker design proves its efficiency when it is implemented with adaptive protection algorithm such as Prims, Kruskal and Bourka combined with Dijkstra, Floyd Warshall and Bellman Ford in a Seven bus DC microgrid system.

The application of the proposed breaker design in a 50 kW seven-bus DC microgrid system: This focuses on scrutinizing the efficiency of the breaker. The implementation is specifically executed within the confines of the 50-kW system, and the results are validated through software-in-loop testing using a real-time simulator.

The organization of the paper is as follows: Section II delineates the modelling of seven-bus DC microgrid system and Z-source breaker topologies. Section III explains the parameter estimation of modified Z-source breaker and its fault ramp rate calculation. Section IV portrays the results of suggested breaker and its voltage and current stress reduction under various fault conditions. Section V briefs out the implementation of modified Z-source breaker in seven bus DC microgrid and Section VI explains the conclusion and future work.

2. Need for modelling of Z-source breaker using Minimum Detectable Fault Ramp Rate

Generally, a Z-source breaker consists of a thyristor, with a twin of inductor, capacitor and a snubber circuit as shown in Fig. 1 [9]. During fault period, the thyristor tends to turn off when the current through Z-source capacitor equals the Z-source inductor.

Conventional Z-source breaker topology [9]

The Fig. 2 [13] shows the necessity of inductor requirement in return path of DC source is sorted in parallel z-source type where the pair of inductor and capacitor are in-line with the DC source to provide a common ground [9-16].

Inductor based Breaker modelling [13]

Tao Li in his proposed new z source breaker [26] shown in Fig. 3 satisfies the z-source breaker condition i.e., when the inductor current equals the capacitor current, the SCR will turn off which is the major condition for designing a Z source breaker.

New Z-source Breaker modelling [26]

Given the current configuration of inductance and capacitance values, the breaker encounters voltage stress significant enough to produce a voltage spike five times higher than the supply voltage. Consequently, such a spike could potentially prolong the existence of an arc at the breaker terminal. Thus, fine-tuning the inductance and capacitance values at minimum fault ramp rate calculation, along with implementing an appropriate auxiliary circuit, can effectively mitigate the stress on the switching device.

3. Application of existing breaker topology in Seven Bus radial DC Microgrid System

3.1. Modelling of Renewables

3.1.1. PV Modelling

A standalone DC microgrid, with Solar, wind and Battery as sources and resistive loads are considered for the proposed study. The PV considered for the study is of 3kW with 32 cells

connected in series and 1 in parallel to make a single module. Therefore 24 modules are connected to provide a voltage of 400V. Fig. 4 shows the equivalent circuit of single diode model of PV cell [27].

Single diode model of PV cell [27]

Considering $V_{PV} = V_{OC}$ $N_p = 1$ *and* $N_s = 36$, the PV module is designed based on the given equation for I_{PV} which can be written as,

$$I_{pv} = I_{ph} - I_o\left[exp\left\{\frac{q\left(V_{PV} + I_{PV}R_S\right)}{N_S AKT}\right\} - 1\right] \quad (1)$$

Where I_{ph} is the photo-current in Amps, I_{rs} is reverse saturation current, I_{PV} is the output current,V_{PV} is the output voltage,V_{OC} is the open circuit voltage, I_O is the saturation current of a module varies with temperature of a cell, N_S is number of cells connected in series and R_S is series resistance, respectively. Furthermore, the boost converter interfaced with photo-voltaic array is used to increase the required voltage levels during low irradiation period.

3.1.2. PMSG wind modelling

Fixed speed direct-drive wind turbine with a permanent magnet synchronous generator (PMSG) [28]

Fig. 5 shows the working model of permanent magnet synchronous generator (PMSG) based fixed speed wind turbine (WT) [28]. Considering a fixed speed of 9m/s as the wind speed and zero pitch angle, the aerodynamic model of a wind turbine is given by

$$P = \frac{1}{2}\rho AC(\lambda)\, V^3 \quad (2)$$

Where P - wind power generated,ρ - air density, A - area covered by the blades, v - wind speed, C_p - power coefficient and λ - tip speed ratio.

Tip speed ratio,

$$\lambda = \frac{Rn\pi}{30v} \quad (3)$$

where n - wind turbine rotor speed in revolutions per minute(r/min).

$$T_m = \frac{P_\omega}{\omega_m} = \frac{0.5\rho A_r C_p(\alpha,\beta)\, v^3}{\omega_m} \quad (4)$$

where S stands for Blade span Area, α signifies the angle of attack, and β indicates pitch angle. The fixed speed PMSG wind turbine is designed to produce an output of 400V, 2kW and a

rectifier is connected for converting the AC input from turbine to DC output with LC filter value of 47uH and 220uF, respectively.

3.1.3. Battery Modelling

The battery modelling requires adequate importance since the microgrid has bidirectional power flow. So, a bidirectional battery modelling of 2kWh with buck-boost converter is required to interlink in DC bus [29]. The radial configuration of DC microgrid architecture integrated with renewables and loads as framework of DC microgrid is shown in Fig. 6. The existing new z source breaker [26] considered for the study are represented as CB1 to CB8 and respective relays are R1 to R8. During normal operating conditions, the current in forward direction from PV to Load 1,2,3 and 4. When a fault occurs in bus 3, immediately, the corresponding breaker CB3 operates in interrupting the fault.

Framework of DC microgrid

Voltage, Power and Current results of seven bus DC system and also Voltage and current of existing Z-source breaker during faulted period

The DC grid voltage, current and power are shown in Fig. 7 the Voltage and current of existing Z-source breaker during faulted period

From Fig. 7(d), it is observed that the voltage and current associated with the existing z-source breaker consequence in high stress on switching device, negative fault current and fault current reflected to the source in the DC grid.

3.2. Modelling of Z-source breaker using Minimum Detectable Fault Ramp Rate

New z source breaker topology [20] and Current flow of new z source breaker when SCR is turned off

The disadvantages of existing z source breakers are overcome by Tao Li in his proposed new z source breaker [26].

This breaker shown in Fig. 8 (a) satisfies the z-source breaker condition i.e., from Fig. 8 (b) when the current through inductor matches the capacitor current, the SCR will turn off which is the major condition for designing a Z source breaker. But, during reclosing operation of a breaker, a voltage spike occurs which portrays the switching stress caused by power electronic switches present in the breaker.

The voltage stress across the switching component is caused by load capacitor and z source components which result in permanent fault condition. The design equations for the z

source breaker topology designed in [26] are elaborated in the following parametric analysis. If the values of inductor and capacitor are incorrect and not designed accurately using design calculations, then the breaker may lead to reverse recovery volage which results in voltage stress in the breaker.

3.2.1 Parametric analysis of L and C design for Z-source breaker

The Z source breaker design is based on minimum rate of rise of fault current that makes the SCR turnoff when the z-source inductor current equals the z-source capacitor current. From the current flow path of fault current, the capacitor current can be written with respect to capacitor divider ratio,

$$I_c = \frac{C}{C + 3C_{load}} I_F \tag{5}$$

Where I_F is the fault current

During fault, $I_L = I_c = I_{load}$

The short circuit current from equation (5) can be written as,

$$I_F = \frac{C + 3C_{load}}{C} I_{load} \tag{6}$$

As this breaker works on fault conductance G_F at minimal rate [30],

From equation (5),

$$G_F = \frac{C + 3C_{load}}{C} \frac{1}{R_{load}} \tag{7}$$

(or)

Suppose the fault conductance ramp from [0 t], the fault conductance can be expressed as

$$G_f = k.t \tag{8}$$

Where k is the rising fault rate $k = \frac{G_f}{t}$

Let us assume the internal source inductance is negligible and constant load current, the fault current by load capacitor is detemined as

$$C_{load} \frac{dv_{out}}{dt} = - \frac{3C_{load}}{C + 3C_{load}} V_{out}.k.t \tag{9}$$

Solving the equation (9), the Taylor series expansion of output voltage and short circuit fault current can be written as,

$$V_{out} = V_{source}\left(1 - \frac{3.k.t^2}{2C + 6C_{load}}\right) \tag{10}$$

$$I_F = V_{source}.k.t.exp\left(-\frac{3.k.t^2}{2C + 6C_{load}}\right) \tag{11}$$

Combining (1) and (7), the capacitor current is,

$$I_C = V_{source}\frac{C}{C + 3C_{load}}exp\left(\frac{3.k.t^2}{2C + 6C_{load}}\right) \tag{12}$$

The time at which the maximum current calculation from the above equations are

$$t_{max} = \sqrt{\frac{C + 3Cload}{3k}} \tag{13}$$

$$I_{Cmax} = \sqrt{\frac{k}{3e\left(C + 3C_{load}\right)}}.C.V_{source} \tag{14}$$

Where e = 2.718 natural constant

When the capacitor current reaches its maximum value, it is concluded that it equals with load current. $\sqrt{\frac{k}{3e\left(C + 3C_{load}\right)}}.C.V_{source} = \frac{V_{out}}{R_{load}} = I_{load}$

(15)

The maximum z source capacitor current should be equal or greater than nominal load current. So, the minimum detectable fault ramp rate is

$$k_{min} = 3e\frac{1}{R_{load}.C}\left\{\frac{C + 3C_{load}}{C}\frac{1}{R_{load}}\right\} \tag{16}$$

$$I_C = V_{source}.\frac{C}{C + 3C_{load}}exp\left(k.t - \frac{9k^2.t^3}{2C + 6C_{load}}\right) \tag{17}$$

The following expression is the equation for no turn off period of SCR

$$\begin{aligned} I_{SCR} &= I_L - I_C \\ &= I_{load} - \frac{V_{source}C.k}{C + 3C_{load}}.t + \frac{V_{source}.k}{C + 3C_{load}}\left(\frac{1}{4L} + \frac{9.k.C}{2C + 6C_{load}}\right)t^3 \end{aligned} \tag{18}$$

Taking the third term of equation (18), the relationship of z-source breaker inductance is as follows,

$$\frac{1}{4L} << \frac{9.k.C}{2C + 6C_{load}} \tag{19}$$

On simplification of equation (19)

$$L >> \frac{1}{18k}\frac{C + 3C_{load}}{C} \tag{20}$$

$$L >> \frac{1}{54e}\left(R_{load}\right)^2.C \tag{21}$$

From the 10 times error margin consideration,

$$L \approx \frac{1}{12}\left(R_{load}\right)^2.C \tag{22}$$

3.2.2 Impact of Inductance in Z-source Breaker Design

The breaker interruption and reclosing are affected by voltage and current spike due to the switching components. This problem is portrayed and taken into consideration to reduce the stress caused by the switching components. Based on the expression of k_{min}, the inductor and capacitor values are chosen such that the minimum detectable fault ramp rate are identified. When $k > k_{min}$, the breaker disconnects the circuit, in which the value of k as $8300S^{-1}\Omega^{-1}$ [26], where $\frac{1}{18}$ times of value can be taken in to consideration for inductance.

3.2.3 Importance of Selection of Breaker Components

The value of k is the rate of rise of inductor current with respect to fault period. The value of k decides the breaker to interrupt during fault period. To obtain the k_{min} value during the fault period, various combinational analysis with respect to z-source capacitor and load resistor are carried out. On reducing the z-source capacitor and load resistor values the delayed response in detecting the rate of escalation of fault current is observed. This may lead to damage power electronic components present near the faulted network. So, choosing the optimal value of inductor, the circuit and equation (32) has to be redesigned.

4. Need for Redesigning Breaker Inductance and Capacitance

Voltage and Current stress during fault occurrence and reclosing operation of new z source breaker

The voltage stress in Fig. 9(a & b) replicates the spike in voltage and current during the interrupting and reclosing of a breaker. As the voltage spike reaches up to 5000V and the current raise up to 420A, the spike may affect the renewable sources and grid assets interfaced with it, if it becomes a permanent fault. So, the consideration towards this issue needs to be addressed. On proper designing of load capacitor, the voltage and current spikes can be reduced during the opening and closing of breakers. Based on the input and load requirements, the load capacitor and load resistor need to be redesigned.

5. Modified Design of Z-source breaker

Modes of operation of modified new z -source breaker for reducing voltage stress during Normal conduction mode, fault instant ,commutation of T1 and T2 and capacitor precharging circuit

As per the designed parameters and basic operation of Z-source breaker, during the fault occurrence, when inductor current equals with capacitor current, the SCR turn off. This was satisfied by the newly designed breaker waveforms which is illustrated in Fig. 10. The

During fault, Peak fault current with respect to SCR current and current flow in Z-source components

As in Fig. 10 (a & b), the first two modes of operation is same as [26] which is explained in section 2. After the commutation of T2, the capacitor C is charged to a negative voltage. The capacitor negative voltage for forward biasing the diode resulting in formation of conduction path through C, L and R. Later capacitor charges to the positive voltage resulting in the diode to reverse bias and making the loop to be inactive. Atlast, the capacitor is fully charged and it acts when there is a need for reclosing and rebreaking operation as shown in Fig. 10 (c & d). The following equation is derived for determining the optimal value of z-source inductor and capacitor.

Fig. 11(a) shows the fault occurrence at 5 second which reaches to ten times peak of 120A. Similarly, when inductor current equals to capacitor current at 18A, immediately the SCR trip off and satisfies the basic operation of proposed breaker design as portrayed in Fig. 11(b).

The following expression is the equation for no turn off period of SCR (T1 & T2) current

$$I_{SCR} = I_L - I_C$$
$$= I_{load} - \frac{V_{source} C.k}{C + 3C_{load}}.t + \frac{V_{source}.k}{C + 3C_{load}}\left(\frac{1}{6L} + \frac{9.k.C}{3C + 6C_{load}}\right)t^3 \quad (23)$$

The z-source breaker inductance has the following relationship,

$$\frac{1}{6L} << \frac{9.k.C}{3C + 6C_{load}} \quad (24)$$

$$L >> \frac{1}{20k}\frac{C + 3C_{load}}{C} \quad (25)$$

$$L >> \frac{1}{56e}\left(R_{load}\right)^2.C \quad (26)$$

From the 10 times error margin consideration,

$$L_{min} \approx \frac{1}{16}\left(R_{load}\right)^2.C \quad (27)$$

From the above Eq. (23-27), L_{min} is calculated with respect to Z source capacitance C. To find the minimal voltage and current rise, 810 combinations of L and C values were taken in to consideration. From the analysis, it is found that using the value of L as $1e^{-1}$ *and* $1e^{-2}$ with C as $1e^{-1}$ *and* $1e^{-2}$, the delay in reclosing operation of about 5 secs is considered and depicted in Table 1. This elongates the arc quenching period resulting in delayed operation of breaker reclosing. On the other hand, with any value of L with respect to C as $1e^{-3}$, the breaker fails to operate and the values are highlighted in Table 1. This combination is a failure case in Z-source breaker topology. Also, the analysis results in decreasing the voltage and current stress during breaker reclosing operation.

From the analysis of different combinational values for z-source components as shown in Table 1, it is concluded that the highlighted values in green make the breaker to work optimally with respect to standard DC voltage and reduces the voltage and current stress. For finding the optimal value of inductor and capacitor, the following procedure is carried out with 810 values of

LC combinational analysis. Among these values, a few values are portrayed in Table 1 and Fig. 12.

Different combination of L and C values for reducing voltage stress during reclosing operation of modified new z -source breaker when Fixing L value as $1e^{-1}$and varying C, Fixing L value as $1e^{-2}$, and varying C, Fixing C value as $1e^{-1}$ and varying L, Fixing C value as $1e^{-2}$, and varying L

By fixing the inductance value and varying the capacitance or vice versa, we reached the conclusion that when the chosen inductor and current values are very low, the auto-reclosing period becomes higher, leading to a longer arcing period. In contrast, when the breaker values chosen are higher, the breaker size gets increased. The LC combination with capacitor value of C as $1e^{-3}$ unit fails in reclosure of breaker for smooth system operation, resulting in unsuitable choice of LC values.

Table 1 Different combination of L and C values for reducing voltage stress during reclosing operation of modified new z -source breaker.

Table 1 shows the peak voltage spike of different combination of L and C values with voltage stress during reclosing operation of modified new z -source breaker. The voltage stress during reclosing operation of a breaker for few combinations of L with respect to C are portrayed in Fig.12.

Table 2 Breaker comparison

From this analysis, the breaker stress is reduced to ten times the peak from nominal voltage and current when compared to existing z source breaker. This highlights and proves the proposed LC values of breaker to work efficiently and reliably. The comparison of various breaker topologies is depicted in Table 2. Upon comparing various breaker topologies, it was found that the proposed breaker exhibits negligible negative fault current flow (0.0092A) and surge due to fault (2A). Additionally, the fault isolation speed is less compared to the New Z-source circuit breaker [26]. However, a significant advantage of the proposed breaker is that there is no fault current reflected back to the source, distinguishing it from other breakers. The primary objective of the breaker is achieved as both voltage and current stresses are considerably lower, measuring at 3V and 0.8A respectively, in contrast to values reported in other papers [10-13,17,18]. The efficiency of the proposed breaker for 5kW system is recorded as 99.1%, which

represents an optimal value when compared to other circuit breakers. Also, the breaker is tested for 50kW in the upcoming section which provides the efficiency of 98.27%.

6. Implementation of Modified Z-Source Breaker with Adaptive Algorithm Fed Controller in Seven Bus DC Microgrid

There are some algorithm-based protection techniques which predicts the active bus and identifies the shortest path for rapid fault interruption. In [31], an implementation of data structure algorithm for protection of microgrid carried out with the central controller that finds the active buses using prims algorithm and minimal distance of faulted path using Dijkstra's algorithm. The time complexity calculation for Prims and Kruskal algorithm, are termed as O(V2) and O (E log V) respectively where V is the number of vertices. The need for predicting the specified branch and its faulted bus in short span resulted in the acquisition of cascaded algorithms which is enhanced to prevent sympathetic tripping and blinding of protection in efficient manner [32-35]. This algorithm acts faster than other algorithm as it uses data structure and graph theory techniques for fault detection in DC microgrid. The proposed LC tuned breaker is implemented and checked for its efficiency of working in adaptive environment.

The modified LC tuned breaker is linked at the line, with the protection controller monitoring the status of the grid. If an overcurrent is detected in the line current, the protection controller examines the faulted branch. Additionally, if the line current falls below or rises above the threshold value, the adaptive active bus algorithm concurrently determines the status of the buses. Thereby, the least distance is determined using the shortest path algorithm. The adaptive relay setting works based on the commands from the protection controller. The active bus identification algorithm such as Prims, Kruskal and Boruvka are tested with shortest path algorithms such as Dijkstra, Floyd Warshall and Bellman-Ford for justifying its robustness and adaptability in the proposed breaker.

In this study, the Opal RT (real-time simulator) is employed, utilizing an external control strategy known as control hardware in loop (CHIL) testing. This approach is used to analyze the system performance with an adaptive algorithm interfaced with a modified Z-source breaker. In interfacing MATLAB/Simulink 2018a with Python, a model was developed to simulate a seven-bus DC microgrid system with proposed breaker incorporating a protection controller. The protection algorithm triggers an alarm signal directed to the overcurrent relay circuit on the breadboard via the DATA OUT channel. To facilitate communication, an Arduino is interfaced

with the processor through a USB cable port. This ensures the retrieval of node profiles without encountering overruns or delays. The hardware prototype undergoes examination. The hardware implementation closely follows the proposed seven-bus system for DC system voltage of 5V/div, with the breadboard circuit diagram emulating the configuration depicted in Fig. 13.

Experimental setup on implementation of adaptive algorithm with modified new z-source breaker

7. Results and Discussions

7.1 Implementation of Modified Z-Source Breaker in 5kW DC Microgrid System

7.1.1 Performance under Line-Line Faults

A Line-to-Line fault is induced at L23 and 34, that interfaced with relays R3 and R4 in a seven-bus islanded DC microgrid, where the inactive buses are identified as the LED turnoff automatically as shown in faulted bus identification setup. The fault path is 4-3-2-1-common bus (path weight - 4) where the other path weights are higher than the above calculated distance. In the identified shortest path, the corresponding proposed modified z-source circuit breaker interrupts the fault which is verified with CHIL testing. Fig. 14 shows the Faulted Path from line 3 -4 to PCC on occurrence of Line-to-Line Fault in Seven bus DC Microgrid.

Faulted Path on occurrence of Line-to-Line Fault in Seven bus DC Microgrid.

From Fig. 15(a) the DSO results evaluates the performance of modified z-source breaker in algorithm-based protection. Fig. 15(b) depicts that the voltage drops to zero during the occurrence of line-line fault where there's no impression of reverse recovery voltage by the breaker. The fault current is interrupted by adaptive algorithm and its corresponding breaker CB6 trips. On continuation to this fault, a line-to-line fault occurs at line 32 results in tripping of CB 3.

7.1.2 Performance under Line-Ground Faults

To validate the algorithm functionality with proposed breaker for Line to ground fault on the line L 1-2 were simulated, and the results have been discussed here. The corresponding relay senses the fault and the protection controller simultaneously act based on the results from active node algorithm in finding the active nodes.

Thereby, it determines the corresponding shortest path as 'Bus 2-1-common bus' which concludes the least distance as 2 and it is identified by shortest path algorithm. The fault current

contribution is shown in Fig. 15(b) resulting in summing up of total fault equals the sum of fault current produced by DGs. On comparing with simulation results, the fault current initially reaches the value of 400 A in a shorter period (within 10 ms), and it is further interrupted by circuit breaker CB2. The reclosing operation of breaker after interruption settles to a nominal value of 13A as shown in Fig. 15. The algorithm used in protection controller provides the running time to detect and interrupt the fault in few milliseconds (ms) by proposed modified z-source breaker with tuned parameters of L and C neglecting the voltage or current spikes caused by switching device. Hence the proposed breaker proves its efficacy in seven bus DC microgrid system networked with adaptive protection controller. From table 3 and 4, it is observed that, the results of DC microgrid with adaptive algorithm and LC tuned breaker acts faster than existing AC microgrid techniques. The feasibility is tested with two processors and the fault detection time is very less compared to AC microgrid.

Performance of breaker on occurrence line - line fault and line - ground fault

Table 3 Comparison of protection algorithms in literature for active bus identification [31-35]

Table 4 Comparison of protection algorithms in literature with proposed breaker for shortest path identification [31-35]

7.2 Implementation of Modified Z-Source Breaker in 50kW DC Microgrid System

The proposed 50 kW seven-bus DC microgrid system is outlined in Fig. 16. The Common bus/Point of common coupling (PCC), interconnected with the 20kW PV and DC-DC converter, facilitates connectivity with all buses within the grid. The transmission line separating each bus is standardized at one kilometre distance. Buses 1, 3, 5, and 7 are interfaced with resistive loads to distribute the generated power. Furthermore, bus 2 is interlinked with a bidirectional battery system of 5kWh energy storage, while bus 6 is equipped with a 25kW Permanent Magnet Synchronous Generator (PMSG) based Wind Energy Conversion System (WECS) and a rectifier to ensure effective interfacing. Under normal operating conditions, power flows from the common bus interfaced with PV towards Bus 5 in feeder 1 and from the common bus to bus 7 in feeder 2. In instances where PV power is unavailable, the battery discharges, thereby redirecting power flow from Bus 2 to Bus 1 via the common bus. R1 to R8 are overcurrent relays and CB1 to CB8 are modified z-source breaker. During normal operating

conditions, the simulation results of voltage, current, and power are 750V, 66.6A and 50kW respectively in the DC Grid, as depicted in Fig. 17 (a), (b) and (c).

Proposed 50 kW seven-bus DC microgrid system

Simulation results of Proposed 50 kW seven-bus DC microgrid system and its Grid Voltage, Grid Current and Grid Power

With the proposed breaker of tuned L and C values in the range of 0.1H and 0.01F, the work is carried out and the breaker is implemented and tested in 50kW DC microgrid system which works on 750V, 66A to prove the efficiency for high power applications. This work is examined in Software-in-the-loop (SIL) testing that provides a significant advantage by eliminating the need for external data transmission, thereby maintaining signal coherence. This section entails the testing of seven bus DC microgrid system interfaced with proposed breaker using a real-time (RT) simulator (OP4500) constructed on the RT-Lab environment. Simulink models of the seven-bus system integrated with PV, WECS, Battery, Loads and proposed breaker are amalgamated with Opcomm and Opctrl RT controller blocks, that are existing on the host computer connected to the OP4500 simulation target through a Transmission Control Protocol (TCP) / Internet Protocol (IP) communication network, as illustrated in Fig. 18. The voltage levels, at 750V and 66.6V, are constrained to reside within the range of +/-16V to comply with the real-time simulator compatibility requirements. Consequently, voltage gain of 1/50 applied to facilitate these adjustments. To scrutinize the system dynamics, a line-to-line fault F is introduced in transmission line between bus 3-4 to analyse the impact of the proposed breaker in the 50kW DC microgrid as shown in Fig. 19. The execution reveals that the proposed breaker topology in 50kW DC system has an efficiency of 98.27% and the CB4 breaker voltage trips and recloses in 6.399 milliseconds and 33.23 milliseconds as shown in Fig. 20. Similarly, the CB4 breaker current interrupts and recloses the fault at 6.400 and 4.250 milliseconds respectively with an insignificant spike due to the presence of switching device. Consequently, the breaker CB8 and CB 5 also interrupts for the fault F. With the obtained results from OPAL RT, the estimated efficiency of the breaker is estimated to be 98.27%.

Software in loop testing using Real-time simulator

Analysis of Line-to-Line Fault (F) in transmission line between Bus 3 and 4 in 50 kW seven-bus DC microgrid system

Interrupting and Reclosing of breaker CB4 due to the occurrence of Fault F in 50kW DC microgrid

8. Conclusion

The DC microgrid protection is a challenging mission owing to the adaptive microgrid network. The traditional protection strategy is not appropriate for DC networks as they result in false tripping and blinding of protection. Incorporating adaptive techniques in existing z- source breaker topology, is the emerging trend in breaker designs. The voltage stress on the breaker is analysed, and tuned values of L and C are employed to decrease the stress on the switching device. At last, the new modified z source breaker is verified in 400V/5kW low-scale renewable integrated DC microgrid with adaptive algorithms to validate the design process of the new z source circuit breaker. The adaptive protection algorithm determines the least distance path between a faulted point to the closest distributed generation with the help of real time processor using Python scripts. This algorithm clears the fault with minimum load disconnection and the efficiency of the proposed algorithm is verified with existing algorithm by CHIL in real time simulator for various faults such as bus faults, line to line faults and line to ground fault. Furthermore, the proposed breaker with tuned LC values proves that the adaptivity and viability of different fault types in the DC microgrid network. The modified new Z source with high fault interrupting capability is subjected to Prims - Dijkstra algorithm, thereby exhibiting minimal detection and interruption time period of 252μs when compared with the existing algorithm in the literature. Additionally, the efficiency is verified through testing the modified new Z source breaker in a 50-kW system under line-to-line fault conditions, demonstrating the viability of the breaker. The execution reveals that the modified Z source breaker topology has an efficiency of 98.27% and the breaker voltage trips and recloses in 6.399 milliseconds and 33.23 milliseconds respectively. The breaker current trips in 6.400 milliseconds and recloses in 4.250 milliseconds. On implementation in a 5-kW system, the efficiency stands at 99.2%, whereas in a 50-kW system, it is calculated as 98.27%. Thus, the above suggested breaker with adaptive algorithm can be applied to other DC microgrid configurations as future extension of work, due its supremacy and robustness towards variable operating conditions. This research work was carried out in opal RT platform in smart grid laboratory at Vellore institute of Technology.

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Figure Captions

Fig. 1. Conventional Z-source breaker topology [9]

Fig. 2. Inductor based Breaker modelling [13]

Fig. 3. New Z-source Breaker modelling [26]

Fig. 4. Single diode model of PV cell [27]

Fig. 5. Fixed speed direct-drive wind turbine with a permanent magnet synchronous generator (PMSG) [28]

Fig. 6. Framework of DC microgrid

Fig. 7. (a)Voltage, (b)Power and (c)Current results of seven bus DC system and also (d)Voltage and current of existing Z-source breaker during faulted period

Fig. 8. (a)New z source breaker topology [20] and (b)Current flow of new z source breaker when SCR is turned off

Fig. 9. (a)Voltage and (b)Current stress during fault occurrence and reclosing operation of new z source breaker

Fig. 10. Modes of operation of modified new z -source breaker for reducing voltage stress during (a)Normal conduction mode, (b) fault instant, (c) commutation of T1 and T2 and (d)capacitor precharging circuit

Fig. 11. During fault, (a) Peak fault current with respect to SCR current and (b)current flow in Z-source components

Fig. 12. Different combination of L and C values for reducing voltage stress during reclosing operation of modified new z -source breaker when (a) Fixing L value as $1e^{-1}$and varying C, (b) Fixing L value as $1e^{-2}$, and varying C, (c) Fixing C value as $1e^{-1}$ and varying L, (d) Fixing C value as $1e^{-2}$, and varying L

Fig. 13. Experimental setup on implementation of adaptive algorithm with modified new z-source breaker

Fig. 14. Faulted Path on occurrence of Line-to-Line Fault in Seven bus DC Microgrid

Fig. 15. Performance of breaker on occurrence (a) line - line fault and (b) line - ground fault

Fig. 16. Proposed 50 kW seven-bus DC microgrid system

Fig. 17. Simulation results of Proposed 50 kW seven-bus DC microgrid system and its (a)Grid Voltage, (b)Grid Current and (c)Grid Power

Fig. 18. Software in loop testing using Real-time simulator

Fig. 19. Analysis of Line-to-Line Fault (F) in transmission line between Bus 3 and 4 in 50 kW seven-bus DC microgrid system

Fig. 20. Interrupting and Reclosing of breaker CB4 due to the occurrence of Fault F in 50kW DC microgrid

Table captions

Table 1 Different combination of l and c values for reducing voltage stress during reclosing operation of modified new z -source breaker

Table 2 Breaker comparison

Table 3 Comparison of protection algorithms in literature for active bus identification [31-35]

Table 4 Comparison of protection algorithms in literature with proposed breaker for shortest path identification [31-35]

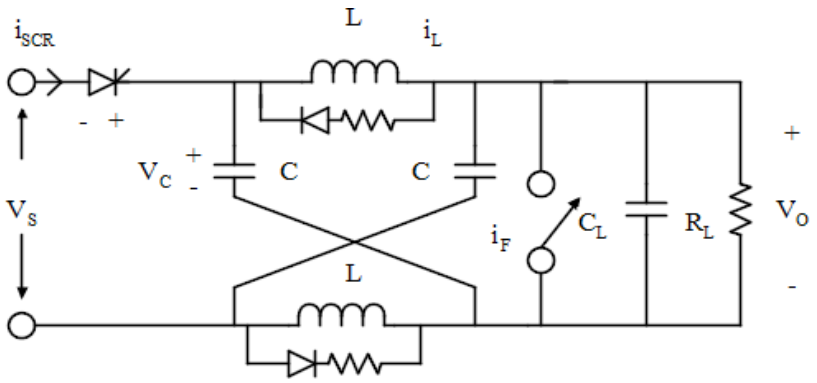


Fig. 1

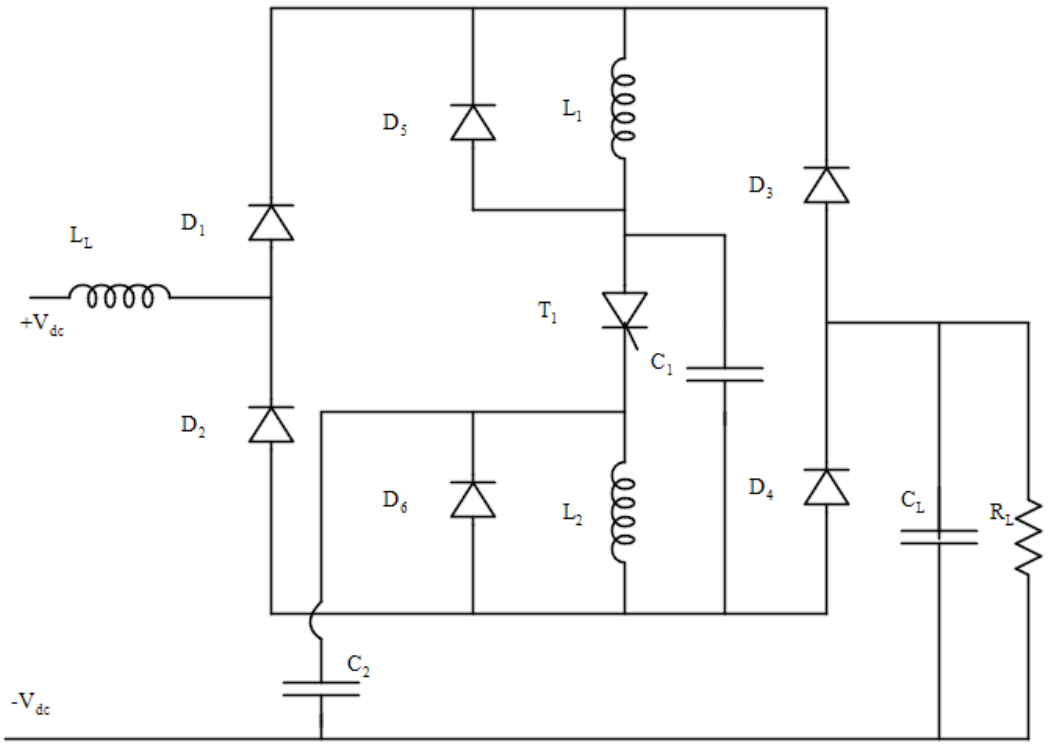


Fig. 2

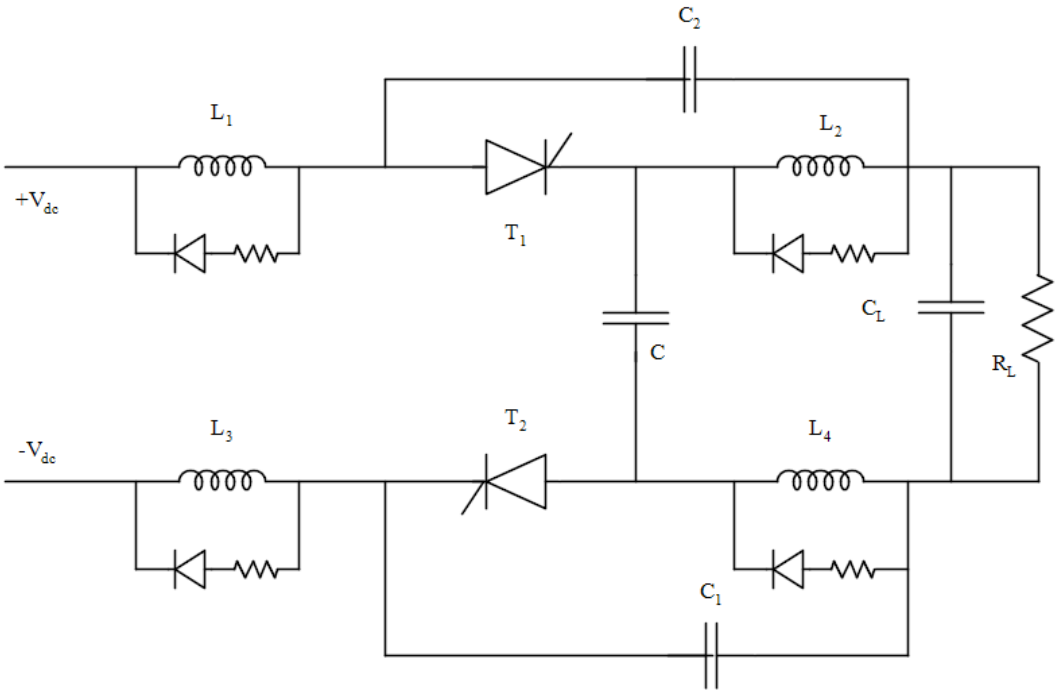


Fig. 3

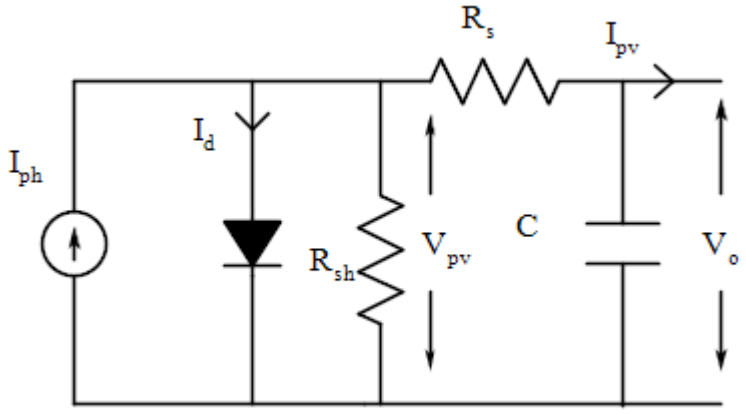


Fig. 4

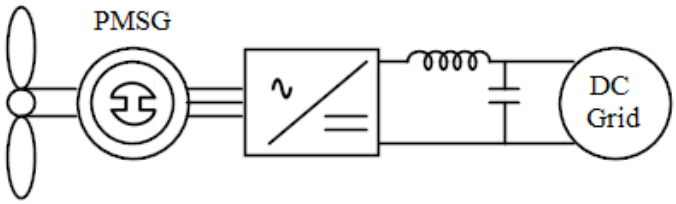

PMSG
DC
Grid

Fig. 5

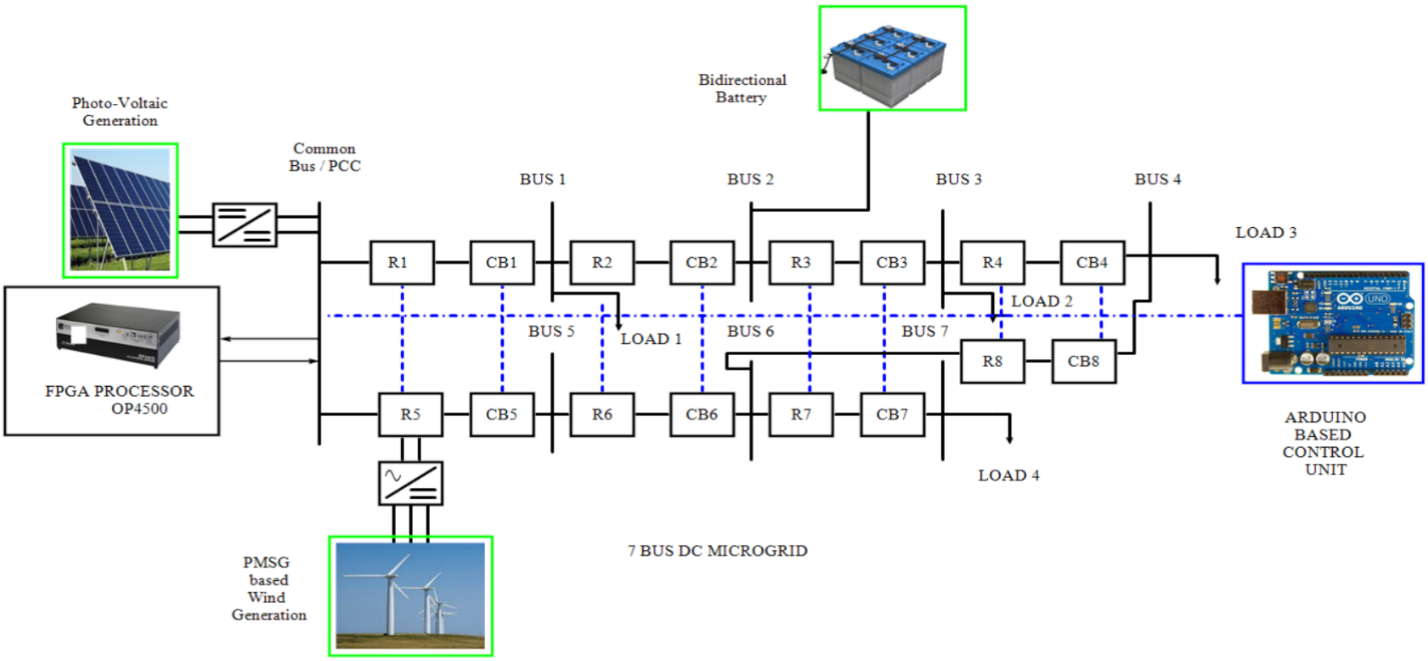
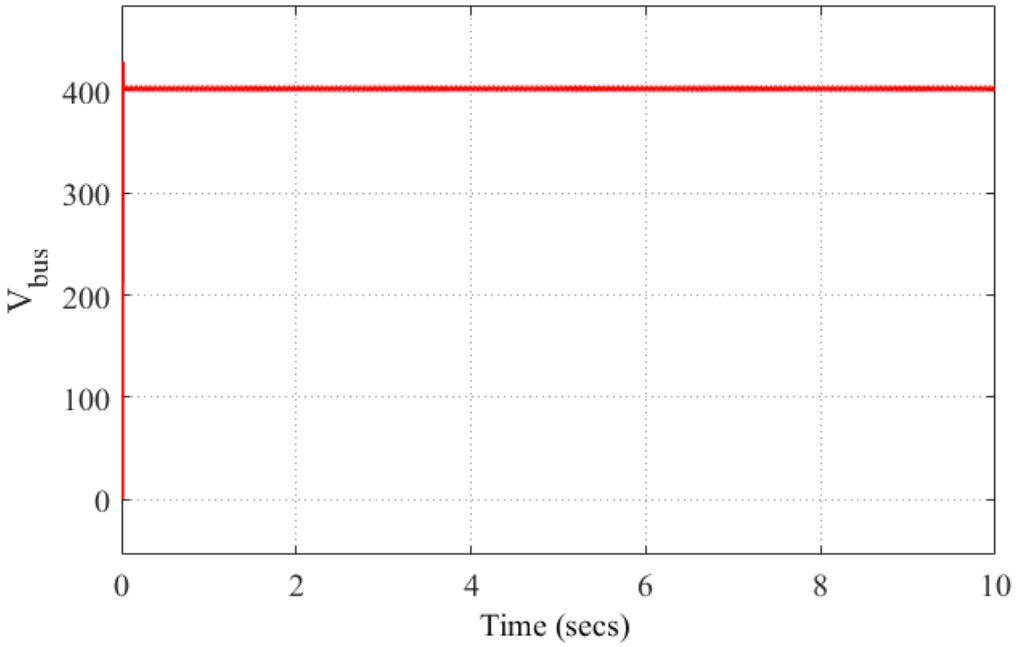
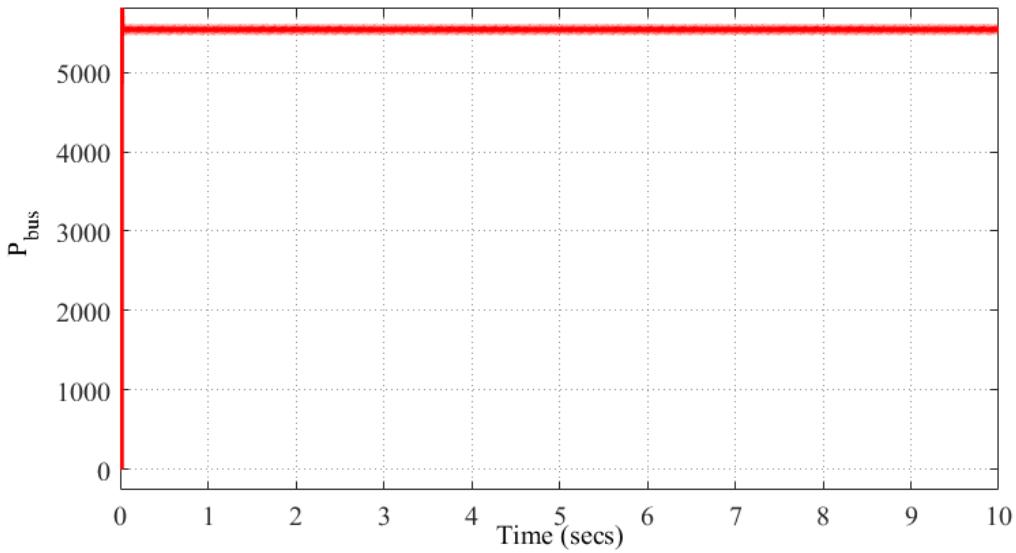


Photo-Voltaic
Generation
Common
Bus / PCC
Bidirectional
Battery
BUS 1
BUS 2
BUS 3
BUS 4
LOAD 3
R1
CB1
R2
CB2
R3
CB3
R4
CB4
LOAD 2
BUS 5
LOAD 1
BUS 6
BUS 7
R8
CB8
FPGA PROCESSOR
OP4500
R5
CB5
R6
CB6
R7
CB7
LOAD 4
ARDUINO
BASED
CONTROL
UNIT
PMSG
based
Wind
Generation
7 BUS DC MICROGRID

Fig. 6

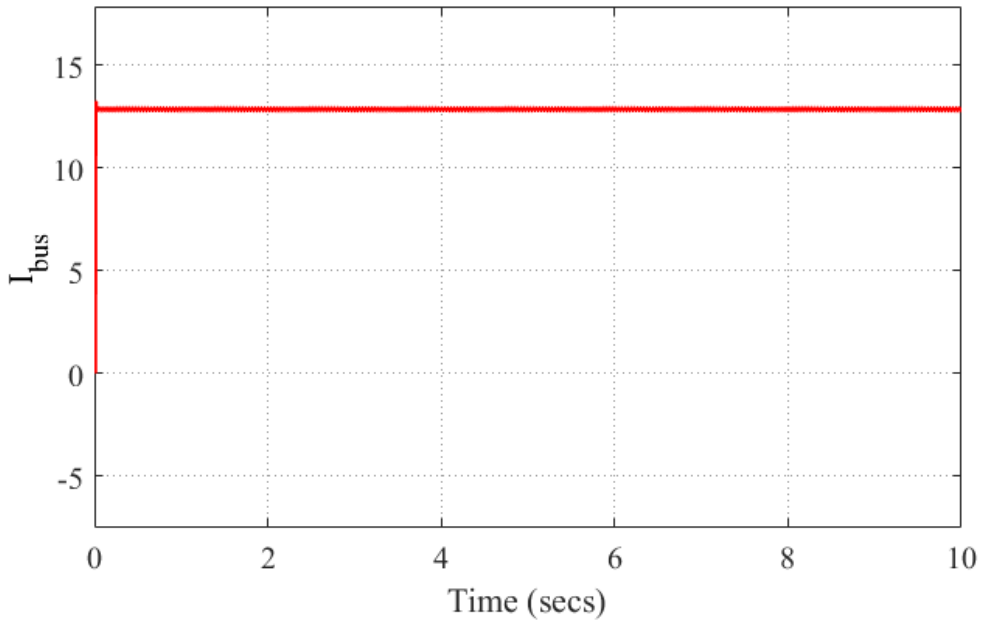

400
300
200
100
0
V_{bus}
0
2
4
6
8
10
Time (secs)

(a)

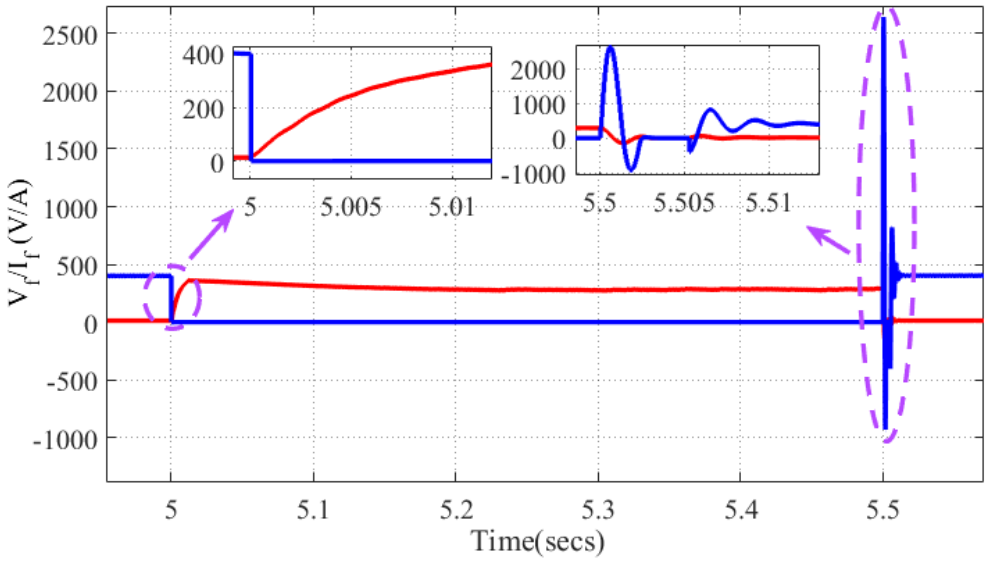

5000
4000
3000
2000
1000
0
P_{bus}
0
1
2
3
4
5
6
7
8
9
10
Time (secs)

(b)

Fig 7

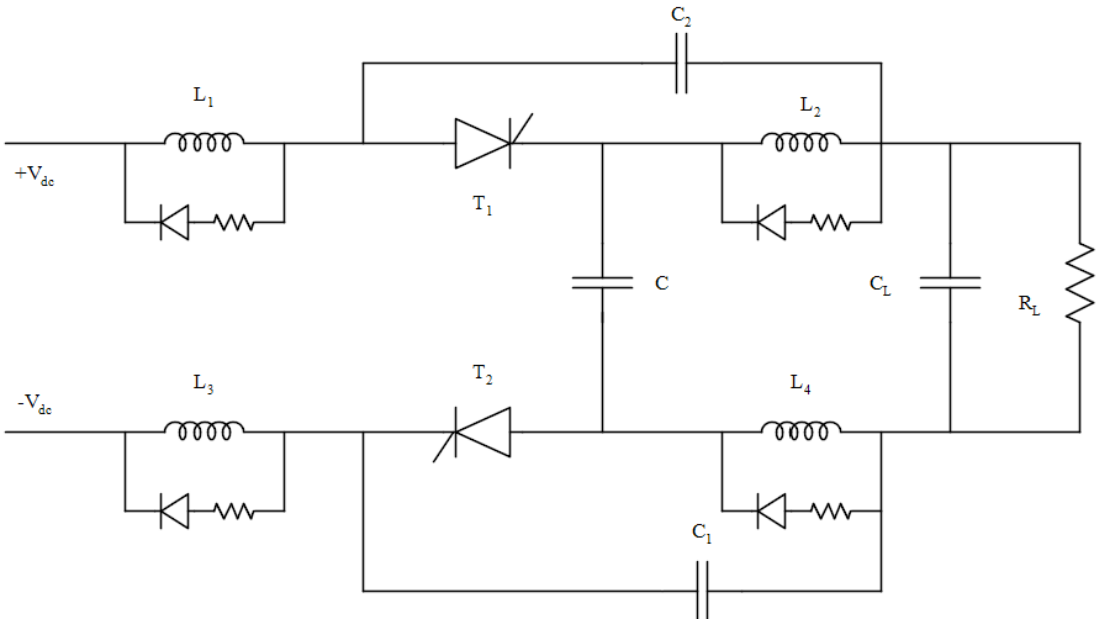

15
10
5
0
-5
I_{bus}
0
2
4
6
8
10
Time (secs)

(c)

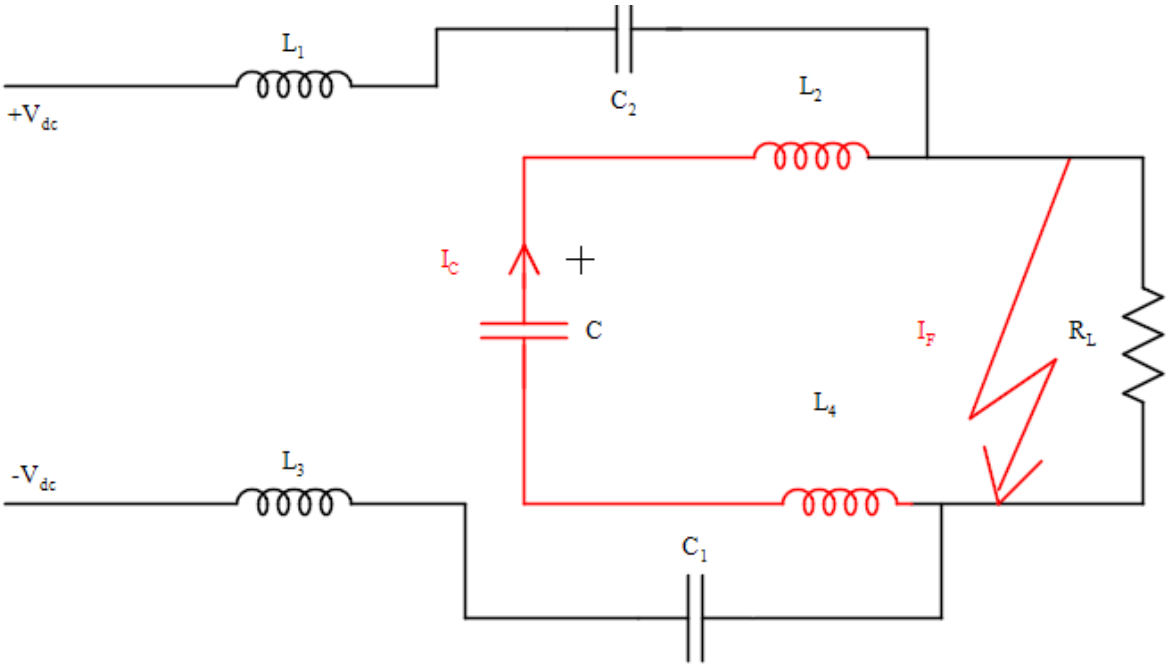

2500
2000
1500
1000
500
0
-500
-1000
V_f/I_f (V/A)
400
200
0
5
5.005
5.01
2000
1000
0
-1000
5.5
5.505
5.51
5
5.1
5.2
5.3
5.4
5.5
Time(secs)

(d)

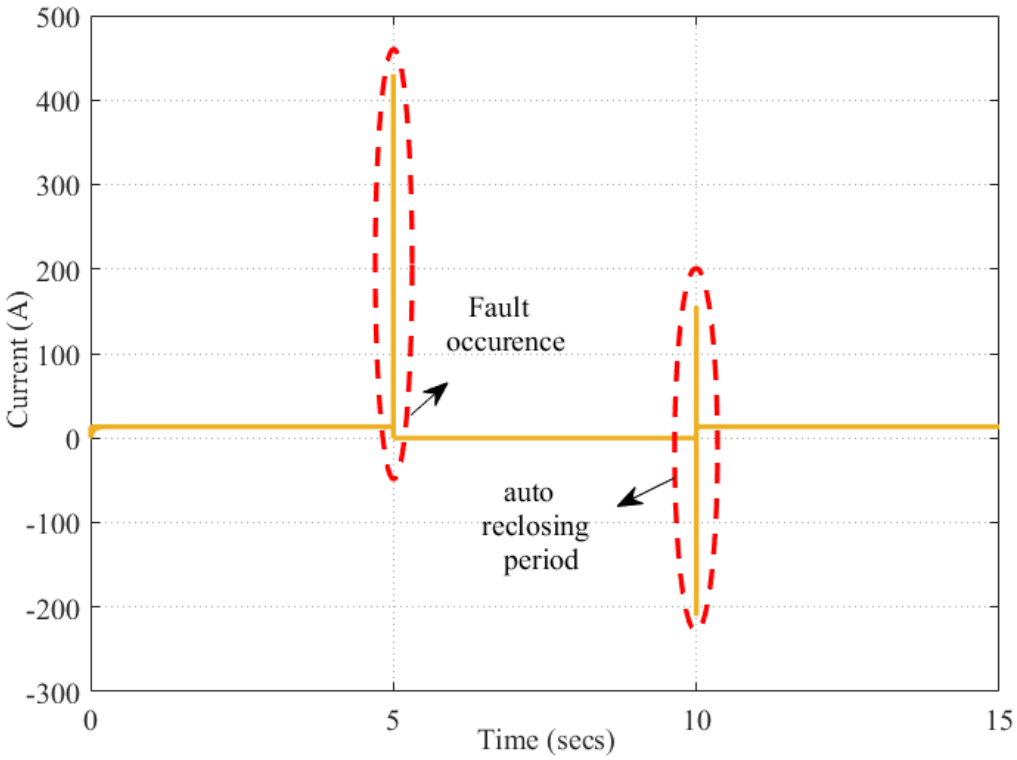
Fig 7


C2
L1
L2
+Vdc
T1
C
CL
RL
T2
L3
L4
-Vdc
C1

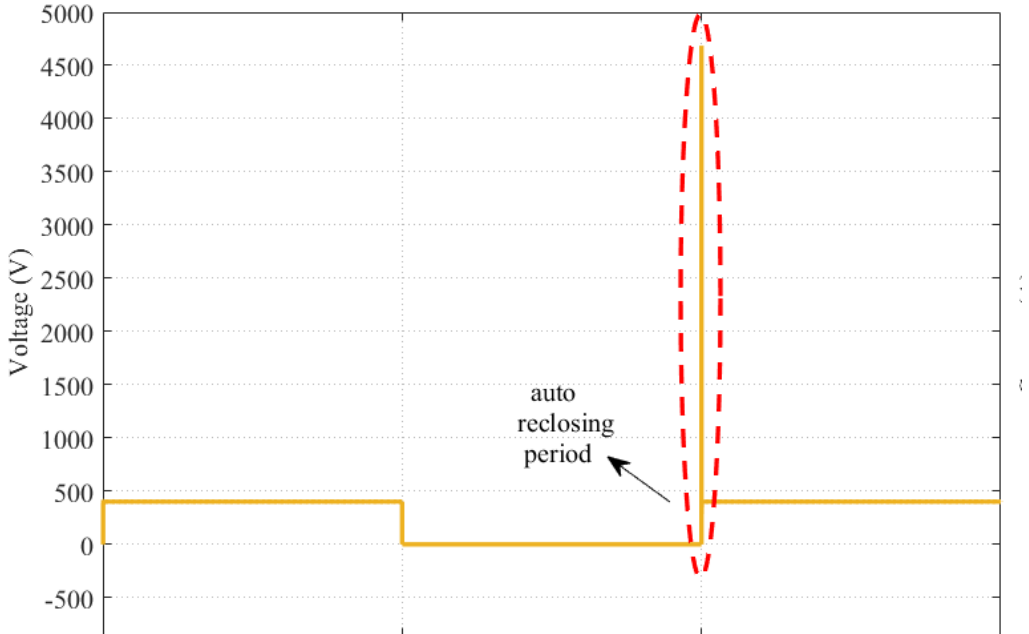
(a)


L1
C2
L2
+Vdc
IC
+
C
IF
RL
L4
-Vdc
L3
C1

(b)


500
400
300
200
100
0
-100
-200
-300
Current (A)
0
5
10
15
Time (secs)
Fault
occurence
auto
reclosing
period

(a)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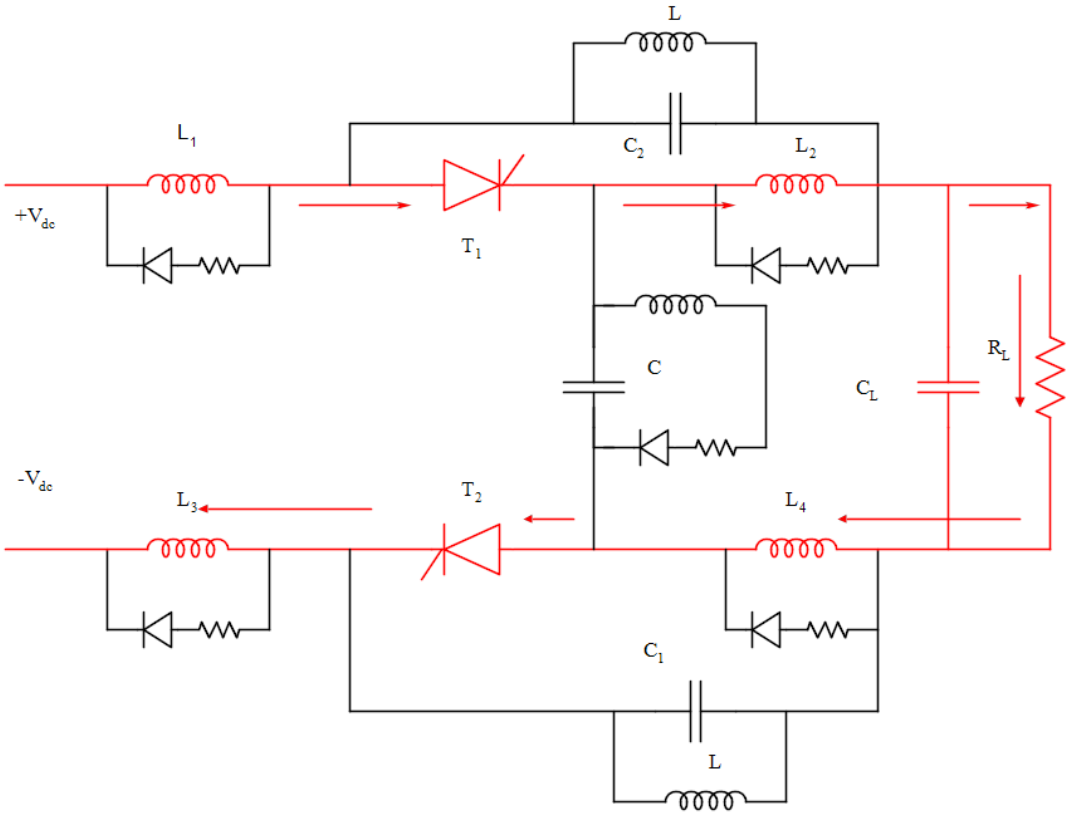
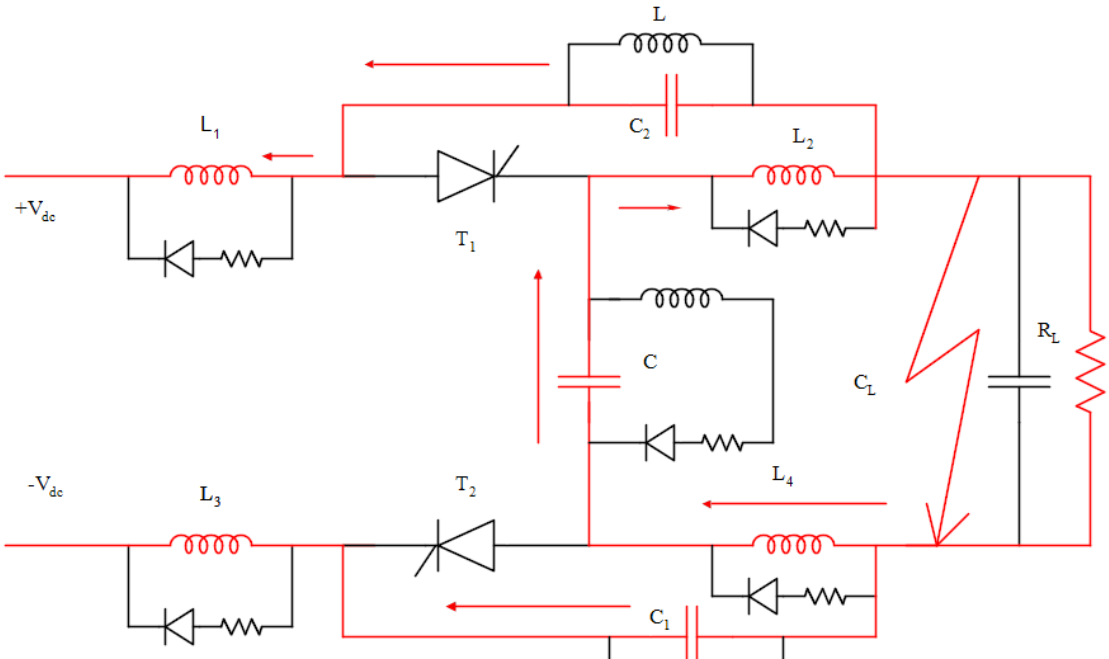
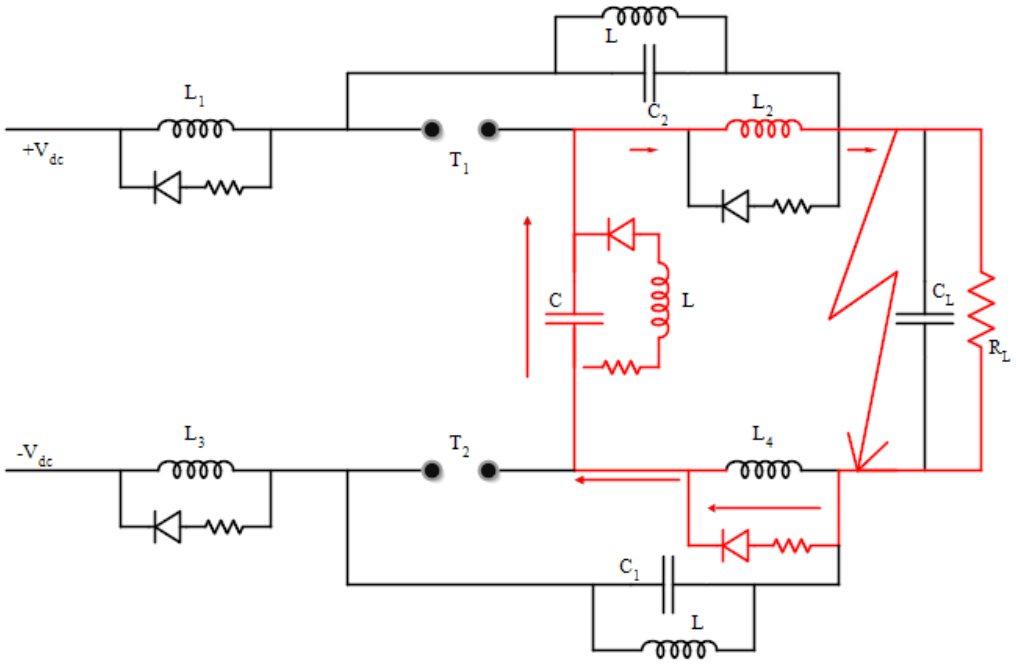
4500
4000
3500
3000
2500
2000
1500
1000
500
0
-500
Voltage (V)
auto
reclosing
period

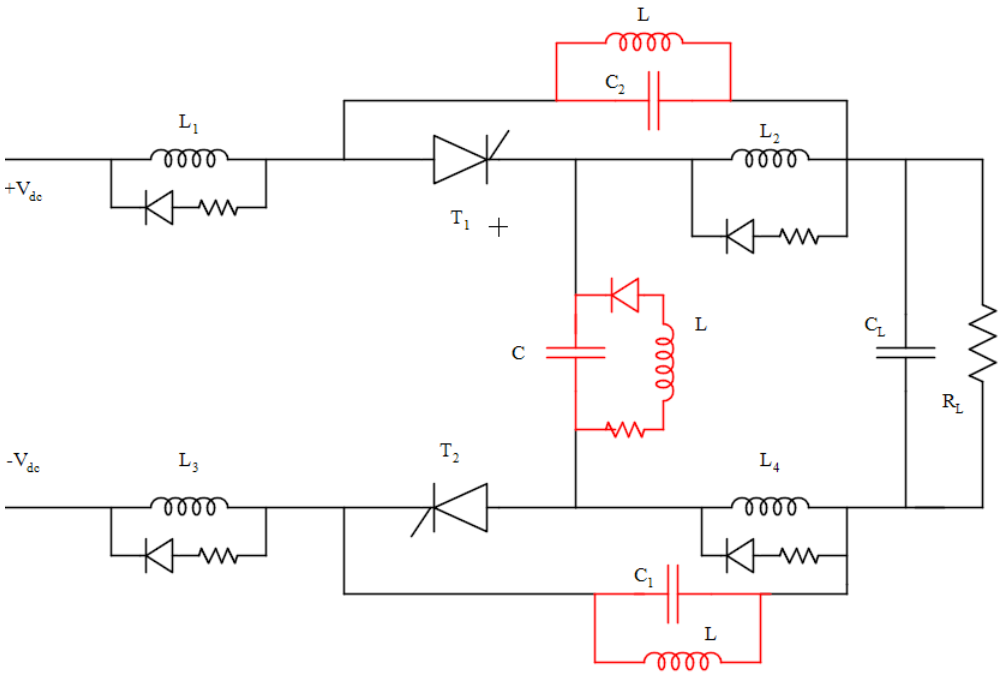

L
L1
C2
L2
+Vdc
T1
C
RL
CL
-Vdc
L3
T2
L4
C1
L

(a)

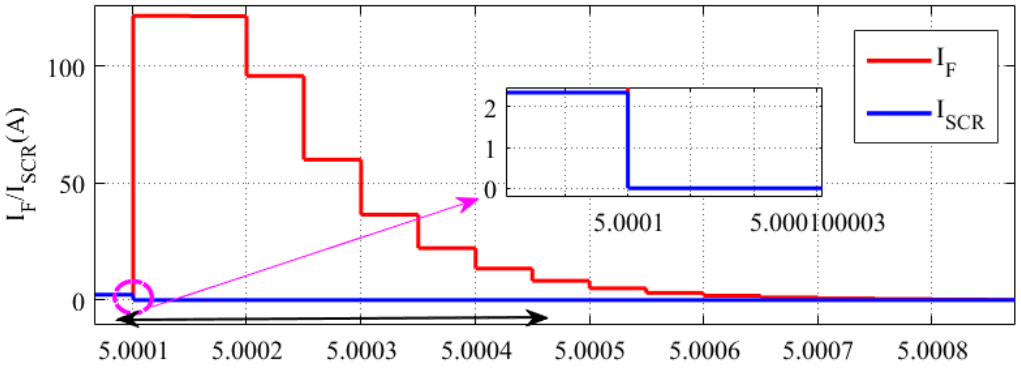

L
L1
C2
L2
+Vdc
T1
C
RL
CL
-Vdc
L3
T2
L4
C1


L
C2
L1
L2
+Vdc
T1
C
L
CL
RL
-Vdc
L3
T2
L4
C1
L

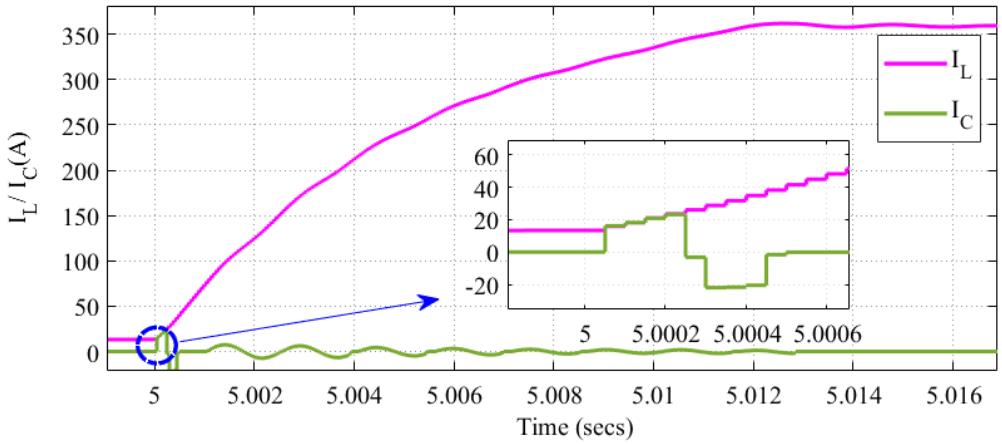
(c)


L
C2
L1
L2
+Vdc
T1
C
L
CL
RL
-Vdc
L3
T2
L4
C1
L

(d)


100
50
0
I_F/I_{SCR}(A)
2
1
0
5.0001
5.000100003
I_F
I_{SCR}
5.0001
5.0002
5.0003
5.0004
5.0005
5.0006
5.0007
5.0008

(a)


350
300
250
200
150
100
50
0
I_L / I_C(A)
60
40
20
0
-20
5
5.0002
5.0004
5.0006
I_L
I_C
5
5.002
5.004
5.006
5.008
5.01
5.012
5.014
5.016
Time (secs)

(b)

Fig. 11

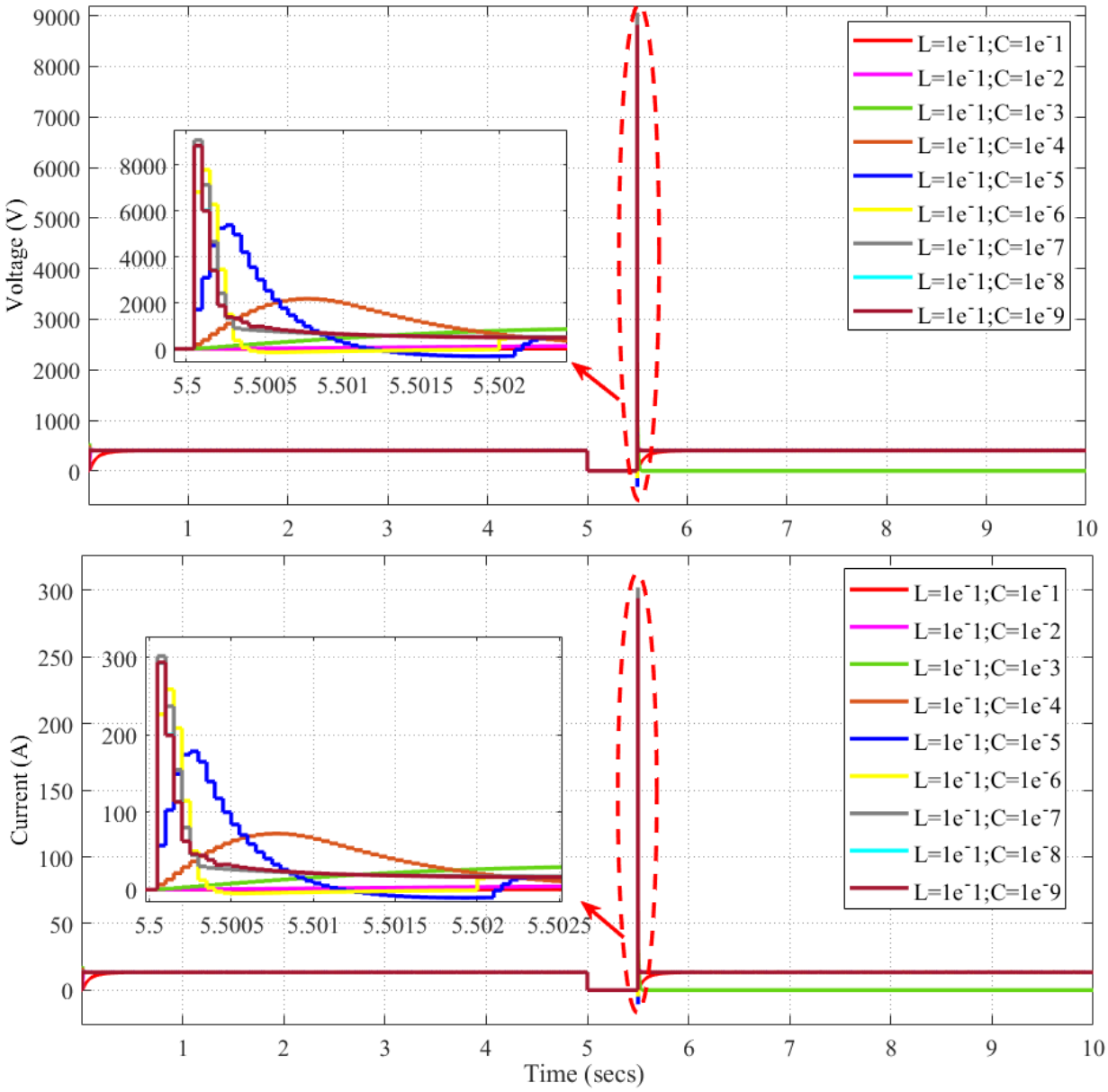
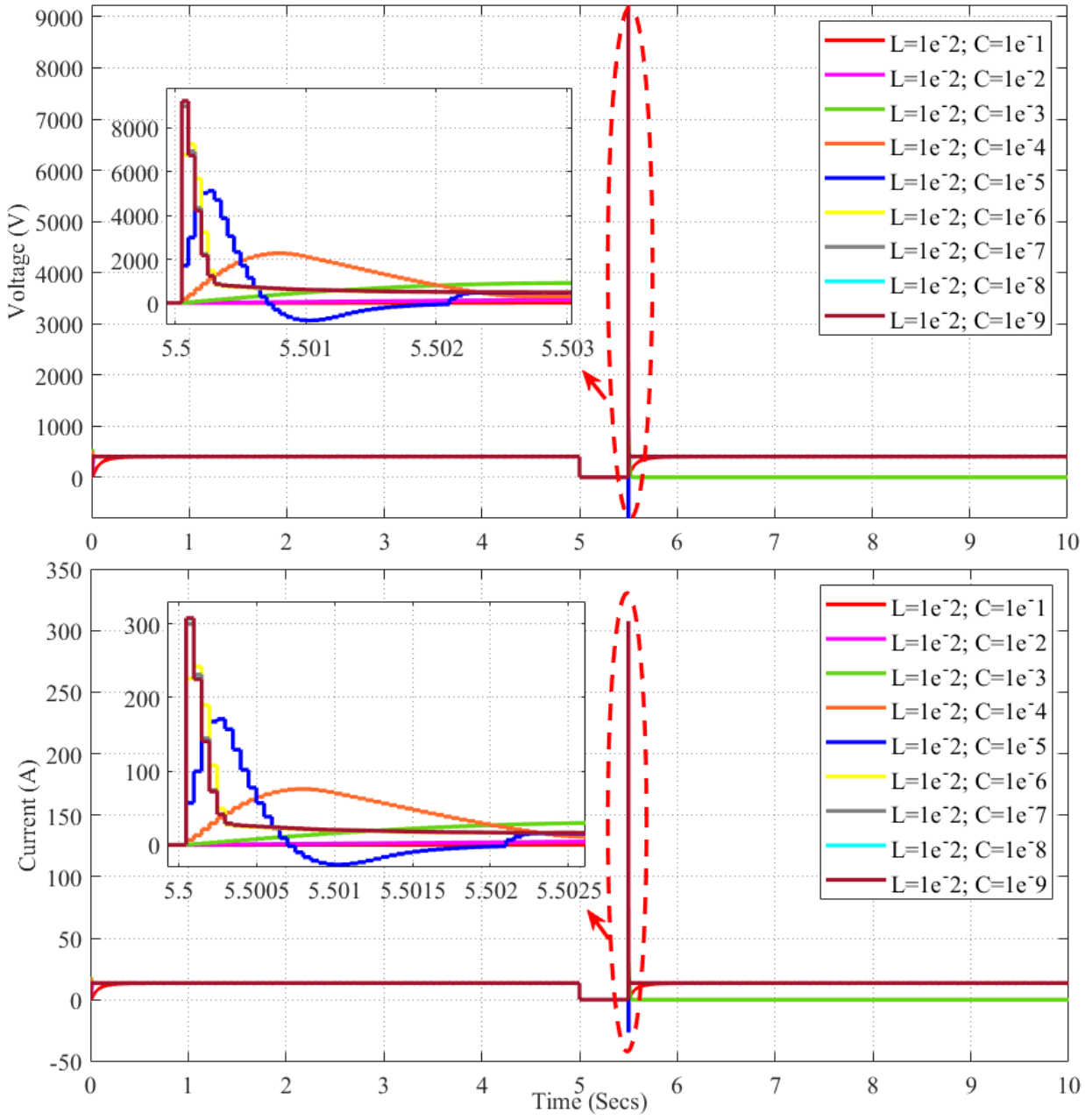
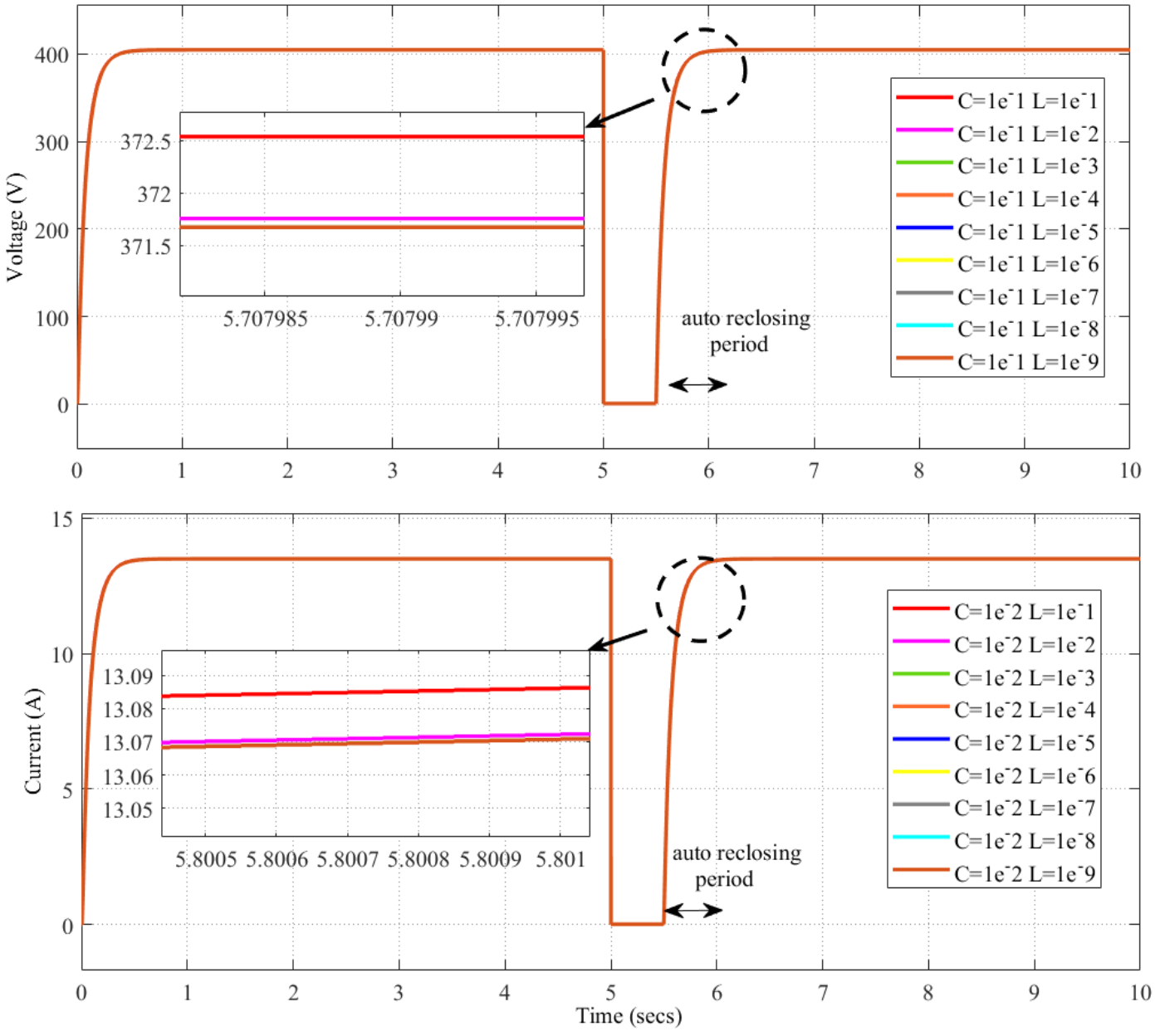

Voltage (V)
Current (A)
Time (secs)
L=1e-1;C=1e-1
L=1e-1;C=1e-2
L=1e-1;C=1e-3
L=1e-1;C=1e-4
L=1e-1;C=1e-5
L=1e-1;C=1e-6
L=1e-1;C=1e-7
L=1e-1;C=1e-8
L=1e-1;C=1e-9

Fig. 12 (a)


Voltage (V)
Current (A)
Time (Secs)
L=1e-2; C=1e-1
L=1e-2; C=1e-2
L=1e-2; C=1e-3
L=1e-2; C=1e-4
L=1e-2; C=1e-5
L=1e-2; C=1e-6
L=1e-2; C=1e-7
L=1e-2; C=1e-8
L=1e-2; C=1e-9

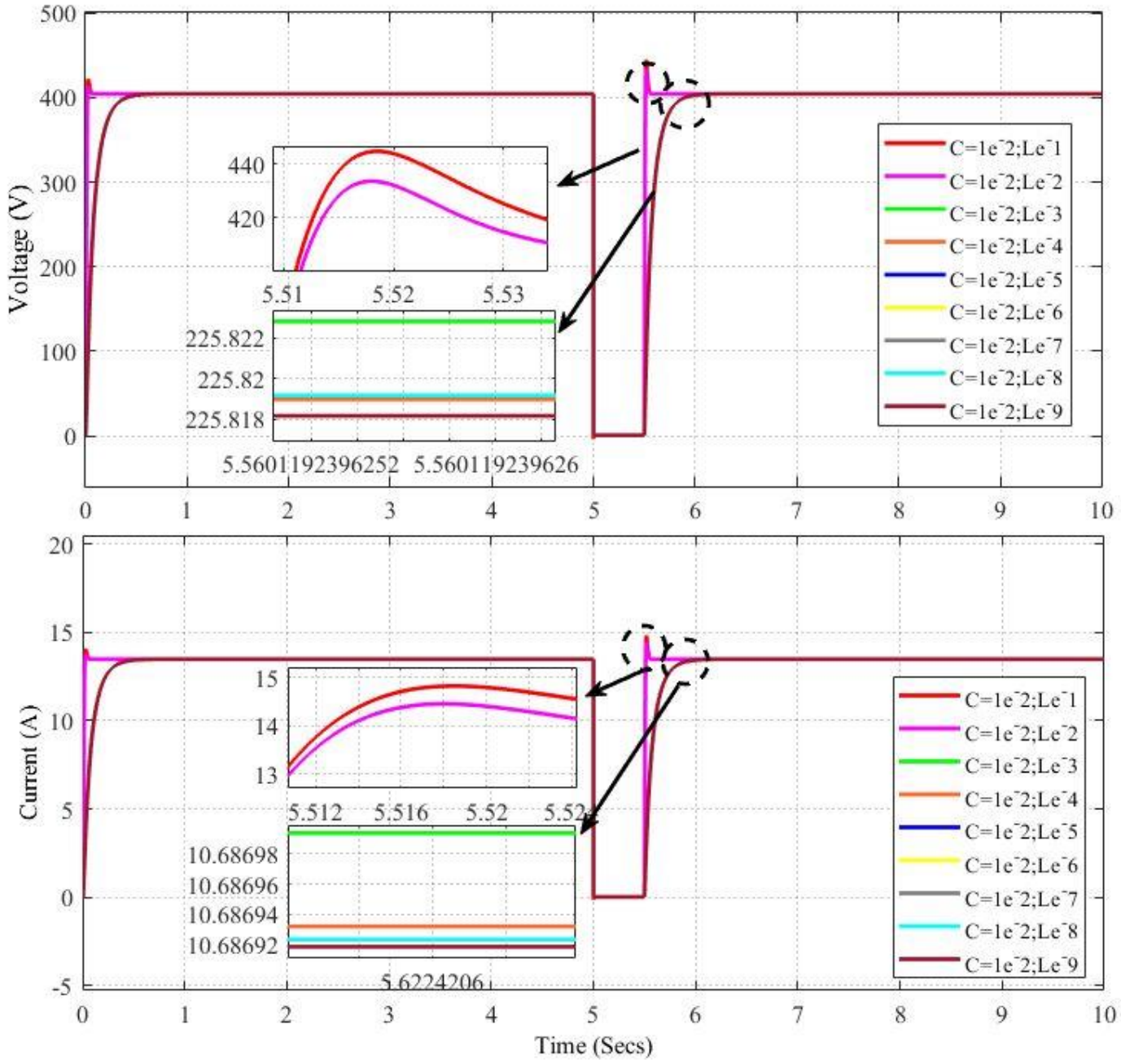
(b)

Fig. 12 (b)


Voltage (V)
400
300
200
100
0
372.5
372
371.5
5.707985
5.70799
5.707995
auto reclosing
period
C=1e-1 L=1e-1
C=1e-1 L=1e-2
C=1e-1 L=1e-3
C=1e-1 L=1e-4
C=1e-1 L=1e-5
C=1e-1 L=1e-6
C=1e-1 L=1e-7
C=1e-1 L=1e-8
C=1e-1 L=1e-9
0 1 2 3 4 5 6 7 8 9 10
Current (A)
15
10
5
0
13.09
13.08
13.07
13.06
13.05
5.8005 5.8006 5.8007 5.8008 5.8009 5.801
auto reclosing
period
C=1e-2 L=1e-1
C=1e-2 L=1e-2
C=1e-2 L=1e-3
C=1e-2 L=1e-4
C=1e-2 L=1e-5
C=1e-2 L=1e-6
C=1e-2 L=1e-7
C=1e-2 L=1e-8
C=1e-2 L=1e-9
0 1 2 3 4 5 6 7 8 9 10
Time (secs)

(c)

Fig. 12 (c)


Voltage (V)
Current (A)
Time (Secs)
C=1e-2;Le-1
C=1e-2;Le-2
C=1e-2;Le-3
C=1e-2;Le-4
C=1e-2;Le-5
C=1e-2;Le-6
C=1e-2;Le-7
C=1e-2;Le-8
C=1e-2;Le-9
440
420
5.51
5.52
5.53
225.822
225.82
225.818
5.5601192396252
5.560119239626
15
14
13
5.512
5.516
5.52
10.68698
10.68696
10.68694
10.68692
5.6224206

(d)

Fig. 12 (d)

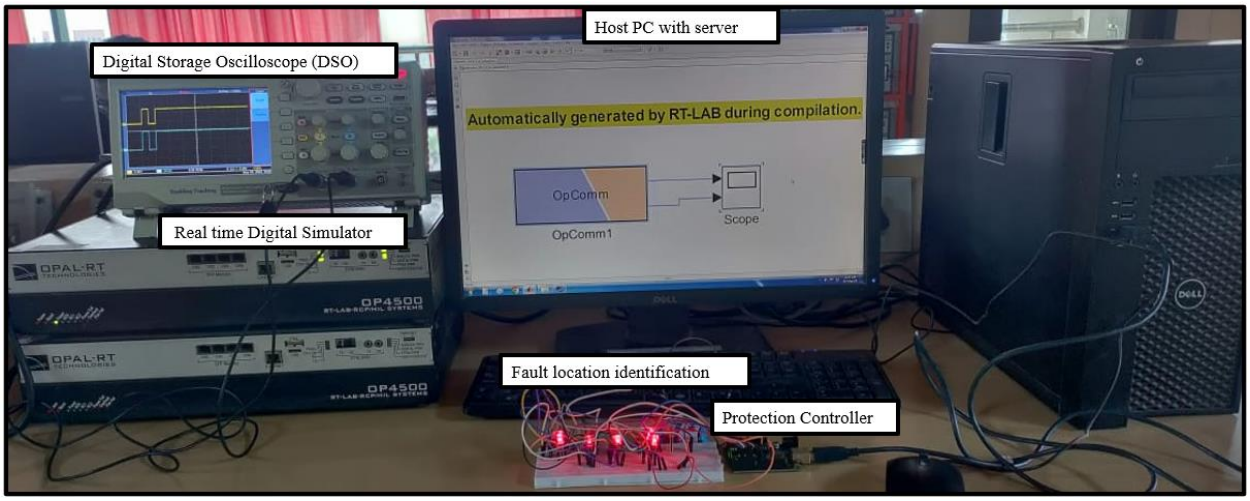

Host PC with server
Digital Storage Oscilloscope (DSO)
Automatically generated by RT-LAB during compilation.
OpComm
OpComm1
Scope
Real time Digital Simulator
OPAL-RT
OP4500
Fault location identification
Protection Controller

Fig. 13

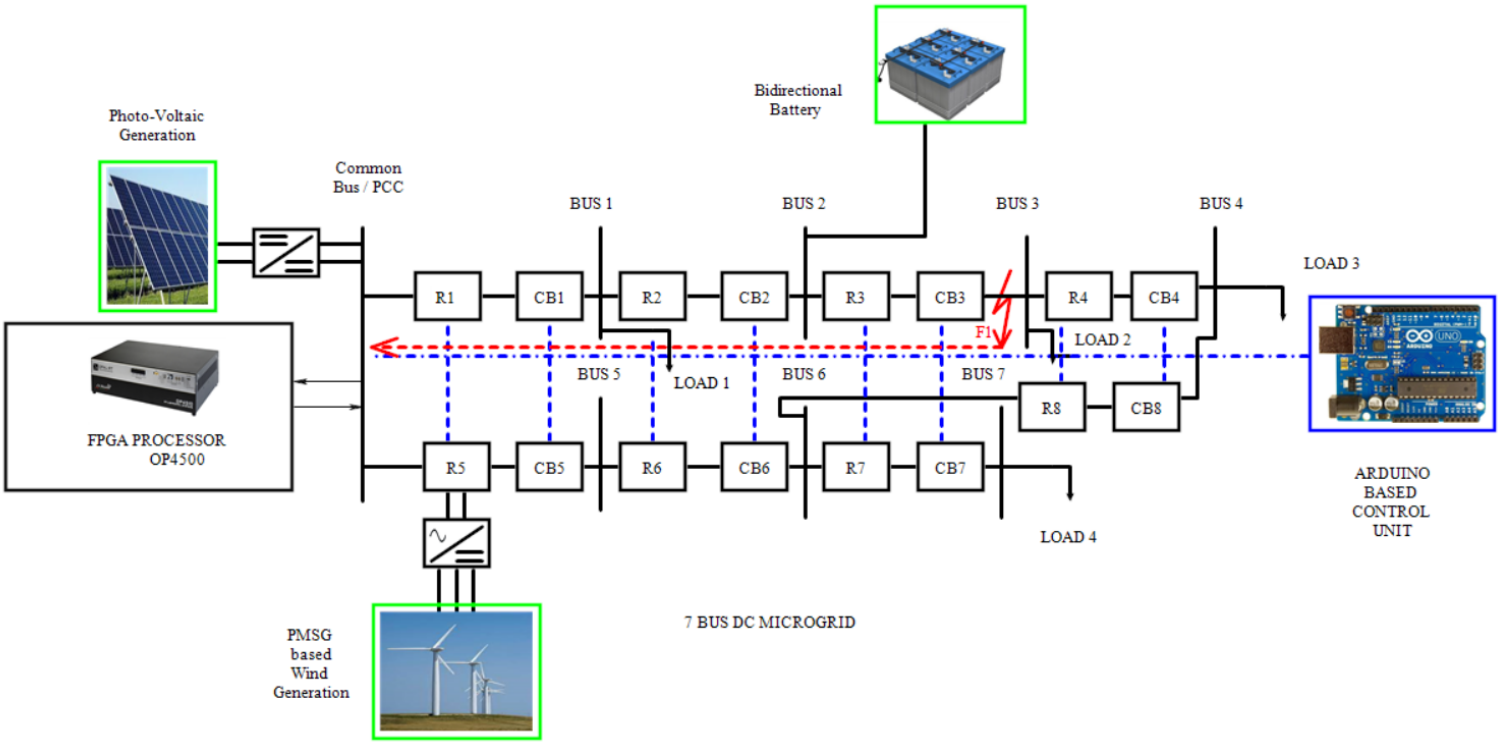


Photo-Voltaic Generation
Common Bus / PCC
Bidirectional Battery
BUS 1
BUS 2
BUS 3
BUS 4
LOAD 3
R1
CB1
R2
CB2
R3
CB3
R4
CB4
F1
LOAD 2
BUS 5
LOAD 1
BUS 6
BUS 7
R8
CB8
FPGA PROCESSOR OP4500
R5
CB5
R6
CB6
R7
CB7
LOAD 4
ARDUINO BASED CONTROL UNIT
PMSG based Wind Generation
7 BUS DC MICROGRID

Fig. 14

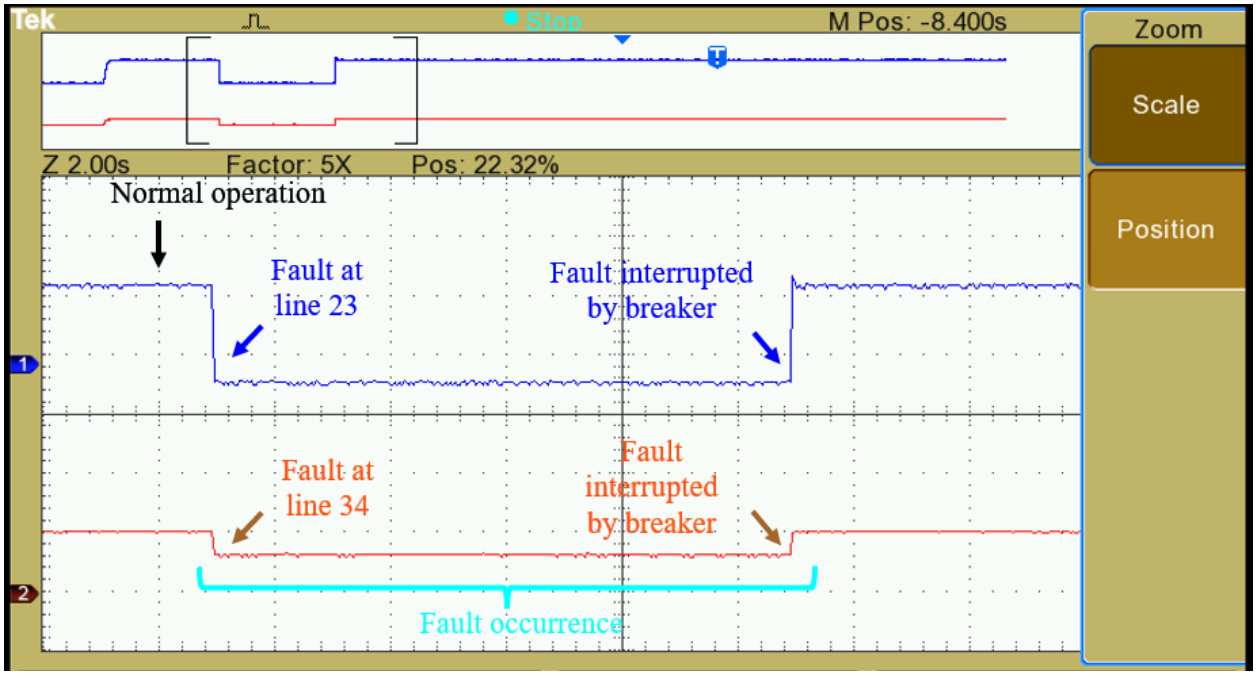


Fig. 15 (a)

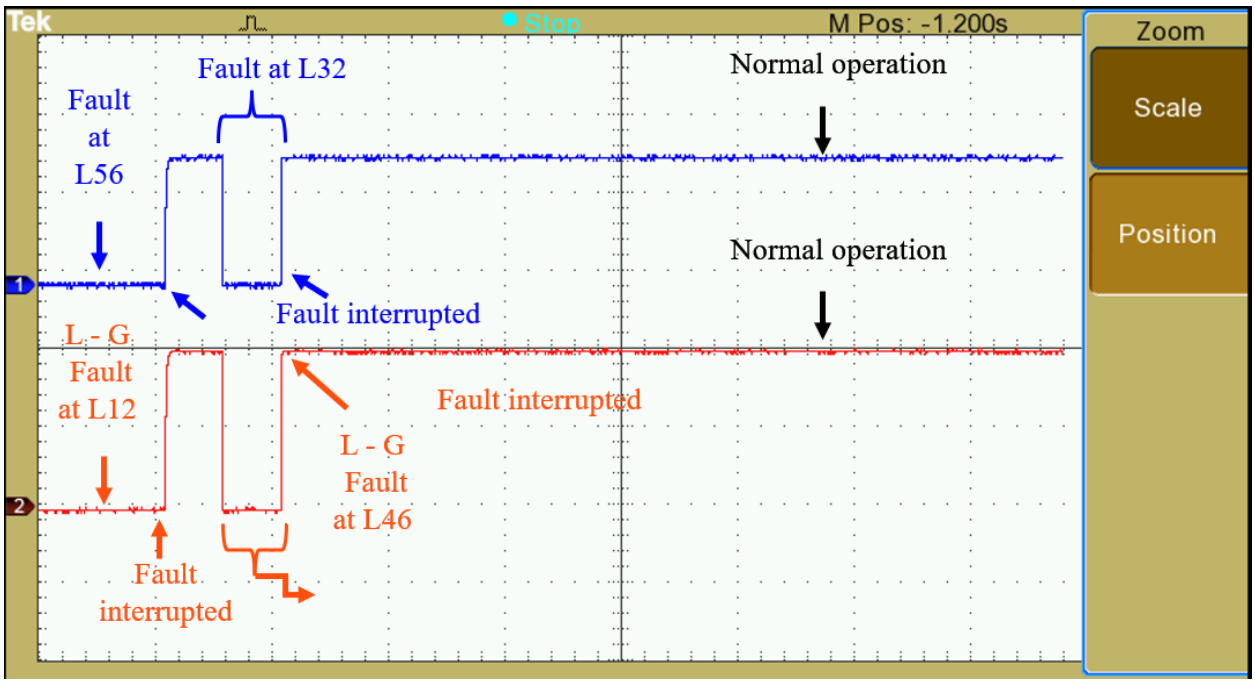


Fig. 15 (b)

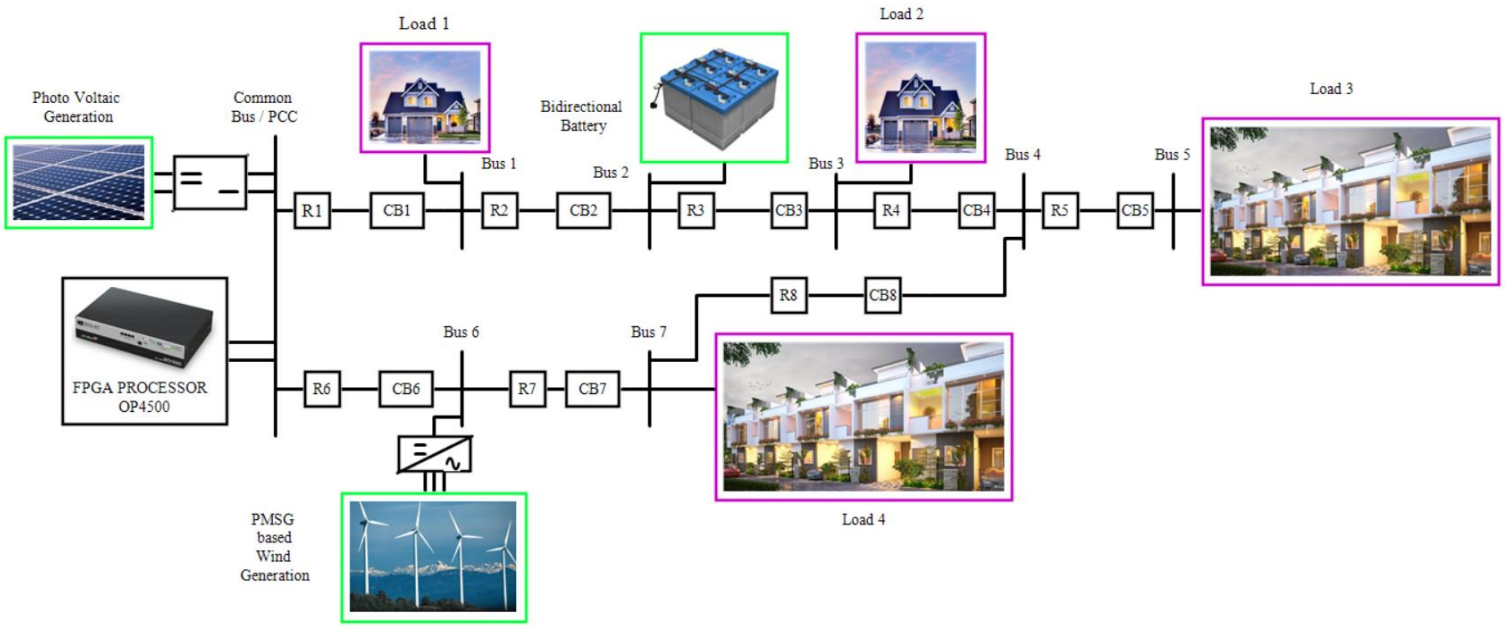
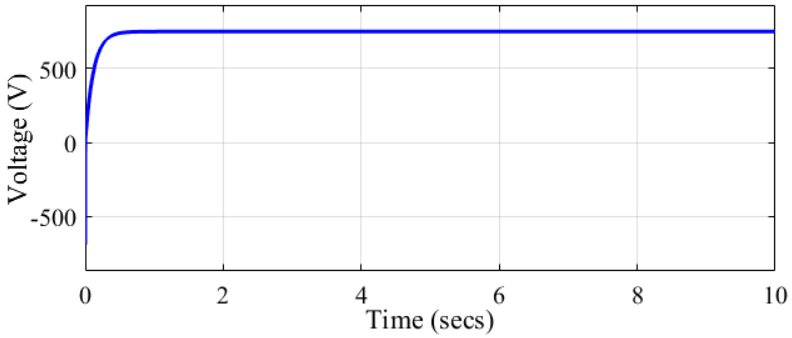
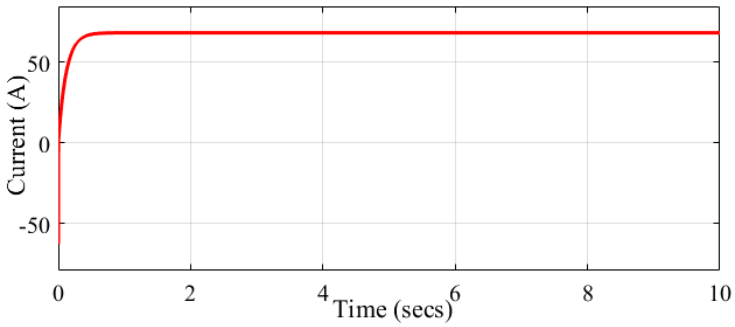

Load 1
Load 2
Load 3
Photo Voltaic Generation
Common Bus / PCC
Bidirectional Battery
Bus 1
Bus 2
Bus 3
Bus 4
Bus 5
R1
CB1
R2
CB2
R3
CB3
R4
CB4
R5
CB5
R8
CB8
FPGA PROCESSOR OP4500
Bus 6
Bus 7
R6
CB6
R7
CB7
PMSG based Wind Generation
Load 4

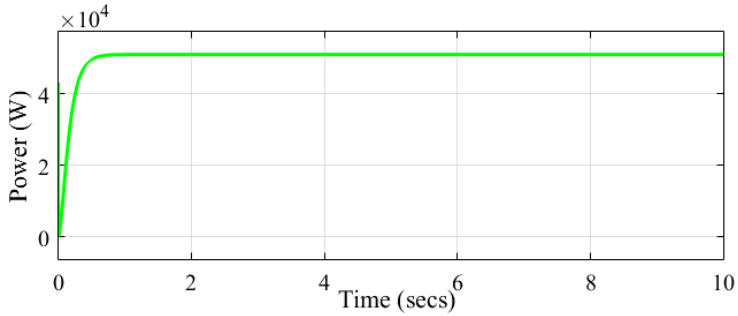
Fig. 16


Voltage (V)
500
0
-500
0
2
4
6
8
10
Time (secs)

(a)


Current (A)
50
0
-50
0
2
4
6
8
10
Time (secs)

(b)


×10^4
Power (W)
4
2
0
0
2
4
6
8
10
Time (secs)

(c)

Fig 17

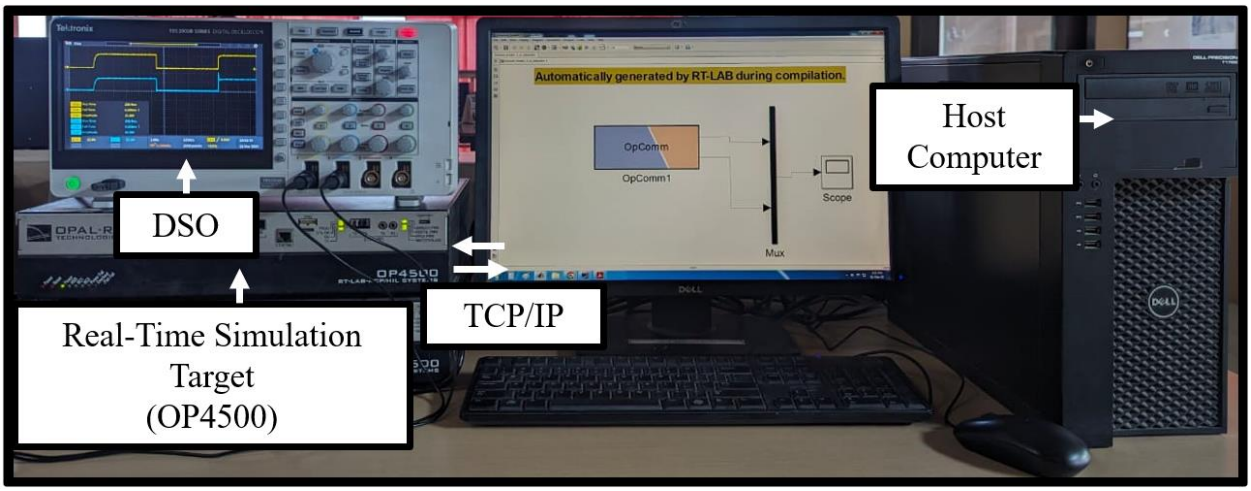

DSO
Real-Time Simulation Target (OP4500)
TCP/IP
Host Computer
Automatically generated by RT-LAB during compilation.
OpComm
OpComm1
Mux
Scope

Fig. 18

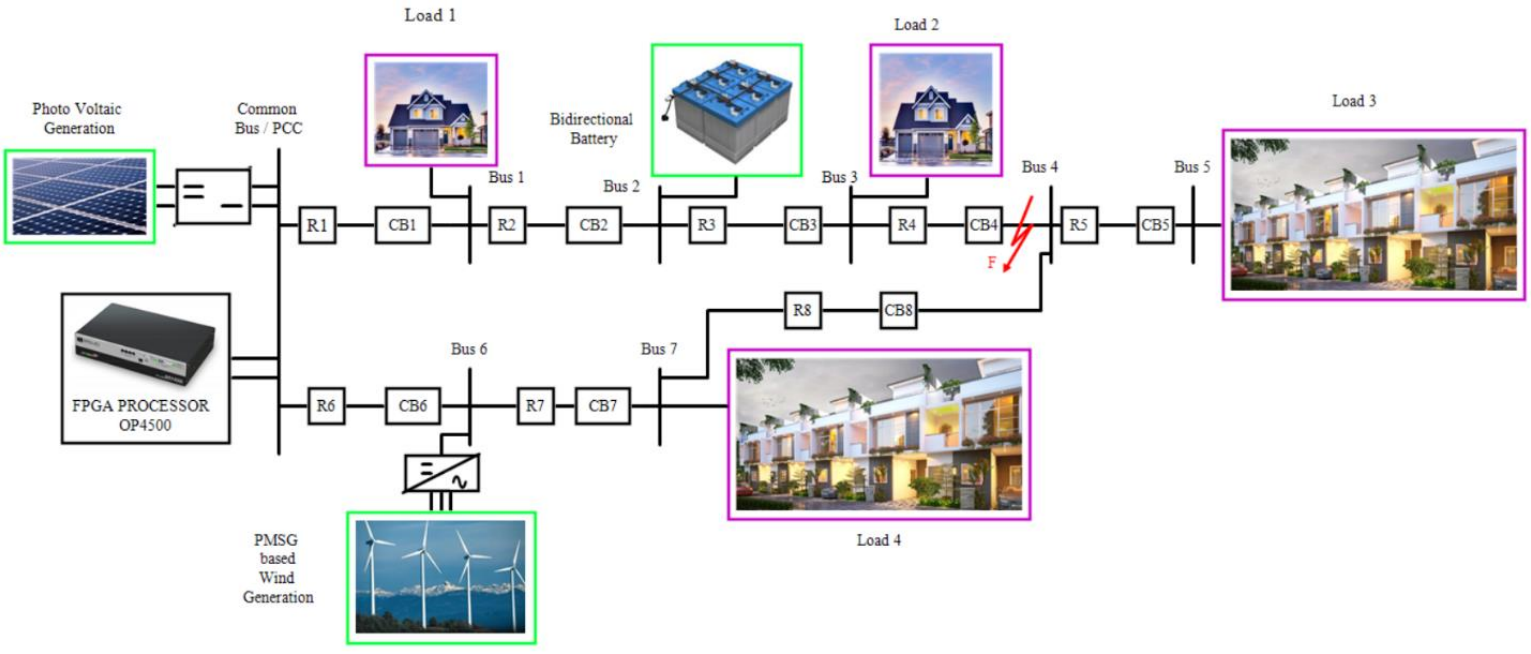

Load 1
Load 2
Load 3
Photo Voltaic Generation
Common Bus / PCC
Bidirectional Battery
Bus 1
Bus 2
Bus 3
Bus 4
Bus 5
R1
CB1
R2
CB2
R3
CB3
R4
CB4
R5
CB5
F
R8
CB8
FPGA PROCESSOR OP4500
Bus 6
Bus 7
R6
CB6
R7
CB7
PMSG based Wind Generation
Load 4

Fig. 19

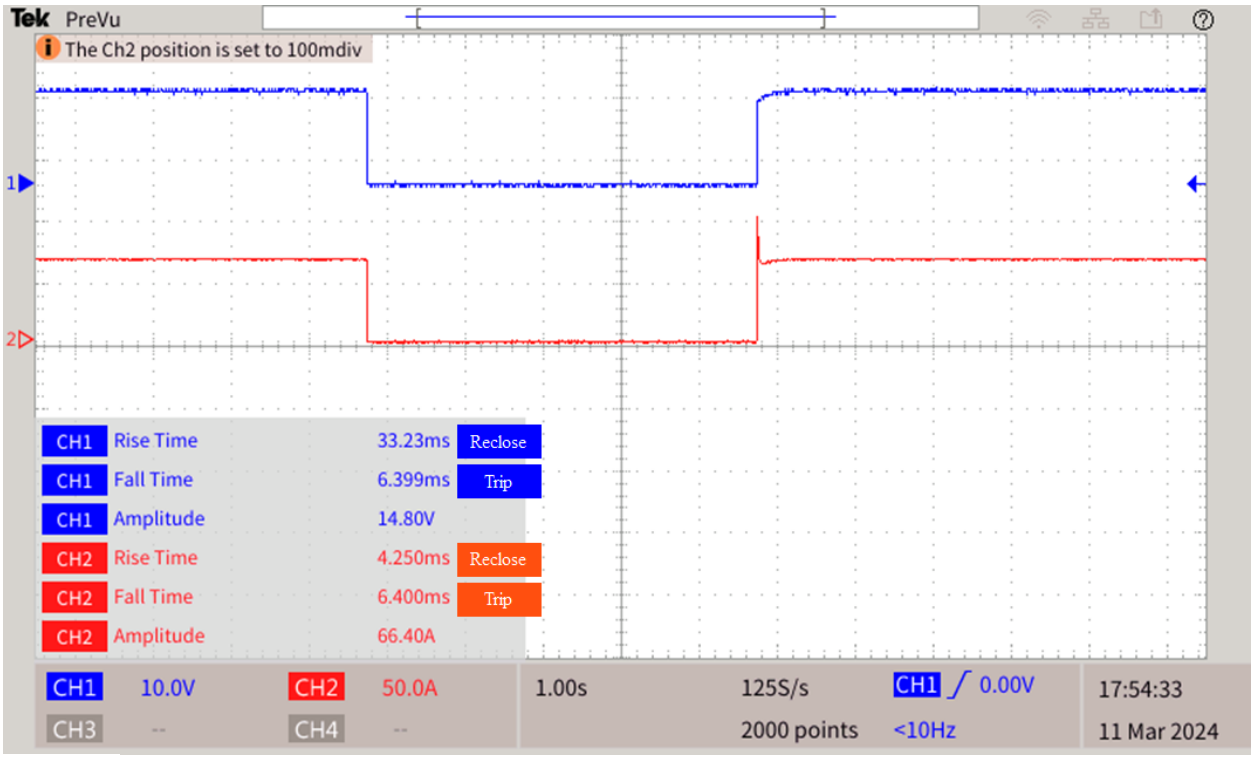


Fig. 20

Table 1 Different combination of L and C values for reducing voltage stress during reclosing operation of modified new z -source breaker

Capacitor / Inductor	L = $1.e^{-1}$	L = $1.e^{-2}$	L = $1.e^{-3}$	L = $1.e^{-4}$	L = $1.e^{-5}$	L = $1.e^{-6}$	L = $1.e^{-7}$	L = $1.e^{-8}$	L = $1.e^{-9}$
C = $1.e^{-1}$	401 V 13.46 A	404.23 V 13.48 A	404.584 V 13.486 A	404.585 V 13.486 A	404.58 V 13.4855 A	404.584 V 13.486 A	404.584 V 13.4861A	404.583V 13.486A	404.585V 13.486A
C = $1.e^{-2}$	444.77 V 14.825 A	433.65 V 14.45 A	431.93 V 14.397 A	431.81 V 14.394 A	431.809 V 14.393 A	431.808 V 14.3936 A	431.804 V 14.39345A	431.8045V 14.39349A	431.80455V 14.3135A
C = $1.e^{-3}$	579.292 V 19.31 A	912.42 V 30.41 A	899.13 V 29.97 A	899.25 V 29.974 A	899.25 V 29.975 A	899.24 V 29.975 A	899.2485 V 29.973 A	899.2487 V 29.9749 A	899.2485 V 29.9749 A
C = $1.e^{-4}$	2327.13 V 77.5 A	2271.88 V 75.73 A	2176.16 V 72.54 A	2176.14 V 72.538 A	2176.22 V 72.54 A	2176.226V 72.54 A	2176.227V 72.54 A	2176.227V 72.5409 A	2176.2276V 74.5409 A
C = $1.e^{-5}$	5369.96 V 178.99 A	5125.905 V 170.86 A	4743.68 V 158.12 A	4743.59 V 158.12 A	4743.76 V 158.125 A	4743.75 V 158.125 A	4743.756 V 158.1252 A	4743.756 V 158.125 A	4743.756 V 158.125 A
C = $1.e^{-6}$	7774.74 V 259.15 A	7263.276 V 242.109 A	6706.32 V 223.54 A	6706.26 V 223.54 A	6706.27 V 223.54 A	6706.14 V 223.538 A	6706.141 V 223.538 A	6706.1414V 223.538 A	6706.1414V 223.538 A
C = $1.e^{-7}$	9065.059 V 302.168 A	8993.64V 299.785 A	8619.31 V 287.31 A	8618.482 V 287.28 A	8618.27 V 287.27 A	8618.26 V 287.275 A	8618.2659 V 287.2755 A	8618.2659 V 287.2755 A	8618.2659 V 287.2755 A
C = $1.e^{-8}$	9290.289 V 309.67 A	9212.73 V 307.09 A	8802.25 V 293.408 A	8801.43 V 293.38 A	8801.236 V 293.37 A	8801.2366 V 293.374 A	8801.2368 V 293.3745 A	8801.2367V 293.3745 A	8801.2367 V 293.3745 A

C = $1.e^{-9}$	9311.29 V 310.37 A	9232.92 V 307.76	8818.989 V 293.96 A	8818.14 V 293.935 A	8818.945 V 293.9315 A	8817.945 V 293.9315 A	8817.9458 V 293.9315 A	8817.9458 V 293.93152 A	8817.9458 V 293.9315A

Table 2 Breaker comparison

Features	**ZSCB [9]**	**SZSCB [10]**	**BZSCB [36]**	**BDSZSCB [13]**	**MBZCB [19]**	**QZSCB [18]**	**modified OZ [12]**	**OZSCB [37]**	**TSCB [17]**	**New Z [26]**	**Modified new Z (proposed)**
Diodes	2	2	2	6	nil	nil	0	nil	1	4	**5**
Switching devices	1	1	4	1	4	2	4	2	4	2	**2**
Capacitors	2	2	3	2	1	1	1	1	1	3	**3**
Inductor / Magnetic Component required	2	2	2	2	1	1	1	1	1	4	**4**
Negative Fault Current Flow	22A	30A	0.5A	4.2A	0.7A	35A	0.049A	0.2A	0.45A	202A	**0.0092**
Fault isolation time (µs)	113	75	5000	320	24	5000	500	80	90	600	**200**
Snubber circuit	2	2	1	2	1	1	0	1	2	4	**4**
Load current il (A)	6A	10A	6A	6	6A	8	8	8A	10A	12	**14**
Power loss (W)	19	25	18	23.4	14.4	9.64	9.37	9.38	181	5.5	**4**
Tripping based on fault conductance	No	No	Yes	Yes	No	No	Yes	Yes	No	Yes	**Yes**
Fault current reflected to source	6A	50A	8A	6A	0	48A	64A	7.2A	0	72A	**0**
Surge due to fault	48A	52A	18A	17A	12A	22A	10A	10.5A	15A	410A	**2A**
Rating of switching device	High	High	High	Low	High	Moderate	Low	Low	High	Moderate	**High**
Common ground	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	**Yes**
Application	MVDC	LVDC	MVDC	LVDC & MVDC	MVDC	high current	LVDC & MVDC	LVDC	LVDC & MVDC	MVDC	**LVDC Microgrid**
Negative current in load during Reclosing operation	5.2A	6A	4.2A	3.8A	0.4A	0.3A	0.009A	0.11A	2.11A	210A	**0.2A**
Voltage & current stress	9V,0.85 A	28V,17 A	33V,12A	102V,19A	22V,2A	1.2V,3.94A	11V,0.9A	10V,2.2A	172V,22A	480V,420A	**3V,0.8A**
Configuration	Uni-directional	Uni-directional	Uni-directional	Bidirectional	Bidirectional	Bidirectional	Uni-directional and bidirectional	Bidirectional	Uni-directional	Bidirectional	**Bidirectional**
load analyzed	Resistive &Inductive	Resistive & capacitive	Resistive & capacitive	Resistive & capacitive	Resistive & capacitive	Resistive	Resistive	Resistive	Resistive & capacitive	Resistive & capacitive	**Resistive & capacitive**
Efficiency (%)	82	89	81	85	91	97.2	98	90.2	90.5	96	**99.1(5kW) 98.27(50kW)**
Total cost (INR)	800	900	1800	1550	1600	750	600	200	2800	2200	**600**

Table 3 Comparison of protection algorithms in literature for active bus identifications [31-35]

ALGORITHM	AC MICROGRID			DC MICROGRID		
	BUS NETWORK	PROCESSOR USED	RUNNING TIME (ms)	BUS NETWORK	PROCESSOR USED	RUNNING TIME (ms)
Prims [31]	21 Bus	AMD A10	0.015	7 Bus	Intel Xeon E3-1225 V3 @ 3.20GHz	**0.10**
		Intel i3	0.013		Intel i5	**0.08**
Kruskal [34]	39 Bus	Intel Celeron	1.6358	7 Bus	Intel Xeon E3-1225 V3 @ 3.20GHz	**0.175**
		Intel i5	0.6661		Intel i5	**0.123**
Boruvka [32]	7 Bus	AMD A10	0.015	7 Bus	Intel Xeon E3-1225 V3 @ 3.20GHz	**0.312**
					Intel i5	**0.118**

Table 4 Comparison of protection algorithms in literature for shortest path identifications [31-35]

ALGORITHM	AC MICROGRID			DC MICROGRID		
	BUS NETWORK	PROCESSOR USED	RUNNING TIME (ms)	BUS NETWORK	PROCESSOR USED	RUNNING TIME (ms)
Dijkstra's [18]	39 Bus	Intel i5	0.2930	7 Bus	Intel Xeon E3-1225 V3 @ 3.20GHz,	**0.328**
		Intel Celeron	0.9030		Intel i5	**0.252**
Floyd Warshall [34]	39 Bus	Intel i5	4.3686	7 Bus	Intel Xeon E3-1225 V3 @ 3.20GHz	**0.997**
		Intel Celeron	21.8058		Intel i5	**0.867**
Bellman-Ford [35]	NIL	NIL	NIL	7 Bus	Intel Xeon E3-1225 V3 @ 3.20GHz	**0.235**
					Intel i5	**0.442**

Author's Biography

Faazila Fathima S received bachelor of engineering degree from SRR Engineering College, Chennai, India in 2012 and Masters of technology degree from B.S. Abdur Rahman University, Chennai, India in 2014. Currently working as a research associate and pursuing PhD at Vellore Institute of Technology, Chennai, India. The areas of interest include protection of DC microgrid, data science optimization algorithm and artificial intelligence. E-mail: faazila.fathima2019@vitstudent.ac.in

Premalatha L received Bachelor degree in Electrical and Electronics, Master's in Power Systems and Ph.D. in Electrical Engineering from Anna University, Chennai, India, in 2009. Following her doctoral studies, she was awarded a post-doctoral fellowship from the University of Malaya, Kuala Lumpur, in 2013. Accumulating over 25 years of teaching and her scholarly contributions include over 60 publications across various international journals and conferences. Currently, she is working as a Professor in the School of Electrical Engineering at Vellore Institute of Technology, Chennai, India, focusing her research on the application of power electronics in power systems, power quality issues, and the utilization of IoT and machine learning in power systems. Email: premalatha.l@vit.ac.in