# A Unified Controller Design Method for Multiple Control Structure with Perspective to Parametric Independent Control of Boost Converter

Purnima Verma[a*] and Md Nishat Anwar[a]

[a]Department of Electrical Engineering, National Institute of Technology, Patna 800005, Bihar, India

*Corresponding author- Email address: purnimav.phd19.ee@nitp.ac.in, Mob. No. +917080533224

***Abstract*— In this work, a unified approach for controller design has been presented which can be used in different control structures. To validate the proposal, output voltage regulation of the boost converter has been considered as control problem. The control structure considered are single feedback control structure, parallel control structure, two-degree of freedom internal model control structure and cascade control structure. In these control structures, the transfer function model obtained through simple closed-loop test has been used to derive the controller parameter. This modelling makes the control scheme independent of boost converter circuit parameter information as well as loads. The controller parameters in all these structures have been obtained through direct synthesis design in frequency domain. Experimental results for nominal and perturbed values are illustrated under changing set-point command and load-disturbance (variation in input voltage and duty cycle). Using small gain theorem, robustness of all the structures is evaluated where cascade control structure is found to have stability of 60% change in gain uncertainty. Performance of cascade structure is observed to be better in comparison with other structures. The control performance of the proposed work has also been compared with the recently reported works.**

***Index Terms*— Boost converter, parallel control structure, cascade control structure, parametric independent control, PI controller**

## 1. INTRODUCTION

The output voltage control of the boost converter (BC) is challenging due to its non-minimum phase (NMP) behavior, non-linearity, discontinuity in time and parametric uncertainties [1]. The general controller design procedure involves with selection of appropriate model, control structure, type of controller and its proper design technique. The appropriate model greatly affects the controller design procedure and achievable desired performance. In order to capture the dynamics of BC different modelling techniques have been used like small signal modelling [1]–[6], large signal modelling [7]–[9], discrete time modelling [10]–[13], Lagrangian approach based modelling technique [14], [15]. Aforementioned analytical techniques involve detailed information of circuit parameters and loading conditions. It however, encompass approximation or linearization techniques which ultimately

lead to plant-model mismatch. Apart from this, real time experiments can capture more realistic dynamics of BC attenuating the mismatch between plant and its model. Closed loop test (CLT) is one of them in which an open loop model of a system is obtained using a proportional (P) or proportional-integral (PI) controller. In the literature, real time experiments-based models are rarely reported.

Voltage mode and current mode are the two modes in which majority of BC are regulated. In the voltage mode control scheme, the output voltage is compared to the reference voltage, and the error is sent to the controller, which modifies the duty cycle to reach the reference voltage. Both the output voltage and the inductor current of BC are controlled in the current mode control by using an extra current sensor. Two control loops make up the cascade control structure (CCS) used to implement BC current mode control. Kim and Lee [16] have proposed a current mode control scheme where PI controllers of inner and outer loop are designed by robust feedback linearization technique which accounts for parametric uncertainty. Robust performance against parametric uncertainty is obtained using nested reduced order PI observer by Kim and Son [17]. They have achieved improved robust performance over [16] in feedback and feedforward configuration. The tracking performance is further improved by Kim and Ahn [18] as compared with [16]. Zhang et al. [19] have proposed a new cascade control strategy with digital peak current mode control for minimizing the current tracking delay in the BC. Further, model predictive control and input state linearization has been used by Aouni and Dessaint [20] in cascade control configuration for output voltage of BC. Kim and Lee [21] has proposed a new cascade control scheme for BC without the use of current sensor and method does not require converter parameter information.

Apart from current mode control, tremendous work has been reported for voltage mode control with modified control structure like, single feedback control structure (SFCS), internal model control (IMC) structure, two degree of freedom internal model control (T-DF IMC) structure, variable control structure, active disturbance rejection control, etc. Kobaku et al. [22] have controlled the output voltage of BC in voltage mode using IMC control scheme. Their method requires the converter circuit parameter and load. However, Kim [23] has proposed a nonlinear observer based multivariable and multiloop control scheme which does not require the true value of converter parameter. Further, Kobaku et al. [24] have presented a robust proportional-integral-derivative (PID) controller for BC designed through modified direct synthesis (DS) scheme under feedforward framework. Ahmad and Ali has presented a review of control of BC with active disturbance rejection control scheme, T-DF IMC structure and T-DF conventional control scheme in [25]. Jha et al. [26] have considered SFCS and IMC structure for voltage mode control of BC however their method does not require BC parameter information. A comparative review of recent work is given in Table 1.

In light of discussed literature, the following conclusion can be drawn.

- Most of the work is based on the analytical model of BC, where circuit parameter information and load are mandatory. Under varying load conditions, as a result, the dynamics of the converter change accordingly, making real-time experiments a better choice. Thus, a limited amount of work has been reported that does not require BC circuit parameter information.
- Many controller design procedures involve complex and lengthy mathematical approaches. However, an approximation-based frequency domain technique is reported which is simple and convenient to implement for any complex control structure.
- In the literature, BC is often controlled by various control structures categorized in single degree of freedom, two degree of freedom and cascade structures etc. but a comparative analysis is required to identify the suitability of control structure.
- Minimum attention has been given to develop a controller design strategy which can be applicable to different control structures in a unified way.

With these motivations, a unified controller design method has been presented which can be used in different control structure (SFCS, parallel control structure (PCS), T-DF IMC and CCS). In this work, control of BC in different control structures have been presented. The test based modelling technique reported in our earlier work [26] is used in all these structures which makes them parametric independent also, loading condition is not required. All these schemes are implemented through hardware and compared. Robustness analysis has also been investigated through the small gain theorem. The main contribution of this work is highlighted as:

1. A generic controller design technique has been proposed which can be applied in different control structures in a unified way.
2. The suitability of the model (obtained through test) for control of BC has been established.
3. Three parametric independent control schemes (PCS, T-DF IMC, CCS) have been proposed for the control of BC.
4. Comparative performance analysis of different control structures (SFCS, PCS, T-DF IMC, CCS) for control of BC has been done.
5. Comparative robustness analysis of these control structures has been investigated through the small gain theorem.

Rest of the manuscript is organized as follows: Section 2 presents modelling of BC using CLT. Four different control structures and their controller design method are discussed in Section 3. Hardware results and discussion is presented in Section 4 followed by robustness analysis in Section 5. Section 6 is the conclusion of the paper.

## 2. CLOSED LOOP TEST-BASED MODELLING OF BOOST CONVERTER

In this work, model of BC is obtained through simple CLT. As stated in our previous work [26], this obtained model uses a proportional controller to perform a simple closed loop step test. The test is performed with the control configuration as shown in Figure 1, where, $v_{ref}$ is the reference voltage, $v_o$ is the output voltage, $d$ is the duty cycle, $Q$ is the proportional controller, $G_3$ is the BC. The BC $(G_3)$ is represented as cascaded system $G_1$ and $G_2$ which is used in the current mode control of the BC.

The circuit parameter of BC is selected as: inductance $(L)=5mH$, capacitance $(C)=1100\mu F$, input voltage $(V_{in})=12V$, output voltage $(V_o)=18V$, duty ratio $(D)=0.33$, resistance $(R)=50\Omega$ and switching frequency $(f_s)=15kHz$. A set-point experiment has been performed several times with different values of gains and finally five transfer functions have been obtained for five different gains. The obtained transfer function models from output voltage to duty cycle $(M_{3jv/d})$ and from inductor current to duty cycle $(M_{2ji/d})$ are given in Table 2. The obtained model should be able to define the dynamics of real system. From control point of view, better suited model is required to achieve improved performance. The frequency response of these obtained models is shown in Figure 2 and Figure 3. From these figures, it can be seen that these models are matching closely. Thus, it gives freedom to choose any of these models for the controller design. All these models have been successfully used for the controller design. However, the response of controller with models $M_{31v/d}$ and $M_{21i/d}$ are presented in this work.

## 3. CONTROLLER DESIGN METHOD FOR DIFFERENT CONTROLLER STRUCTURES

In this work, the output voltage of BC has been controlled using different control structures, like (i) SFCS, (ii) PCS, (iii) T-DF IMC, and (iv) CCS. In all these structures, PI controller has been considered and its parameter is designed using DS approach in frequency domain [31], [32] either for improved set-point (SP) response or for load-disturbance (LD) response. In DS method, a desired reference model or transfer function is selected which is further equated with the closed loop transfer function of the system to offer necessary closed loop performance. In case of NMP dynamics system, right half plane zeros are included as a part of desired reference model. Further, a SP controller and/or LD rejection controller is obtained in terms of the system model and desired reference transfer function. The obtained controller may be in a higher order form and is not physically realizable. Using approximate frequency matching technique, the controller parameters i.e., PI are evaluated for each of the aforementioned structures. With regard to this, an overview of controller design method is briefly discussed below:

### *3.1 Overview of approximate frequency response matching technique*

Suppose a function $Q(s)$ is required to be approximated as a function $R(s)$. These two functions will be identical, if the frequency response of these functions is matched for $\omega$ ranging from 0 to $\infty$. This can be mathematically represented as

$$Q(s)|_{s=j\omega} \cong R(s)|_{s=j\omega}; \forall \omega \in (0,\infty) \tag{1}$$

Now, Equation (1) is dissociated into real and imaginary part,

$$Q^{Re}(s)|_{s=j\omega} + jQ^{Im}(s)|_{s=j\omega} \cong R^{Re}(s)|_{s=j\omega} + jR^{Im}(s)|_{s=j\omega} \tag{2}$$

Comparing real and imaginary part of Equation (2), yields

$$\begin{aligned} Q^{Re}(\omega) &\cong R^{Re}(\omega) \\ Q^{Im}(\omega) &\cong R^{Im}(\omega) \end{aligned} \tag{3}$$

In order to match LHS and RHS of Equation (3), Taylor series expansion around $\omega = 0$ is equated using its initial terms. Matching of Equation (3) is further accomplished by equating the initial $H$ derivatives written as

$$\left.\begin{aligned} \frac{d^k}{d\omega^k}\left[Q^{Re}(\omega)\right]|_{\omega=0} &= \frac{d^k}{d\omega^k}\left[R^{Re}(\omega)\right]|_{\omega=0} \\ \frac{d^k}{d\omega^k}\left[Q^{Im}(\omega)\right]|_{\omega=0} &= \frac{d^k}{d\omega^k}\left[R^{Im}(\omega)\right]|_{\omega=0} \end{aligned}\right\}; k \in [0, H-1]. \tag{4}$$

A good approximation is hold by using dividend difference calculus discussed in [33], real and imaginary parts of Equation (4) approximately matches if,

$$\left.\begin{aligned} Q^{Re}(\omega)\Big|_{\omega=\omega_n} &= R^{Re}(\omega)\Big|_{\omega=\omega_n} \\ Q^{Im}(\omega)\Big|_{\omega=\omega_n} &= R^{Im}(\omega)\Big|_{\omega=\omega_n} \end{aligned}\right\}; k \in [0, H-1] \tag{5}$$

Here, $\omega_n$ is positive and small value around $\omega$. It is observed from Equation (5) that $H$ values of $\omega$ provide $2H$ linear algebraic equations and thus, to get two unknown controller parameters (i.e., PI), $H$ is chosen as 1. And for three unknown controller parameters (i.e., PID), $H$ is chosen as 2. Thus, by matching at suitably low value of frequency higher order function $Q(s)$ can be approximated to a lower order function $R(s)$. If $Q(s)$ is required to be approximated as PI controller $\left(Q^{PI}(s)\right)$ with the parallel form given below:

$$Q^{PI}(s)|_{s=j\omega} = K_P + K_I / j\omega$$

where, $K_P$ = Proportional controller, $K_I$ = Integral controller.

Using Equation (5), matching at one frequency point will be following two equations.

$$\begin{bmatrix} 1 & 0 \\ 0 & \frac{-1}{\omega} \end{bmatrix} \begin{bmatrix} K_P \\ K_I \end{bmatrix} = \begin{bmatrix} Re\left(Q(\omega)\right) \\ Im\left(Q(\omega)\right) \end{bmatrix} \tag{6}$$

Solving Equation (6), one will get the controller parameters.

This approximation technique is applied in different structures in the below subsections:

### *3.2. Single feedback control structure (SFCS)*

A single feedback control structure is shown in Figure 4. where, $G_3$ is the BC and $Q_{SFCS}$ is the PI controller. In SFCS, both the SP and LD rejection responses are controlled using a single controller providing a single degree of freedom control.

#### 3.2.1 Controller design for SFCS

The closed loop SP transfer function for SFCS is obtained as

$$\frac{V_o(s)}{V_{ref}(s)} = P_{1SFCS} = \frac{Q_{SFCS}(s)G_3(s)}{1+Q_{SFCS}(s)G_3(s)}. \tag{7}$$

The desired reference transfer function for SP response is chosen as

$$P_{1des,SFCS}(s) = \frac{1}{\left(\lambda_{1SFCS}s+1\right)^{n_{1SFCS}}} \tag{8}$$

where, $\lambda_{1SFCS}$ is the tuning parameter and $n_{1SFCS}$ is the order of the desired reference transfer function which is selected to make the controller physically realizable. In order to design the PI controller parameters through DS approach, a desired reference transfer function is equated with the closed loop transfer function of the BC. Further, controller is obtained in terms of model of BC and desired reference transfer function as

$$Q_{SFCS}(s) = \frac{P_{1des,SFCS}(s)}{G_3(s)\left[1-P_{1des,SFCS}(s)\right]}. \tag{9}$$

One can get the PI controller parameters evaluated from Equation (9) and from matrix given in Equation (6). The parallel form of controller parameters is given by,

$$Q_{SFCS}^{PI}(s) = K_{P1,SFCS} + \frac{K_{I1,SFCS}}{s} \tag{10}$$

Now, the closed loop transfer function for load disturbance rejection is obtained as

$$\frac{V_o(s)}{L(s)} = P_{2SFCS} = \frac{G_3(s)}{1+Q_{SFCS}(s)G_3(s)} \tag{11}$$

$Q_{SFCS}(s)$ is to be calculated which is written in parallel PI form by,

$$Q_{SFCS}^{PI}(s) = K_{P2,SFCS} + \frac{K_{I2,SFCS}}{s} \tag{12}$$

The desired reference transfer function for LD rejection is selected as

$$P_{2des,SFCS}(s) = \frac{Ks}{(\lambda_{2SFCS}s+1)^{n_{2SFCS}}}. \tag{13}$$

Here, a zero is placed at the origin to eliminate the effect of load disturbances and $\lambda_{2SFCS}$ is the adjustable tuning parameter. The value of $K$ is evaluated using final value theorem [34], Equation (11) is equated with Equation (13) as given below:

$$\lim_{s\to 0}\frac{G_3(s)}{1+Q_{SFCS}(s)G_3(s)} = \lim_{s\to 0}\frac{Ks}{(\lambda_{2SFCS}s+1)^{n_{2SFCS}}} \tag{14}$$

Substituting the value of $G_3(s)$ or $M_{3jv/d}(s)$ and $Q_{SFCS}(s)$ as PI controller in Equation (14), we get

$$\lim_{s\to 0}\frac{\dfrac{7.3121e5}{s^2+140.5s+2.366e4}}{1+\left[\left(\dfrac{sK_{P2,SFCS}+K_{I2,SFCS}}{s}\right)\left(\dfrac{7.3121e5}{s^2+140.5s+2.366e4}\right)\right]} = \lim_{s\to 0}\frac{Ks}{(\lambda_{2SFCS}s+1)^{n_{2SFCS}}} \tag{15}$$

On substituting $s\to 0$, Equation (15) results into,

$$K = \frac{1}{K_{I2,SFCS}}. \tag{16}$$

The controller for LD rejection is obtained using Equation (11), Equation (12) and Equation (13) by approximating them at a frequency point, $\omega$.

$$K_{P2,SFCS} + \left.\frac{K_{I2,SFCS}}{s}\right|_{s=j\omega} = \left.\frac{1}{P_{2des,SFCS}(s)} - \frac{1}{G_3(s)}\right|_{s=j\omega} \tag{17}$$

On assuming, $(K_{I2,SFCS}\times(\lambda_{2SFCS}s+1)^{n_{2SFCS}})/s = a$ and $1/G_3(s) = b$, Equation (17) can be grouped into a matrix after dissociating it into real and imaginary part,

$$\begin{bmatrix} 1 & -Re\{a(\omega)\} \\ 0 & \left(\frac{-1}{\omega} - Im\{a(\omega)\}\right) \end{bmatrix} \begin{bmatrix} K_P \\ K_I \end{bmatrix} = \begin{bmatrix} -Re(b(\omega)) \\ -Im(b(\omega)) \end{bmatrix} \quad (18)$$

From here, the value of PI controller is found.

The gains of PI have been obtained by approximately matching frequency response of $Q_{SFCS}(s)$ and $Q_{SFCS}^{PI}(s)$ at $\omega = 0.01$ rad/sec.

In SFCS, the SP and LD response are controlled with only one controller and are coupled together. Improvement in SP response generally leads to degradation in the LD response and vice versa. One solution is to design the improved LD response and further SP filter is used to get improved SP response [35]. Another solution is the use of two degree of freedom (T-DF) control structures which decouples the SP and LD response. In this work, T-DF control structure has been considered for the output voltage regulation of BC namely, PCS and T-DF IMC. These T-DF control structure and their controller design method are discussed below.

### *3.3. Parallel control structure (PCS)*

PCS is a T-DF control structure where the two controllers are used to control the SP and LD response independently. This structure was proposed by Karunagaran and Wenjian [36]. Figure 5 represents a parallel control structure. In this figure, $M_{31v/d}$ is the model of the system and $G_3$ is the actual system of the BC. $Q_{1PCS}$ controls the SP response with control signal $d_1$ whereas $Q_{2PCS}$ regulates the LD rejection performance with control signal $d_2$.

From Figure 5, the relation of output voltage to SP command and LD is obtained as

$$V_o(s) = \frac{G_3(s)}{M_{31v/d}(s)}\left[\frac{Q_{1PCS}(s)M_{31v/d}(s)}{1+Q_{1PCS}(s)M_{31v/d}(s)}\right] \left(\frac{1+Q_{2PCS}(s)M_{31v/d}(s)}{1+Q_{2PCS}(s)G_3(s)}\right)V_{ref}(s) + \frac{G_3(s)}{1+Q_{2PCS}(s)M_{31v/d}(s)}L(s). \quad (19)$$

For the perfect modelling i.e., $G_3(s) = M_{31v/d}(s)$, relation in Equation (19) is simplified to,

$$V_o(s) = \left[\frac{Q_{1PCS}(s)M_{31v/d}(s)}{1+Q_{1PCS}(s)M_{31v/d}(s)}\right]V_{ref}(s) + \frac{G_3(s)}{1+Q_{2PCS}(s)M_{31v/d}(s)}L(s). \quad (20)$$

From Equation (20), it is evident that LD response is controlled through $Q_{2PCS}$ whereas better SP response can be obtained using

$Q_{1PCS}$ only. Thus, this structure decouples the SP and LD response. Also, it is noticeable that the closed loop transfer function is same as the one obtained for SFCS in Equation (7) and Equation (11). Thus, the performance of PCS is similar to that of SFCS.

### 3.3.1 Controller design for PCS

The transfer function from output voltage to SP voltage is obtained by considering ($l = 0$) given by,

$$\frac{V_o(s)}{V_{ref}(s)} = P_{1PCS}(s) = \left[\frac{Q_{1PCS}(s) M_{31v/d}(s)}{1 + Q_{1PCS}(s) M_{31v/d}(s)}\right]. \tag{21}$$

The desired reference transfer function for the SP response is chosen as

$$P_{1des,PCS}(s) = \frac{1}{(\lambda_{1PCS} s + 1)^{n_{1PCS}}} \tag{22}$$

where, $\lambda_{1PCS}$ is the only tuning parameter and $n_{1PCS}$ is the order of the desired reference transfer function. Similarly, $Q_{1PCS}$ is obtained using Equation (21) and Equation (22),

$$Q_{1PCS}(s) = \frac{P_{1des,PCS}(s)}{M_{31v/d}(s)\left[1 - P_{1des,PCS}(s)\right]} \tag{23}$$

The transfer function from output voltage to LD is obtained by considering $(v_{ref} = 0)$ as

$$\frac{V_o(s)}{L(s)} = P_{2PCS}(s) = \frac{M_{31v/d}(s)}{1 + Q_{2PCS}(s) M_{31v/d}(s)}. \tag{24}$$

The desired reference transfer function for LD rejection is selected as

$$P_{2des,PCS}(s) = \frac{Ks}{(\lambda_{2PCS} s + 1)^{n_{2PCS}}}. \tag{25}$$

The value of $K$ is selected similarly as discussed from Equation (13) to Equation (16) and thus, $K$ results in $1/K_{I2,PCS}$.

The controller $Q_{2PCS}$ is obtained as

$$Q_{2PCS}(s) = \frac{1}{P_{2des,PCS}(s)} - \frac{1}{M_{31v/d}(s)}. \tag{26}$$

The controllers $Q_{1PCS}$ and $Q_{2PCS}$ in PI form is considered as

$$Q_{1PCS}(s) = Q_{1PCS}^{PI}(s) = K_{P1,PCS} + \frac{K_{I1,PCS}}{s} \tag{27}$$

$$Q_{2PCS}(s) = Q_{2PCS}^{PI}(s) = K_{P2,PCS} + \frac{K_{I2,PCS}}{s} \tag{28}$$

The parameter of SP controller $Q_{1PCS}$ and LD controller $Q_{2PCS}$ is obtained by matching the relation in Equation (23) with Equation (27), and relation Equation (26) with Equation (28) at low frequency point, respectively.

*3.4. Two degree of freedom IMC structure (T-DF IMC)*

T-DF IMC is another T-DF control structure that gives freedom to control the SP response and the LD response separately. Its control structure is shown in Figure 6, where $M_{31v/d}$ is the model of the BC, $Q_{1T-DF\ IMC}$ and $Q_{2T-DF\ IMC}$ are SP and LD controller, respectively [37].

**3.4.1 Controller design for T-DF IMC**

The transfer function from output voltage to SP voltage is obtained by considering ($l = 0$) as

$$\frac{V_o(s)}{V_{ref}(s)} = P_{1T-DF\ IMC}(s) = \frac{G_3(s)Q_{1T-DF\ IMC}(s)}{1+\left[G_3(s)-M_{31v/d}(s)\right]Q_{1T-DF\ IMC}(s)} \frac{\left[1+M_{31v/d}(s)Q_{2T-DF\ IMC}(s)\right]}{+G_3(s)Q_{2T-DF\ IMC}(s)} \tag{29}$$

On assuming, $G_3(s) = M_{31v/d}(s)$, Equation (29) is simplified to,

$$P_{1T-DF\ IMC}(s) = G_3(s)Q_{1T-DF\ IMC}(s) \tag{30}$$

The transfer function of SFCS in Equation (7) is compared with Equation (30) when $Q_{2T-DF\ IMC}(s) = 0$, resulting in,

$$Q_{SFCS}(s) = \frac{Q_{1T-DF\ IMC}(s)}{1 - Q_{1T-DF\ IMC}(s)M_{31v/d}(s)} \tag{31}$$

$$Q_{1T-DF\ IMC}(s) = \frac{Q_{SFCS}(s)}{1 + Q_{SFCS}(s)M_{31v/d}(s)} \tag{32}$$

Equation (31) and Figure 6 ultimately corresponds to SFCS (Figure 4). As discussed in the above subsections, a desired reference model is selected and is equated with Equation (30). Similar procedure is followed to get the resulting expression of $Q_{1T-DF\ IMC}(s)$ and is further approximated to PI controller parameters, where $Q_{1T-DF\ IMC}(s)$ is obtained as

$$Q_{1T-DF\ IMC}^{PI}(s) = K_{P1,T-DF\ IMC} + \frac{K_{I1,T-DF\ IMC}}{s} \tag{33}$$

The transfer function in case of LD when $v_{ref} = 0$ is obtained as

$$\frac{V_o(s)}{L(s)} = P_{2T-DF\ IMC}(s) = \frac{G_3(s)\left[1 - M_{31v/d}(s)Q_{1T-DF\ IMC}(s)\right]}{1 + \left[G_3(s) - M_{31v/d}(s)\right]Q_{1T-DF\ IMC}(s) + G_3(s)Q_{2T-DF\ IMC}(s)} \tag{34}$$

On assuming $G_3(s) = M_{31v/d}(s)$, Equation (34) is simplified to,

$$P_{2T-DF\ IMC}(s) = \frac{G_3(s)\left[1 - M_{31v/d}(s)Q_{1T-DF\ IMC}(s)\right]}{1 + G_3(s)Q_{2T-DF\ IMC}(s)} \tag{35}$$

To design the LD controller $Q_{2T-DF\ IMC}(s)$, a reference model is selected and further its PI controller parameters is given as:

$$Q^{PI}_{2T-DF\ IMC}(s) = K_{P2,T-DF\ IMC} + \frac{K_{I2,T-DF\ IMC}}{s} \tag{36}$$

Relation in Equation (35) depends on controller $Q_{1T-DF\ IMC}(s)$ and $Q_{2T-DF\ IMC}(s)$. This allows to select the LD rejection controllers after proper selection of $Q_{1T-DF\ IMC}(s)$. T-DF IMC differs from SFCS only by the usage of an additional controller to reject the external disturbances quickly.

### *3.5. Cascade control structure (CCS)*

The enhanced LD rejection performance can be obtained through CCS with an additional sensor and controller. It results into two loop structure as shown in Figure 7 where, $Q_{2CCS}$ is the inner loop controller whereas $Q_{1CCS}$ is the outer loop controller. $G_1$ is the plant of the outer loop known as primary plant and $G_2$ is the plant of the inner loop also named as secondary plant.

Essential requirements for the implementation of CCS is that the inner loop must act faster than the outer loop in order to reject the external disturbances before it affects the entire system. To achieve this, the inner loop is designed faster than the outer loop [38]. The overall behavior of CCS is analyzed by firstly dealing with the inner loop where the transfer function from Figure 7 is obtained from the below expression

$$i_L(s) = \frac{G_2(s)Q_{2CCS}(s)}{1 + G_2(s)Q_{2CCS}(s)} i_{ref}(s) + \frac{G_2(s)}{1 + G_2(s)Q_{2CCS}(s)} L(s) \tag{37}$$

$$i_L(s) = G^*_2(s) i_{ref}(s) + G^*_1(s) L(s) \tag{38}$$

Figure 7 is now consolidated to the below figure represented as

Now, using Figure 8, the transfer function of the overall CCS is written as

$$V_o(s) = \frac{G_1(s)G_2^*(s)Q_{1CCS}(s)}{1+G_1(s)G_2^*(s)Q_{1CCS}(s)}V_{ref}(s) + \frac{G_1^*(s)G_1(s)}{1+G_1(s)G_2^*(s)Q_{1CCS}(s)}L(s) \quad (39)$$

Comparing Equation (7) and Equation (11) of SFCS with Equation (39), we get

$$\left.\begin{aligned} G_2^*(s) = 1 = \frac{G_2(s)Q_{2CCS}(s)}{1+G_2(s)Q_{2CCS}(s)} \\ G_1^*(s) = 1 = \frac{G_2(s)}{1+G_2(s)Q_{2CCS}(s)} \end{aligned}\right\} \quad (40)$$

As the magnitude of $Q_{2CCS}$ in Equation (40) increases, $G_2^* \to 1$ and $G_1^* \to 0$ resulting to $i_L \to i_{ref}$. Thus, high-performance inner-loop control eliminates the influence of the disturbance $l$ on $i_L$ (and thus on the overall system). As a result, with a fast-acting inner loop (consequence of having a large magnitude for $(Q_{2CCS})$, the entire cascade system becomes significantly less sensitive to the effects of $l$ fluctuations than to SFCS (Figure 4). Moreover, the loops time constant is required to be tuned to reject the external secondary process disturbance before it affects the primary process. For this, controllers should be tuned sequentially. Firstly, the inner loop is tuned considering $Q_{2CCS}$ and $G_2$. Secondly, the primary controller $Q_{1CCS}$ is obtained using primary plant $(G_1)$ and with the inner loop closed. The tuning parameters are selected such that $\lambda_{outer} > \lambda_{inner}$. If the secondary (inner) loop dynamics is not significantly faster than the primary loop dynamics, there lies no benefit of using cascade control [39].

**3.5.1 Controller design for CCS**

The PI controllers in this structure has been designed via IMC scheme. The advantageous feature of IMC scheme is its simplicity in controller design, robust in nature and guaranteed stability for stable systems. Figure 9 shows the application of IMC scheme in inner and outer loop where $M_{21i/d}$ is the model of inner loop plant and $M_{11v/i}$ is the model of the overall plant, $G_P$. $C_{1IMC}$ and $C_{2IMC}$ are the IMC controller for the outer and inner loop, respectively. To design the IMC controller, model of the plant is divided into invertible and non-invertible part. This controller is considered as inverse of invertible part multiplied by a suitable low pass filter [40], [41]. It is to note here that the derived model of BC does not contain non-invertible part (NMP zero and time delay) so the model will be considered as invertible part for deriving the controller.

By considering, $f_2(s) = 1/(\lambda_{inner}s+1)^{n_{inner}}$ as IMC filter of inner loop, the inner loop IMC controller is obtained as

$$C_{2IMC}(s)=\left[M_{21i/d}\right]^{-1}\times\frac{1}{\left(\lambda_{inner}s+1\right)^{n_{inner}}} \tag{41}$$

From the equivalence of SFCS and IMC control structure the relation between $Q_{2CCS}$ and $C_{2IMC}$ for the inner loop is obtained [40].

$$Q_{2CCS}(s)=\frac{C_{2IMC}(s)}{1-M_{21i/d}(s)\times C_{2IMC}(s)}. \tag{42}$$

The desired reference model of the inner loop is chosen by assuming $G_2(s)=M_{21i/d}(s)$. The transfer function of $i_L(s)/i_{ref}(s)$ then results in filter $f_2(s)$ which can also be referred to desired reference model of the inner loop. The controller in Equation (42) is approximated to PI controller by approximate frequency response matching.

$$Q_{2CCS}^{PI}(s)=K_{P2,CCS}+\frac{K_{I2,CCS}}{s}. \tag{43}$$

To design the outer loop controller, the transfer function model from inductor current to output voltage is utilized. This model can be derived from $M_{31v/d}$ and $M_{21i/d}$ as

$$M_{11v/i}=\frac{M_{31v/d}}{M_{21i/d}}. \tag{44}$$

$G_P$ constitutes of $C_{2IMC}$, $M_{21i/d}$, $G_2$ and $G_1$ seen from Figure 9. From the aforementioned assumption, the transfer function $v_o(s)/i_{ref}(s)=f_2(s)\times G_1(s)=G_P(s)$.

On considering, $f_1(s)=1/\left(\lambda_{outer}s+1\right)^{n_{outer}}$ as outer loop IMC filter, the IMC controller in outer loop is obtained as

$$C_{1IMC}(s)=\left[M_{11v/i}\right]^{-1}\times\frac{1}{\left(\lambda_{outer}s+1\right)^{n_{outer}}}. \tag{45}$$

Again, on assuming $G_P(s)=M_{11v/i}(s)$, then transfer function $v_o(s)/v_{ref}(s)=\left[M_{11v/i}\right]^{-1}\times f_1(s)\times G_P(s)$ ultimately resulting in $f_1(s)$ which is nothing but the desired reference model of the outer loop.

The outer loop controller, $Q_{1CCS}$ is obtained using below expression,

$$Q_{1CCS}(s)=\frac{C_{1IMC}(s)}{1-M_{11v/i}(s)\times C_{1IMC}(s)}. \tag{46}$$

The controller $Q_{1CCS}$ is further approximated to PI form using approximate frequency response matching given by,

$$Q_{1CCS}^{PI}(s) = K_{P1,CCS} + \frac{K_{I1,CCS}}{s}. \quad (47)$$

## 4. EXPERIMENTAL RESULTS AND DISCUSSION

In this section, the performance of the proposed schemes has been analyzed and compared through experimental setup. For this, a dedicated hardware setup of BC (Figure 10) has been developed with parameter discussed in Section 2.

TMSF28379D microcontroller is used as an interfacing agent to control the output voltage of BC. Diode MUR3060PT and MOSFET IRFP460 is used as the switching device. Programmable DC source namely, GW Instek PSW 80-27 is used as the input voltage. To sense the output voltage LV25-P is used as the voltage sensor. However, cascade control requires an additional sensor to sense the inductor current for the inner loop here, LA55-P current sensor is used. To assess the controller parameter values for a range of desired response in different control structures, one must choose an appropriate frequency point for approximation. Low frequency points are chosen for this and are listed in the below subsection:

### *4.1 Selection of low frequency points for approximation*

Good approximation of desired reference model $(P_{des})$ and designed system is held only if there exists close matching between the two. The appropriate frequency point is selected based on chosen reference model needed for a good approximation. Although, theoretically, $\omega$ ranges from 0 to $\infty$ and it is very difficult to find a value of $\omega_k$ which is sufficiently small. Therefore, matching of frequency response is done at $\omega_k \to 0$. Thus, to obtain desired steady state performance low frequency points is selected with respect to 0.1% bandwidth frequency of the desired reference model. For this, a close proximity in the low frequency zone for CCS is shown in Figure 11. A similar closeness is observed with the other control structures also.

A specific performance index in terms of error i.e., the absolute deviation in gain plot of ideal or complex controller and the PI controller is tabulated in Table 3. Lowest value of absolute deviation in CCS rejects external disturbance faster than others.

The controller parameters for SFCS, proposed PCS, proposed T-DF IMC and proposed CCS are given in Table. 4, Table 5, Table 6 and Table 7, respectively. The control performance using all these controller parameters in corresponding control structure have been checked and satisfactory performance have been observed. The tracking performance of BC have been observed by applying different changing SP command. The LD rejection property has been observed by introducing change in input voltage and duty cycle while converter is operated in prespecified output voltage.

For a fair comparison of control performance among the control structures, the tuning parameter for outer loop is kept same as 0.002. Controllers corresponding to this value are $Q_{SFCS}(s) = 0.0399 + 8.0893/s$ for SFCS proposed by Jha et al.;

$Q_{1PCS}(s) = 0.0399 + 8.0893/s$ and $Q_{2PCS}(s) = 0.1598 + 48.0368/s$ for the proposed PCS; $Q_{1T-DF\ IMC}(s) = 0.0399 + 8.0894/s$ and $Q_{2T-DF\ IMC}(s) = 0.0637 + 16.012/s$ for the proposed T-DF IMC and $Q_{1CCS}(s) = 0.571 + 272.89/s$ and $Q_{2CCS}(s) = 0.0691 + 16.4681/s$ for the proposed CCS. These controller settings have been implemented in their corresponding control scheme for the output voltage regulation of the BC. The performance of the proposed control schemes has also been compared with the work of Jha et al. and Kobaku et al. The work of Jha et al. is based on the parametric independent modelling of the BC whereas Kobaku et al. has considered modified IMC scheme. This makes these works a suitable choice for performance comparison with the proposed methods in this manuscript.

The SP performance has been observed by applying a SP change command of 20V to 25V at 3s while BC was operating with a SP command of 20V. The transient output voltage response of the proposed PCS, proposed T-DF IMC and proposed CCS along with that of the Jha et al. and Kobaku et al. are shown in Figure 12. The comparative performance indices in terms of rise time, settling time, maximum deviation is given in Table 8. The response of proposed PCS and proposed CCS is faster with slight overshoot however, the response of Jha et al. is slowest. The response of proposed T-DF IMC and Kobaku et al. are similar but at starting there is slightly more up and down in the initial stage. The reason for similar response is that both the scheme uses T-DF internal model control scheme. However, the modelling technique used in this work is based on CLT and the experimental response also confirms the acceptance of the proposed modelling technique.

The load disturbance rejection performance has been observed by perturbing input voltage and duty cycle while BC is operating with a prespecified SP command. The input supply is changed from 12V to 14V at t=3s while the load resistance and SP command is set to a constant value of 50Ω and 18V, respectively. The comparative output voltage is shown in Figure 13 and the performance indices are given in Table 8. The proposed PCS and proposed T-DF IMC are faster and least deviation in the output voltage is observed in the case of proposed CCS. The performance of CCS is better whereas Jha et al. has slower response performance.

The LD response is further analyzed by perturbing deliberately the controlling signal i.e., duty cycle. A duty cycle disturbance of $+$ 0.1 step is introduced at t=3s while output voltage is maintained at 20V. The comparative response of output voltage is shown in Figure 14. It is clear that the output voltage is regulated in all the control structures at 18V. However, least deviation in output voltage is observed in the case of proposed CCS with lesser settling time. The proposed PCS has maximum deviation but it settles quickly. The methods Jha et al. and Kobaku et al. have slow response with slightly larger deviation in the output voltage from a preset value.

It is to note that the performance of proposed schemes (i.e., proposed PCS, proposed CCS and proposed T-DF IMC) are comparatively better than the work of Jha et al. and Kobaku et al. And among all the proposed schemes the overall performance

of the proposed CCS is better. The steady state performance of all these methods have been explored extensively and satisfactory performance is observed. However, the steady state response of the proposed CCS scheme is presented here.

The BC is operated with a SP command of 20V, at time t=14s the SP value is increased to 25V and again back at 20V at time t=56s. The response of output voltage, inductor current, input voltage and duty cycle are shown in Figure 15. From the figure, it is observed that the output voltage of the BC tracks the SP command. The load of the BC is increased to 25Ω at time t=28s and returned back to its original value at time t=42s while the SP command to BC was 25V. It is observed that the output voltage follows the SP command and effect of load change on output voltage is rejected by the controller.

The SP tracking performance range of BC is further investigated by applying changing SP command. SP command of 20V, 23V, 26, 29V, 32V, 35V and 38V has been applied and corresponding response is shown in Figure 16. From the figure, it is observed that the proposed CCS control scheme manipulates the duty cycle up to 0.68 $\left(D>0.5\right)$ to track the changing SP command. It is also to note that there is no subharmonic oscillation in the duty cycle of BC is observed while operating at $D>0.5$.

The LD response of the BC is further examined by perturbing the input voltage periodically while it is operated with a fixed SP value. The SP command of 20V is given and the input voltage is perturbed periodically between 11V to 13V. The response of output voltage, inductor current, input voltage and duty cycle are shown in Figure 17. In effect of perturbed input voltage, the proposed control scheme manipulates the duty cycle which ultimately manages the inductor current and as a result the output voltage of the BC is maintained at a prespecified SP value. Thus, robust load disturbance rejection performance of the proposed control schemes has been observed.

## 5. ROBUSTNESS STABILITY ANALYSIS

The development of mathematical model for an actual system is involved with the approximation and linearization of the nonlinear system. For the designing of controller an actual system is approximated to its system model form. Robustness analysis is basically done in order to ensure the stability of the approximated system under parametric uncertainties. Here, the robustness analysis for all the control structures is done with the help of small gain theorem with multiplicative uncertainty. The system is robustly stable if and only if it satisfies the following condition i.e.,

$$\left\|\delta w_I\left(j\omega\right)T\left(j\omega\right)\right\|<1\forall\,\omega\left(-\infty,\infty\right) \tag{48}$$

Where, $T\left(j\omega\right)$ represents the closed-loop complementary sensitivity and $\delta w_I\left(j\omega\right)$ represents the uncertainty bound of the unity feedback control configuration. The expression for $T\left(j\omega\right)$ and $\delta w_I\left(j\omega\right)$ is given by,

$$\left.\begin{aligned} T(j\omega) &= \frac{Q(j\omega)M_{31v/d}(j\omega)}{1+Q(j\omega)M_{31v/d}(j\omega)} \\ \delta w_I(j\omega) &= \left|\frac{G_u(j\omega)-M_{31v/d}(j\omega)}{M_{31v/d}(j\omega)}\right| \end{aligned}\right\} \tag{49}$$

where, $G_u(j\omega)$ is the uncertain plant with multiplicative uncertainty and $M_{31v/d}(j\omega)$ is the nominal system model.

Complementary sensitivity function for SFCS is obtained as

$$T_{SFCS}(j\omega) = \frac{Q_{SFCS}^{PI}(j\omega)M_{31v/d}(j\omega)}{1+Q_{SFCS}^{PI}(j\omega)M_{31v/d}(j\omega)}. \tag{50}$$

Complementary sensitivity function for PCS is obtained as

$$T_{PCS}(j\omega) = \frac{Q_{1PCS}^{PI}(j\omega)M_{31v/d}(j\omega)}{1+Q_{1PCS}^{PI}(j\omega)M_{31v/d}(j\omega)}. \tag{51}$$

Complementary sensitivity function for T-DF IMC is obtained as

$$T_{T-DF\ IMC}(j\omega) = M_{31v/d}(j\omega)Q_{1T-DF\ IMC}^{PI}(j\omega). \tag{52}$$

Complementary sensitivity function for CCS is obtained as

$$T_{CCS}(j\omega) = \frac{Q_{1CCS}(j\omega)M_{11v/i}(j\omega)M_{21i/d}(j\omega)Q_{2CCS}(j\omega)}{1+Q_{2CCS}(j\omega)M_{21i/d}(j\omega)+Q_{1CCS}(j\omega)M_{11v/i}(j\omega)M_{21i/d}(j\omega)Q_{2CCS}(j\omega)} \tag{53}$$

In the proposed method, being a parametric independent model of BC, the uncertainties are considered in the coefficients of its transfer function. The frequency response plot of complementary sensitivity and uncertainty bound of different control structures are shown in Figure 18. From the figure, it is evident that the robustness level of the proposed CCS is maximum and it can bear upto 60% change the coefficients of the model of the BC. However, proposed T-DF IMC and proposed PCS are robustly stable upto 17% and 20% change in parameters. The method proposed by Jha et al. is stable upto 15% change in parametric uncertainty.

### *5.1 Hardware results by perturbing $L$ and $C$ values*

Servo and regulatory response are obtained experimentally and its robustness is tested by perturbing the parametric values of BC. The values of $L$ and $C$ are changed to $6mH$ and $1320\mu F$, respectively. Using the perturbed values, the control structures are tested under change in SP, input voltage and duty cycle disturbance with its corresponding performance indices given in Table 8. A similar trend is noticed in experimental results with same conditions as provided for nominal values are shown in Figure 19.

SP tracking from 20V to 25V is observed when a command of 5V is introduced at 3s. PCS performance seems to be faster while response of Jha et al. is the slowest among all as shown in Figure 19(a). Load disturbance rejection response in case of input voltage and duty cycle is observed where the output voltage and load resistance are kept constant at 20V. PCS and CCS are having an equal amount of deviation whereas the response of Kobaku et al. shows maximum deviation which is observed in Figure 19(b). For duty cycle disturbance of $+0.1$, CCS performs better shown in Figure 19(c) with respect to deviation as compared to others.

## 6. Conclusion

In this manuscript, control of BC with four different control structures have been investigated. These structures are (i) SFCS, (ii) PCS, (iii) T-DF IMC, (iv) CCS. The model obtained through CLT has been used for controller design in these structures. This makes these scheme independent of BC parameter information. Limitations lies in obtaining the model of the system where about <10% and >60% overshoot occur. For >60%, there exists long overshoots with large settling time requiring excessive input changes and for <10%, small overshoots with less settling time finds the experimental CLT difficult to obtain. Proper selection of gain is important while performing the experiment. The controller used in SFCS, PCS, T-DF IMC, and CCS is PI controller whose parameter is obtained through approximate frequency response matching. All the structure performs satisfactorily for SP and LD response. The model of BC is derived for one operating point around $D = 0.33$ and all the control structures have satisfactorily controlled the converter in wide operating range of duty cycle from 0.33 to 0.68. CCS is showing better regulatory performance. Robustness analysis is done using small gain theorem and is validated in hardware setup. CCS is more robust and is showing stable performance with parametric deviation up to 60% in all the coefficients of transfer function of BC. The future work may be extended to other dc-dc converters with constant power loads. This approximation technique can also be applied to fractional order control.

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**Purnima Verma** received B.Tech degree in electrical engineering from Rajkiya Engineering College, Banda, India in 2018. She is currently working on her Ph.D in electrical engineering from National Institute of Technology, Patna, India. Her research interest includes control system and power electronics.

**Md. Nishat Anwar** (Senior Member, IEEE) received his Ph.D. degree in electrical engineering from Indian Institute of Technology (Indian School of Mines), Dhanbad, India in 2015. He obtained his M.Tech

and B.Tech degree from Aligarh Muslim University, Aligarh, India in 2009 and 2007, respectively. His main research interests include sliding mode control, industrial control and automation, active disturbance rejection control, PID controller, and control of power electronic converter. He is currently working as an Assistant Professor in the Department of Electrical Engineering, National Institute of Technology, Patna, India. He is a senior member of the IEEE Control Systems Society, the IEEE Industry Applications Society and a professional member IFAC-ACDOS (Automatic Control and Dynamic Optimization Society).

**List of Figures**

**List of Tables**



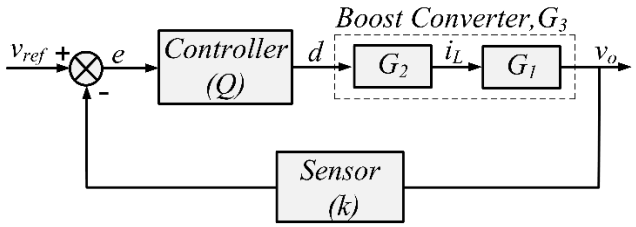



Figure 1. Conventional feedback control structure for BC

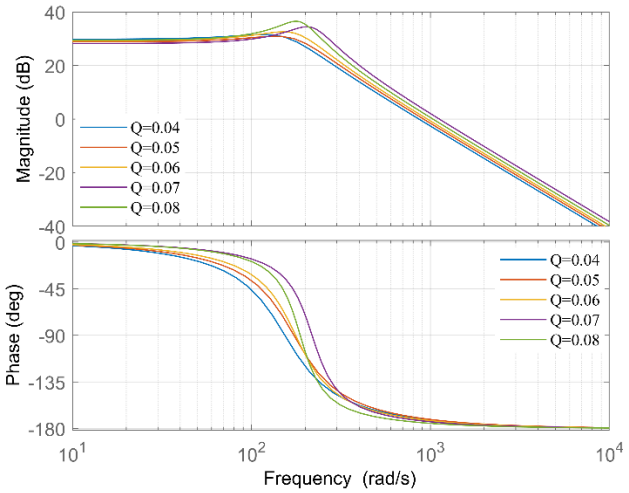



Figure 2. Bode plot of $M_{3jv/d}$ using CLT for different values of proportional controller, $Q$

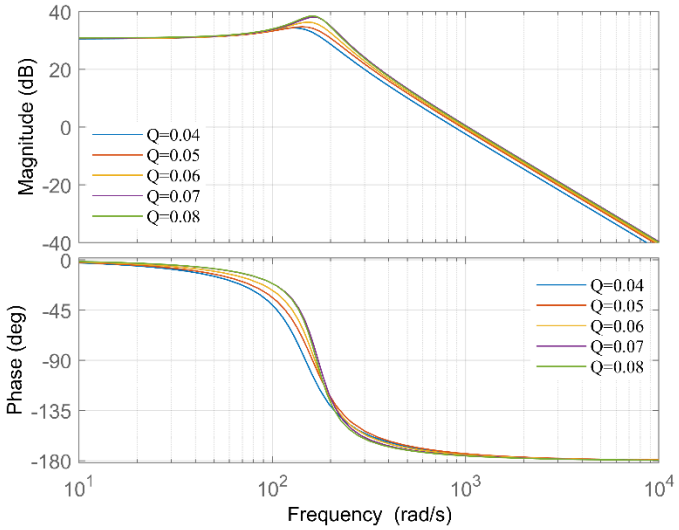



Figure 3. Bode plot of $M_{2ji/d}$ using CLT for different values of proportional controller, $Q$

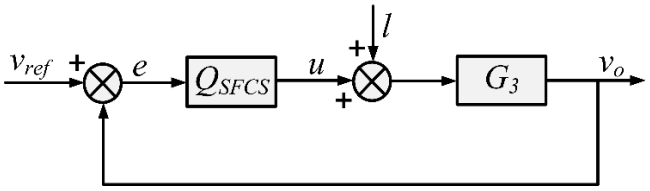



Figure 4. Single feedback control structure (SFCS)

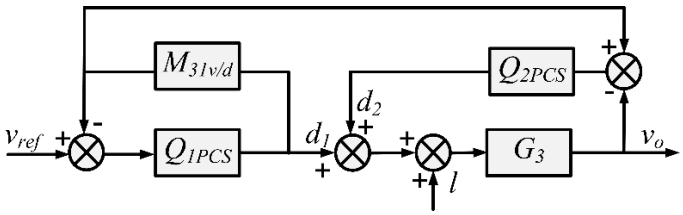



Figure 5. Parallel control structure (PCS)

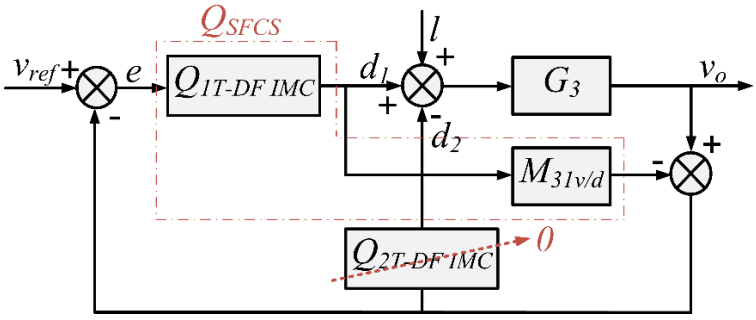


Figure 6. Comparison of Two-DOF IMC structure (T-DF IMC) with SFCS when $Q_{2T-DFIMC}(s)=0$

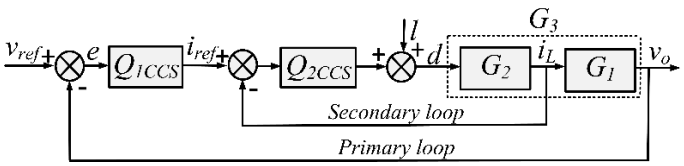



Figure 7. Modified cascade control structure with IMC

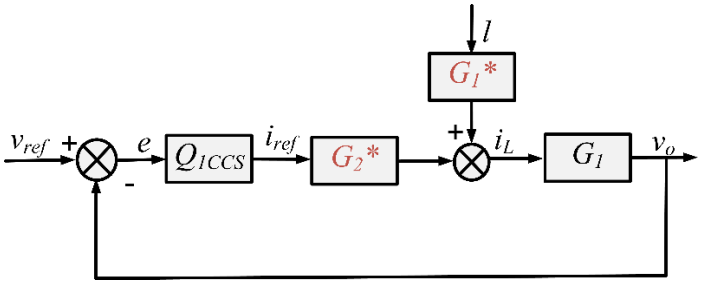



Figure 8. Single loop equivalent of cascade control structure

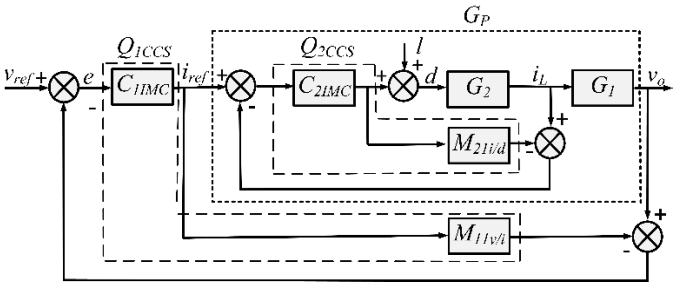



Figure 9. Cascade control structure with IMC

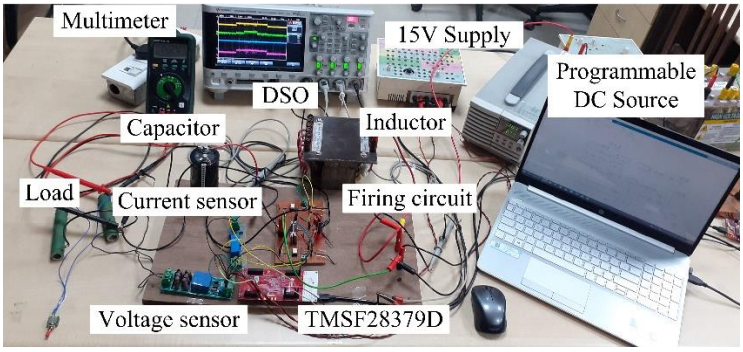



Figure 10. Hardware set up of BC

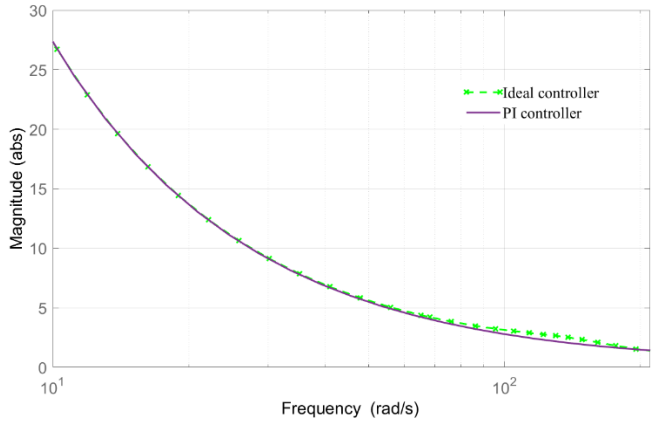



Figure 11. Bode magnitude plot of CCS showing close proximity in the lower frequency zone

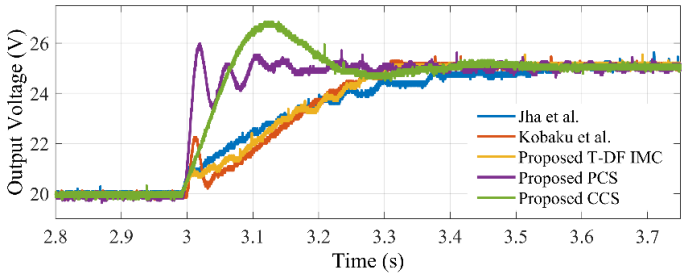



Figure 12. Experimental response of SP change command from 20V to 25V at 3s

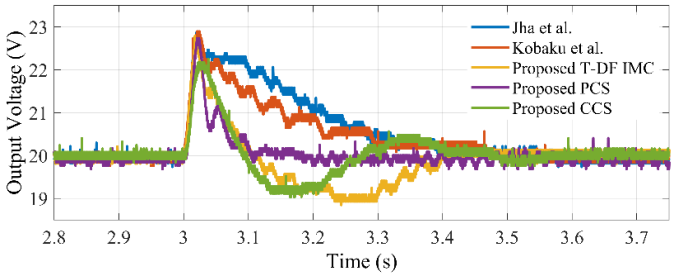



Figure 13. Experimental response of change in input voltage from 12V-14V at 3s

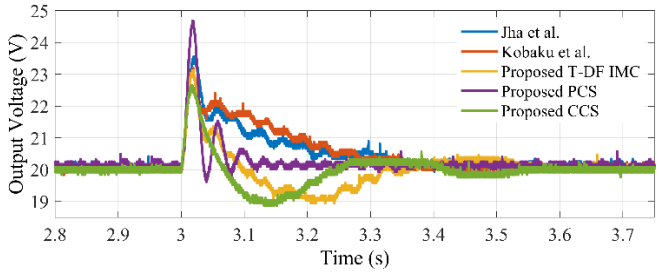



Figure 14. Experimental response of change in duty cycle disturbance of +0.1 at 3s

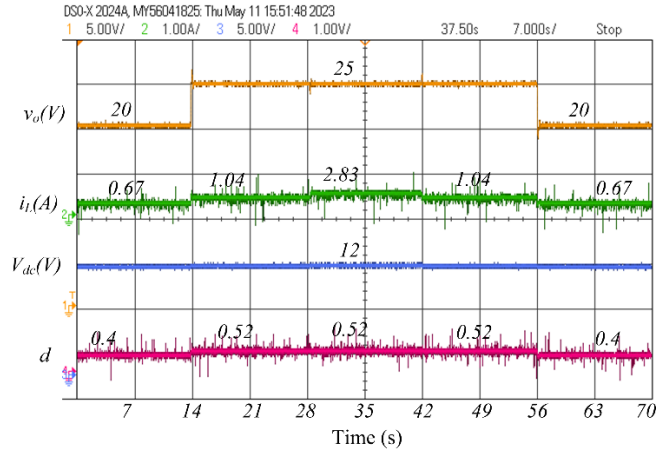



Figure 15. Steady state performance for CCS with SP change and load resistance change

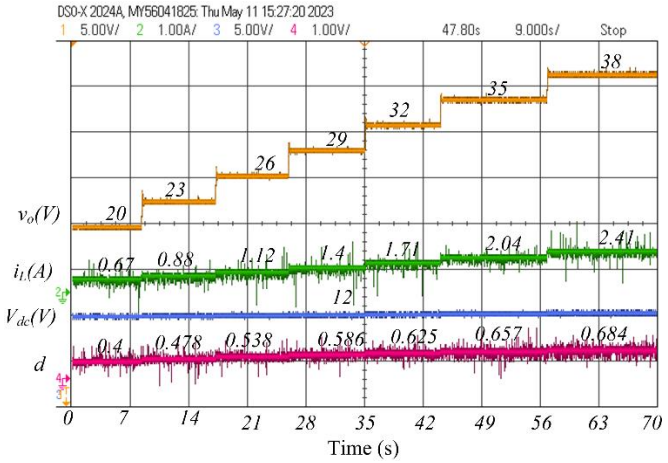



Figure 16. Steady state performance for CCS with SP change for $D > 0.33$

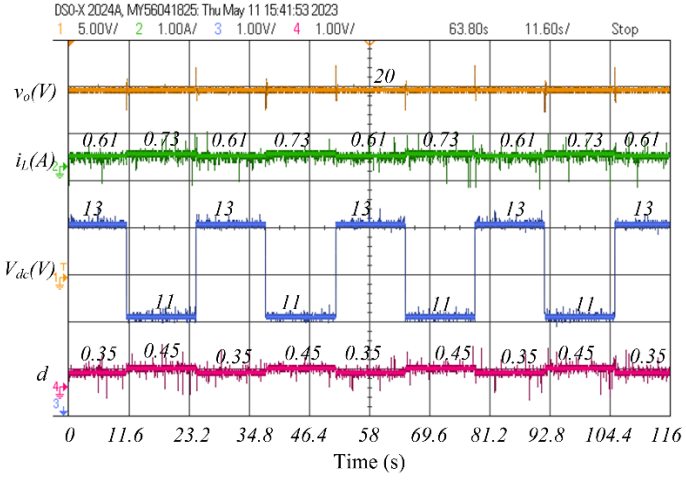



Figure 17. Steady state performance for CCS with periodic supply voltage change

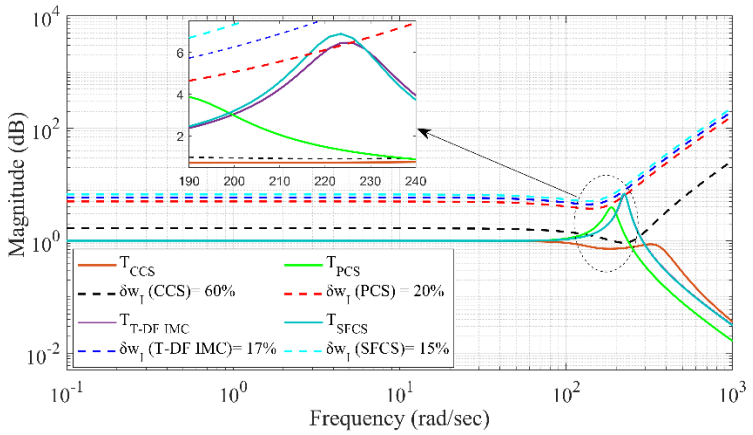
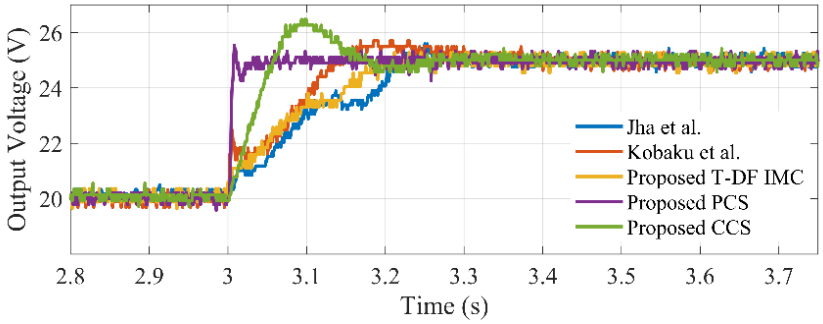
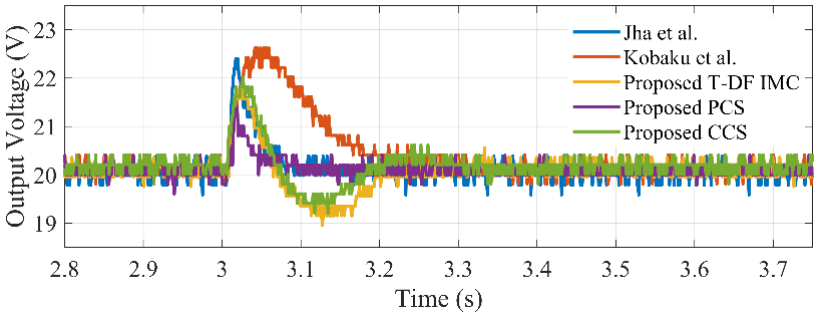


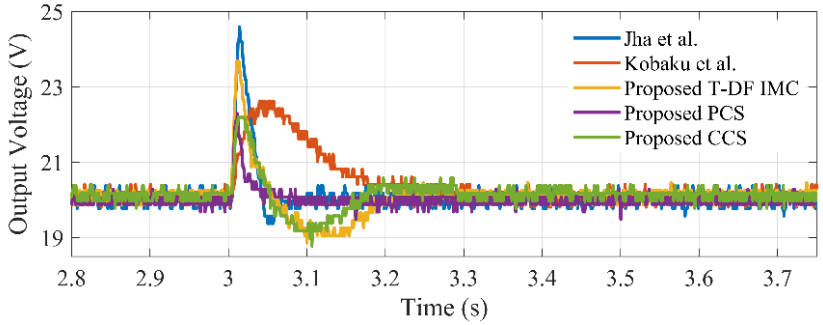

Figure 18. Frequency response magnitude plot of complementary sensitivity and parametric uncertainty of Jha et al., proposed PCS, proposed T-DF IMC and proposed CCS




(a)




(b)



(c)

Figure 19. Experimental response for (a) change in SP command (20V to 25V), (b) input voltage (12V to 14V) and (c) duty cycle disturbance of $+$ 0.1 by perturbing the value of $L$ and $C$ at 3s

Table 1. A comparative review of recent work

| Ref. | Control structure | Modelling technique | Experimental Identification (Yes/No) | Model as a part of controller (Yes/No) | Degree of freedom (Single/ Two) | Control Mode (Voltage/ Current) | Controller used |
|---|---|---|---|---|---|---|---|
| [10] | Double loop | State space averaging technique | No | No | Single | Current | PI controller in both loops |
| [16] | Cascade control structure | State space averaging technique | No | No | Single | Current | PI controller is used in inner loop whereas PI controller is used in outer loop |
| [17] | Cascade control structure | State space averaging technique | No | No | Single | Current | PI controller is used in inner loop whereas IP is used in outer loop |
| [18] | Cascade control structure | State space averaging technique | No | Yes | Single | Current | Self-tuning algorithm with disturbance observers |
| [19] | Cascade control structure | Linear extrapolation based state space averaging technique with current tracking delay | No | Yes | Single | Current | PI compensator with digital peak current controller |
| [20] | Cascade control structure | State space averaging technique with Taylor series expansion | No | No | Single | Current | Input-state linearization controller is used in inner loop whereas linear model predictive control is used in outer loop |
| [21] | Multiloop output feedback system | State space averaging technique | No | No | Two | Voltage | Pole zero cancellation stabilizer as the inner loop controller and adaptive damping stabilizer as the outer loop controller |
| [23] | Multivariable multiloop control structure | State space averaging technique | No | Yes | Single | Voltage | Proportional type controller long with disturbance observer |
| [24] | Single feedback control structure | State space averaging technique | No | No | Two | Voltage | PID controller |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| [25] | Single feedback control structure | State space averaging technique | No | Yes | Two | Voltage | PID controller, IMC controller, ADRC controller |
| [26] | Single feedback control structure | Closed-loop test-based modelling | Yes | Yes | Single | Voltage | PI controller |
| [27] | T-DF IMC | State space averaging technique | No | Yes | Two | Voltage | IMC controller |
| [28] | Single feedback control structure | State space averaging technique | No | No | Single | Voltage | Fractional order PID controller |
| [29] | Feedforward control structure | Discrete state space averaging technique | No | Yes | Two | Voltage | Modified Dahlin's and Vogel-Edgar controller |
| [30] | Single feedback control structure | State space averaging technique | No | No | Two | Voltage | PID controller |
| **Proposed** | SFCS<br>PCS<br>T-DF IMC<br>CCS | Closed-loop test-based modelling | Yes | No<br>Yes<br>Yes<br>No | Single<br>Two<br>Two<br>Single | Voltage<br><br><br>Current | PI controller |

Table 2. Transfer functions for different sets of proportional controller value

| **Proportional controller gain $(Q)$** | **Output voltage to duty cycle transfer function $\left(M_{3jv/d};\ j=1\ to 5\right)$** | **Inductor current to duty cycle transfer function $\left(M_{2ji/d};\ j=1\ to 5\right)$** |
|---|---|---|
| 0.04 | $M_{31v/d}=\frac{7.3121e5}{s^2+140.5s+2.366e4}$ | $M_{21i/d}=\frac{7.442e5}{s^2+102.5s+2.206e4}$ |
| 0.05 | $M_{32v/d}=\frac{8.209e5}{s^2+144.5s+2.836e4}$ | $M_{22i/d}=\frac{8.855e5}{s^2+106.5s+2.606e4}$ |
| 0.06 | $M_{33v/d}=\frac{9.03e5}{s^2+128.8s+3.119e4}$ | $M_{23i/d}=\frac{9.420e5}{s^2+89.9s+2.756e4}$ |
| 0.07 | $M_{34v/d}=\frac{11.18e5}{s^2+108.8s+3.76e4}$ | $M_{24i/d}=\frac{10.340e5}{s^2+76.2s+3.012e4}$ |
| 0.08 | $M_{35v/d}=\frac{10.562e5}{s^2+90.66s+3.508e4}$ | $M_{25i/d}=\frac{10.412e5}{s^2+71.9s+2.990e4}$ |

Table 3. Absolute deviation in gain plot of ideal and PI controller

| Structures | SP controller | LD controller | SP controller | LD controller | SP controller | LD controller | Inner loop | Outer loop |
|---|---|---|---|---|---|---|---|---|
| | SFCS | | T-DF IMC | | PCS | | CCS | |
| **Absolute deviation in gain plot of ideal or complex controller and PI** | 0.0055 | 0.0146 | 0.0055 | 0.0029 | 0.0055 | 0.0146 | 0.0025 | 0.8035 |
| **Bandwidth** | 321.14 | 321.14 | 321.14 | 254.42 | 321.14 | 254.42 | 713.65 | 321.14 |
| **Frequency points chosen** | 0.320 | 0.320 | 0.274 | 0.248 | 0.282 | 0.246 | 0.712 | 0.316 |

Table 4. PI controller parameters for SFCS

| $\lambda_{SFCS}$ | $K_{P1,SFCS}$ | $K_{I1,SFCS}$ | $K_{P2,SFCS}$ | $K_{I2,SFCS}$ |
|---|---|---|---|---|
| 0.001 | 0.088 | 16.1787 | 0.3519 | 192.1471 |
| 0.002 | 0.039 | 8.0893 | 0.1598 | 48.0368 |
| 0.003 | 0.024 | 5.3929 | 0.0957 | 21.3497 |
| 0.004 | 0.016 | 3.2357 | 0.0637 | 12.0092 |
| 0.005 | 0.011 | 3.2357 | 0.0445 | 7.6859 |
| 0.006 | 0.008 | 2.6964 | 0.0317 | 5.3374 |
| 0.007 | 0.006 | 2.3112 | 0.0225 | 3.9214 |
| 0.008 | 0.004 | 2.0223 | 0.0157 | 3.0023 |

Table 5. PI controller parameters for PCS

| $\lambda_{1PCS}$ | $\lambda_{2PCS}$ | $K_{P1,PCS}$ | $K_{I1,PCS}$ | $K_{P2,PCS}$ | $K_{I2,PCS}$ |
|---|---|---|---|---|---|
| 0.001 | 0.001 | 0.0880 | 16.1787 | 0.3519 | 192.1471 |
| 0.002 | 0.001 | 0.0399 | 8.0893 | 0.3519 | 192.1471 |
| 0.003 | 0.001 | 0.0239 | 5.3929 | 0.3519 | 192.1471 |
| 0.004 | 0.001 | 0.0159 | 4.0447 | 0.3519 | 192.1471 |
| 0.005 | 0.001 | 0.0111 | 3.2357 | 0.3519 | 192.1471 |
| 0.001 | 0.002 | 0.0880 | 16.1787 | 0.1598 | 48.0368 |
| 0.002 | 0.002 | 0.0399 | 8.0893 | 0.1598 | 48.0368 |

Table 6. PI controller parameters for T-DF IMC

| $\lambda_{1T-DFIMC}$ | $\lambda_{2T-DFIMC}$ | $K_{P1,T-DFIMC}$ | $K_{I1,T-DFIMC}$ | $K_{P2,T-DFIMC}$ | $K_{I2,T-DFIMC}$ |
|---|---|---|---|---|---|
| 0.001 | 0.005 | 0.0880 | 16.178 | 0.0061 | 2.5620 |
| 0.002 | 0.005 | 0.0399 | 8.0893 | 0.0061 | 2.5620 |

| | | | | | |
|---|---|---|---|---|---|
| 0.003 | 0.005 | 0.0239 | 5.3930 | 0.0061 | 2.5620 |
| 0.004 | 0.005 | 0.0159 | 4.0447 | 0.0061 | 2.5620 |
| 0.005 | 0.005 | 0.0111 | 3.2358 | 0.0061 | 2.5620 |
| 0.002 | 0.002 | 0.0399 | 8.0894 | 0.0637 | 16.012 |
| 0.002 | 0.003 | 0.0399 | 8.0894 | 0.0317 | 7.1167 |
| 0.003 | 0.003 | 0.0239 | 5.3930 | 0.0317 | 7.1167 |

Table 7. PI controller parameters for CCS

| $\lambda_{1CCS}$ | $\lambda_{2CCS}$ | $K_{P1,CCS}$ | $K_{I1,CCS}$ | $K_{P2,CCS}$ | $K_{I2,CCS}$ |
|---|---|---|---|---|---|
| 0.002 | 0.002 | 1.1712 | 272.89 | 0.0270 | 7.4106 |
| 0.002 | 0.001 | 0.6254 | 272.89 | 0.0615 | 14.8213 |
| 0.002 | 0.0009 | 0.571 | 272.89 | 0.0691 | 16.4681 |
| 0.002 | 0.0008 | 0.571 | 272.89 | 0.0787 | 18.5266 |
| 0.002 | 0.0007 | 0.4617 | 272.89 | 0.091 | 21.1733 |

Table 8. Performance indices for different control structures

| | **Parameters** | **SFCS (Jha et al.)** | **Kobaku et al.** | **Proposed T-DF IMC** | **Proposed PCS** | **Proposed CCS** |
|---|---|---|---|---|---|---|
| | | | **Nominal values** | | | |
| **Set-point response** | Rise time (s) | 0.318 | 0.22 | 0.21 | 0.24 | 0.12 |
| | Settling time (s) | 0.495 | 0.29 | 0.283 | 0.34 | 0.28 |
| | Maximum deviation(V) | - | - | - | 2 | 1.8 |
| **Input voltage rejection response** | Maximum deviation (V) | 2.357 | 1.71 | 1.683 | 1.93 | 1.27 |
| | Settling time (s) | 0.561 | 0.30 | 0.293 | 0.35 | 0.32 |
| **Duty cycle rejection response** | Maximum deviation (V) | 3.698 | 3.31 | 3.296 | 3.62 | 2.0 |
| | Settling time (s) | 0.473 | 0.187 | 0.185 | 0.24 | 0.25 |
| | | | **Perturbed values** | | | |
| **Set-point response** | Rise time (s) | 0.195 | 0.04 | 0.148 | 0.01 | 0.10 |
| | Settling time (s) | 0.29 | 0.22 | 0.21 | 0.03 | 0.3 |
| | Maximum deviation(V) | - | 1.12 | - | 0.34 | 0.46 |
| **Input voltage rejection response** | Maximum deviation (V) | 2.39 | 2.42 | 1.56 | 1.4 | 1.4 |
| | Settling time (s) | 0.07 | 0.27 | 0.21 | 0.09 | 0.18 |
| **Duty cycle rejection** | Maximum deviation (V) | 4.2 | 2.42 | 3.47 | 2.09 | 1.8 |

| | | | | | | |
|---|---|---|---|---|---|---|
| **response** | Settling time (s) | 0.1 | 0.25 | 0.21 | 0.08 | 0.18 |