Comprehensive Stochastic Analysis Method for Tree-Type PDNs and Ground Pollution on Mixed-Signal PCBs

Milad Mehri*
Affiliation: Department of Electrical Engineering, Faculty of Engineering, Alzahra University, Tehran, Iran.
Address: Khwarizmi Building, Alzahra University, Dehvanak St., Dehvanak, Tehran, Iran.
Email: m.mehri@alzahra.ac.ir
Office Phone: +9821-85692151
Cell Phone: +98912-4840234

Abstract **- In this paper, a stochastic analysis method is proposed for extraction and evaluation of power distribution map (PDM) in system printed circuit board (PCB). This is conducted based on some high level data including placement and routing geometry, power distribution network (PDN), component package parasitic, and voltage regulator module (VRM). A simple model for supply current of two constituent blocks of electronic systems is analytically extracted. The worst-case simultaneous operation of all consumers are considered for PDM extraction. The approach is applied to a specific designed and fabricated mixed signal board. PDM is beneficial in the placement process of decoupling capacitance or noisy components in an optimum and right location. Also, the proposed approach can be considered as a verification step of PCB design flow and be applicable before routing only based on the placement data of components of the system. This enables the designer to predict the upcoming problems in layout and hastens the process of design verification.**

Keywords **- Power distribution network, stochastic analysis, PCB layout, decoupling capacitor, ground pollution.**

1. INTRODUCTION

The design of an electronic system printed circuit board (PCB) layout is a challenging and time-consuming process. The placement and routing of the devices are challenging processes and need precise automated and manual engineering. In [1], a target-impedance extraction based optimal power distribution network (PDN) design methodology is proposed. The suggested methodology uses both measured current spectra and hierarchical PDN-Z models for target-Z calculation, instead of using the current profile of a chip power models. In [2] presents an efficient methodology based on boundary integration to calculate the dc and ac impedance of power distribution networks for arbitrary-shape and multilayer printed circuit boards. The proposed method adopts a boundary element method to extract inductances for the arbitrary parallel-plane shapes. [3] presents a novel measurement and analysis of electromagnetic information leakage from printed circuit board power delivery network of cryptographic devices. They verified that the EM information leakage depends on the intensity of dominant field distribution on the PCB PDN using the proposed method. In [4] a full-system level noise coupling simulation technique is evaluated on the demonstrator representing a multi-chip mixed-signal PCB for establishing the noise aware design strategy and methodology. In [5], authors put forward a novel EMI behavioral model based common-mode system noise prediction method considering multinoise coupling. Since coupling of multiple converter noises forms the system noise, the effect of such multinoise coupling on system noise prediction is investigated. An ever-increasing concern in electronic literature is EMC/EMI issue, [6] - [8]. The fast-switching transistors and vast number of electronic goods with has led to concerns and guideline over their generation of EMI problems, [9]. Different approaches and policies are considered and approved for modeling and alleviation of the radiated and conducted EMI between electronic devices, [10] and [11]. The populated interconnect PCB is usually used in handheld devices to escalate the density of the circuit, [12]. One of the interesting and complex parts of any PCB is the PDN plan, [13] and [14]. Proper power delivery to building block results to better performance of the system. The SI/PI analysis of system involves precise design of PDN, [15]. Power distribution map (PDM) helps designer in placement and routing steps and EMC/EMI problems assessment [16] and [17]. In addition, it helps to decoupling capacitances placement in correct position. The power distribution of mixed-signal system is a growing worry due to switching voltage variations, [16]. In addition to the power supply switching frequency components, the key reason for a dirty power supply, i.e. ripple and fluctuation in DC voltage level in a mixed-signal electronic system is the digital gates transient switching. Analyses of mixed-signals on PCBs are showed in [18]. CMOS logic gate consumes energy and draws current at transition times of its input and output signals, [19]. The vast number of CMOS gates in highly dense digital system for processing and saving data, entail accurate design and behavior modeling, [20]. Time delay, DC characterization, switching thresholds, and power consumption are the main parameters of CMOS gates [19] – [24]. Definitely, the latter one, is the most important parameters as the technology shrinks and becomes much denser. In addition, there is a large-size CMOS buffer gate in each input/output (I/O) pin of any digital device for increasing the pin current capability and driving strength.

One of the important method for lessening power supply variation is using decoupling capacitors in PDN. In general form, capacitor placement is based on target impedance, which provides a quantity for PDN design, [25] to [27]. In [25], by dividing a capacitor into segments, a modeling approach for the power/ground plane is obtained. But, impedance distribution is not

sufficient for extraction of PDM; It also requires to have current drawn by each device of the system. Due to continuous transistor scaling in ICs, as supply voltage tends to decrease, voltage variation margin progressively reduces, [26]. In [28] an input impedance including information of the impedance matrix, is proposed to analyze PDNs. In [29] an approach is proposed for the modeling, analysis, and design of a PDN. Distributed port is used to measure the characterization of the power distribution network.

Available power integrity CAD tools can extract the PDM of a board based on DC power consumption of building blocks, not frequency dependent one. Particularly in high frequency circuits and mixed-signal boards, this deficiency emerges more. For accurate design of PDN in a board, designer needs to know:

1. frequency dependent supply current,
2. consuming supply cross-correlation of operating building blocks of the system, and
3. grounding quality on PCB.

For insertion of appropriate decoupling capacitance in right position, mentioned information is necessary. In this research the current drawn from two essential active devices is analytically derived based on stochastic input signaling. The PDN is considered under full load in worst-case situation while all consumer devices are operating simultaneously. In this paper a simple systematic model is proposed for different parts of PDN, including voltage regulator, transmission lines, decoupling capacitors, and building blocks. The focus of this paper is to propose a stochastic analysis and extraction method for PDM, and ground plane pollution, and component and decoupling capacitance placement. Most of the time, the placement of a component on a PCB is dominated by its package, corresponding pin configurations, and other interconnected component locations. However, power distribution may apply another contradictory restriction. The supply drawn current will find its return path in least impedance route.

If the ground is implemented with a solid plane, simultaneous insertion of these current will pollute the zero voltage assumption of this plane. Unusually, this phenomenon happens in high frequency RF circuits and mixed-signal PCBs. Extraction of the PDM in a system, needs to have component placement/routing, distribution network parasitic, and each component individual supply current. The supply current of each block depends on five main parameters, including implementation technology, structural topology, physical design values, input signals spectral density, and output load impedance. Thorough investigation of power integrity (PI) in a simple model of PDN for an electronic system shown in Fig. 1, entails modeling of four parts, including consumer, distributer, modifier, and generator.

The paper organization is as follows. Stochastic analysis of supply current for essential constituent blocks of system are in Section 2. Section 3 contains analytical derivations for extraction of PDM based on distributed tracing and component placement. Consuming supply cross-correlation of operating building blocks on PCB is discussed in Section 4. Also, the ground plane pollution due to supply current insertion is discussed in this section. Verifications are done in Section 5. Finally, the paper ends with conclusion and reference.

2. SUPPLY CURRENT OF CONSUMER

Due to stochastic nature of input signals to a block, power spectral density (PSD) of current signals is studied. In the following sub-section, the PSD of supply current signal i_{DD} drawn by two main constituent building blocks of electronic systems including amplifier and CMOS gate are derived. Amplifier, as a fundamental constituent block of every analog system is chosen for investigation of its effect on power supply integrity. In addition, in digital integrated circuits every I/O pins has a CMOS buffer gate for powerful driving of external connecting traces. Therefore, this essential gate is chosen for investigation.

2.1 General Purpose Amplifier

For estimation of supply current in a constituent block of a system, the current signal i_{DD} drawn from the power supply v_{DD} should be estimated.

For a single stage general purpose amplifier shown in Fig. 2-A, one should extract the relation between i_{DD} and v_{in} based on other circuit parameters, like different impedances Z_i, transistor bias, and physical dimension. This current is a function of different parameters including Equation 1,

$$i_{DD} = f\left(v_{in}, Z_{Mi}, Z_{Mf}, Z_{Mo}, Z_L, v_{DD}, \frac{W}{L}, Tech, Temp\right) \qquad (1)$$

where, Z_{Mi} is the gate impedance, Z_{Mf} is the source impedance, Z_{Mo} is the drain impedance of the transistor, and Z_L is the load impedance of the transistor load. Also, $\frac{W}{L}$ is the width/length of the transistor. The general small signal model for a transistor is shown in Fig. 2-B. Using KCL and KVL for single stage amplifier shown in Fig. 2-A results,

$$\frac{v_i - v_f}{Z_{if}} + \frac{v_i - v_{in}}{Z_{Mi} + Z_{in}} + \frac{v_i - v_{out}}{Z_{io}} = 0 \qquad (2)$$

$$\frac{v_f}{Z_{Mf}} + \frac{v_f - v_i}{Z_{if}} + \frac{v_f - v_{out}}{Z_{of}} - g_m(v_i - v_f) = 0 \qquad (3)$$

$$\frac{v_{out}}{Z_{Mo} \parallel Z_L} + \frac{v_{out} - v_i}{Z_{io}} + \frac{v_{out} - v_f}{Z_{of}} + g_m(v_i - v_f) = 0 \qquad (4)$$

where Z_{if} is the input impedance, Z_{of} is the output impedance, Z_{io} is the impedance between input and output ports, and g_m is the trans-conductance of the transistor. Power supply pin current signal i_{DD} is,

$$i_{DD} = -\frac{v_{out}}{Z_{Mo}} = G_i v_{in} \qquad (5).$$

Using Equation 2 to Equation 5 one can derive the relation Equation 6 between i_{DD} and the input voltage v_{in}, source and load impedances Z_{in} and Z_L, transistor small signal parameters, as summarized in Table I, and other impedances in the topology Z_{Mi}, Z_{Mo}, and Z_{Mf}. Other MOS parasitic capacitances like source-bulk capacitor C_{SB} and drain-bulk capacitor C_{DB} can be considered in Z_{Mf} and Z_L.

$$G_i = \frac{\left(\frac{(\frac{1}{Z_{Mo}})\frac{(\frac{1}{Z_{Mi}+Z_{in}})(\frac{1}{Z_{if}}+g_m)}{\frac{1}{Z_{if}}+\frac{1}{Z_{Mi}+Z_{in}}+\frac{1}{Z_{io}}}}{\frac{1}{Z_{Mf}}+\frac{1}{Z_{if}}+\frac{1}{Z_{of}}+g_m-\frac{\frac{1}{Z_{if}}+g_m}{1+\frac{Z_{if}}{Z_{Mi}+Z_{in}}+\frac{Z_{if}}{Z_{io}}}} \right)\left(\frac{1}{Z_{Mf}}+\frac{1}{Z_{if}}-\frac{\frac{1}{Z_{io}}+\frac{1}{Z_{if}}}{1+\frac{Z_{if}}{Z_{Mi}+Z_{in}}+\frac{Z_{if}}{Z_{io}}} \right) - (\frac{1}{Z_{Mo}})\left(\frac{(\frac{1}{Z_{Mi}+Z_{in}})(\frac{1}{Z_{io}}+\frac{1}{Z_{if}})}{\frac{1}{Z_{if}}+\frac{1}{Z_{Mi}+Z_{in}}+\frac{1}{Z_{io}}} \right)}{\frac{Z_{Mo}+Z_L}{Z_{Mo}Z_L}+\frac{1}{Z_{io}}+\left(\frac{\frac{1}{Z_{of}}+\frac{1}{Z_{io}}+\frac{1}{Z_{if}}+g_m}{\frac{1}{Z_{Mf}}+\frac{1}{Z_{if}}+\frac{1}{Z_{of}}+g_m-\frac{\frac{1}{Z_{if}}+g_m}{1+\frac{Z_{if}}{Z_{Mi}+Z_{in}}+\frac{Z_{if}}{Z_{io}}}} \right)\left(\frac{1}{Z_{Mf}}+\frac{1}{Z_{if}}-\frac{\frac{1}{Z_{io}}+\frac{1}{Z_{if}}}{1+\frac{Z_{if}}{Z_{Mi}+Z_{in}}+\frac{Z_{if}}{Z_{io}}} \right) - \frac{1}{\frac{Z_{io}}{Z_{if}}+\frac{Z_{io}}{Z_{Mi}+Z_{in}}+1}\left(\frac{1}{Z_{io}}+\frac{1}{Z_{if}} \right)} \qquad (6)$$

2.2 Random Analog Input Signals

For stochastic process v_{in}, one can write,

$$PSD(V_{in}(f)) = F(R_{v_{in}}(\tau)) = \int_{-\infty}^{\infty} R_{v_{in}}(\tau) e^{-j2\pi f\tau} d\tau = \int_{-\infty}^{\infty} E(v_{in}(t) v_{in}(t-\tau)) e^{-j2\pi f\tau} d\tau \qquad (7)$$

where $R_{v_{in}}$ is the autocorrelation of v_{in} and $E(.)$ is the stochastic mean function. Considering Equation 8 for dependence of $v_{in}(t)$ to its random variables, amplitude X, frequency Ω, phase Φ, and also, its deterministic variable t time,

$$v_{in}(t) = g(X, \Omega, \Phi, t) = X \sin(\Omega t + \Phi) \qquad (8)$$

results

$$R_{v_{in}}(\tau) = \iiint g(X, \Omega, \Phi, t) g(X, \Omega, \Phi, t-\tau) P_{X\Omega\Phi}(x, \omega, \varphi) dx d\omega d\varphi \qquad (9).$$

Random variables, X, Ω, Φ are independent and therefore, joint probability density function (PDF) $P_{X\Omega\Phi}(x, \omega, \varphi)$ can be written as

$$P_{X\Omega\Phi}(x,\omega,\varphi) = P_X(x)P_\Omega(\omega)P_\Phi(\varphi) \quad (10).$$

If random variable Φ has an uniform PDF in $(0,2\pi)$, v_{in} is a wide-sense stationary (WSS) process, [30]. The $P_\Omega(\omega)$ depends on the frequency content of v_{in}, where could choose low-, mid-, and high- frequency spectrum; It is uniformly distributed in bandwidth, [30]. For $P_X(x)$ one can suppose a normal distribution for $P_X(x)$ with variance and mean values as σ_X^2 and m_X, [30].

$$P_\Phi(\varphi) = \begin{cases} \frac{1}{2\pi} & 0 < \varphi < 2\pi \\ 0 & o.w. \end{cases} \quad (11)$$

$$P_\Omega(\omega) = \begin{cases} \frac{1}{\omega_{MAX} - \omega_{MIN}} & \omega_{MIN} < \omega < \omega_{MAX} \\ 0 & o.w. \end{cases} \quad (12)$$

$$P_X(x) = \frac{1}{\sqrt{2\pi}\sigma_X}\exp(-\frac{(x-m_X)^2}{2\sigma_X^2}) \quad (13)$$

where, $\omega_{MIN} = 2\pi f_{MIN}$ and $\omega_{MAX} = 2\pi f_{MAX}$ are the minimum frequency and maximum frequency of the input signal. Using Equation 11 to Equation 13, and doing integration of Equation 9 results

$$R_{v_{in}}(\tau) = \frac{\sigma_X^2 + m_X^2}{2(\omega_{MAX} - \omega_{MIN})}(\frac{\sin(\tau\omega_{MAX})}{\tau} - \frac{\sin(\tau\omega_{MIN})}{\tau}) \quad (14).$$

Doing the integration of Equation 7 by substituting Equation 14 results

$$PSD(V_{in}(f)) = \frac{\sigma_X^2 + m_X^2}{4(f_{MAX} - f_{MIN})} \qquad f_{MIN} \lhd |f| \rhd f_{MAX} \quad (15).$$

Finally, using Equation 5 and Equation 15, results

$$PSD(i_{DD}(f)) = |G_i(f)|^2\ PSD(V_{in}(f)) = |G_i(f)|^2\ \frac{\sigma_X^2 + m_X^2}{4(f_{MAX} - f_{MIN})} \quad (16).$$

Relation Equation 16 is the PSD of current signal drawn by single stage amplifier from power supply where its input signal v_{in} is a stochastic process described by Equation 8.

2.3 Digital Drivers

For extraction of the PSD of current signal i_{DD} drawn from power supply for a digital gate shown in Fig. 3-A,. An efficient and correct enough waveform for current drawn from v_{DD} when a switching happens in digital gate is a triangle shape, as shown in Fig. 4. Both transitions take place in rise- or fall-time of the gate. Meanwhile, the output linearly goes high (V_{dd}) or low level (gnd), [31]. For a single transition from high to low and low to high levels, the input voltage and supply current signals are consisted of two base functions, as shown in Fig. 3-B. In this figure, the input signal is a pulse function; the corresponding output signal will be a pulse signal with rise time (t_r) and fall time (t_f). The transition time τ can be considered as t_r and/or t_f in rise and/or fall transitions. As explained before, the supply current signal (drain current of PMOS) is consisted of two triangle signal which happens in transition times. For a sequence of bits, as input signal, these base functions repeat for every input changing logic level. Having the gate and input signal parameters, the PSD of current signal i_{DD} can be extracted.

Parameter i_{MAX} contains the gate parameters, like the gate size, technology, and loading effect. The maximum current flowing in MOSs in short circuit condition i_{MAX}, can be approximated by alpha-power law model for short channel transistors (Equation 17), [20]. Parameter α varies between 2 (for long channel devices) and 1 (very short channel devices) to model short channel effect of the transistor. Based on [32], for the CMOS buffer i_{MAX} can be estimated from Equation 18

$$i_D = \begin{cases} k_s(v_{GS} - v_{TH})^{\alpha}(1+\lambda v_{DS}) & saturation \\ k_l(v_{GS} - v_{TH})^{\frac{\alpha}{2}} v_{DS} & linear \\ k_{sub} e^{\frac{\beta}{\eta}(v_{GS} - v_{TH})}\left[1 - e^{-\beta v_{DS}}\right] & sub-threshold \end{cases} \quad (17)$$

$$i_{MAX} = k_s(\frac{V_{dd}}{2} - v_{TH})^{\alpha}(1+\lambda\frac{V_{dd}}{2}) \quad (18)$$

where k_{sub}, k_l, k_s, α, β, η, λ and v_{TH} are the parameters of alpha-power model for NMOS transistor, [19] and [20].

2.4 Random Digital Input Signals

In digital circuit, the input signal is a random process which can be considered in two main categories:

1. random digital pulse-amplitude modulated signal, and
2. random telegraph wave signal.

For synchronous sections in digital systems, the random pulse-amplitude modulated signal is appropriate for voltages on interconnection traces. Furthermore, in asynchronous sections, the random telegraph wave signal is suitable for voltages on interconnection traces. For a digital pulse-amplitude modulated (PAM) signal $v_{in}(t)$ is consisted of a base function $p(t)$ as shown in Fig. 5. For a random telegraph wave (RTW) signal, $v_{in}(t)$ makes independent random jumps between two values, V_{dd} and 0 with equal probability, as shown in Fig. 6. The number of jumps per unit time has Poisson distribution function with μ being the average jump rate.

For a CMOS buffer gates, during transition times the current is drawn from power supply, [31]. In other time of operation, there is merely leakage and subthreshold currents. Therefore, transition current is a function of input voltage as,

$$i_{DD}(t) = \frac{-1}{V_{dd}}\frac{dv_{in}(t)}{dt} * p_i(t - \frac{\tau}{2}) \quad (19)$$

$$I_{DD}(f) = \frac{-j2\pi f}{V_{dd}} V_{in}(f) P_i(f) e^{-j\pi\tau f} \quad (20).$$

The operator * in Equation 19 is the convolution. Using Equation 20 the relation between the PSD of current signal i_{DD} and v_{in} can be written as

$$PSD(i_{DD}(f)) = \frac{4\pi^2 f^2}{V_{dd}^2} |P_i(f)|^2 \; PSD(V_{in}(f)) \quad (21)$$

where $P_i(f)$ is Fourier transform of $p_i(t)$, the base function of current signal $i_{DD}(t)$.

For PAM signal, the PSD of $V_{in}(f)$ can be estimated as, [33]

$$v_{in}(t) = \sum_k a_k p_v(t - kT) \quad (22)$$

$$PSD(V_{in}(f)) = \frac{\sigma_a^2}{T}|P_v(f)|^2 + (\frac{m_a}{T})^2 \sum_{n=-\infty}^{\infty} |P_v(\frac{n}{T})|^2 \, \delta(f - \frac{n}{T}) \quad (23)$$

where m_a and σ_a^2 are the average and variance of a_k, respectively. It should be stated that in Equation 23, it is assumed that a_ks are uncorrelated. For a bit sequence signal a_k, if the probability of happening '0' and '1' be equal and statistically independent, therefore $m_a = 0.5$ and $\sigma_a^2 = 0.25$. Also, $P_v(f)$ is Fourier transform of $p_v(t)$ from Equation 24 and T is the period of happening a $p_v(t)$ in $v_{in}(t)$,

$$P_v(f) = V_{dd} W(\frac{\sin(\pi fW)}{\pi fW}) = V_{dd} W \sin c(fW) \quad (24).$$

For RTW signal, the PSD of $V_{in}(f)$ can be estimated from Equation 25, [33]

$$PSD(V_{in}(f)) = \frac{V_{dd}^2}{4\mu[1+(\frac{\pi f}{\mu})^2]} + \frac{V_{dd}^2}{4}\delta(f) \quad (25).$$

Also, $P_i(f)$ is Fourier transform of $p_i(t)$ from Equation 26,

$$P_i(f) = \frac{i_{MAX}\tau}{2}(\frac{\sin(\frac{\pi f \tau}{2})}{\frac{\pi f \tau}{2}})^2 = \frac{i_{MAX}\tau}{2}\sin c^2(\frac{f\tau}{2}) \quad (26).$$

3. PDM EXTRACTION

There are two main sources of power integrity violation on PDM; the VRM generated contribution and the working blocks generated share. In the following of the paper, both contributions are extracted analytically. The effect of each building block on PDM is estimated in this section. In Section 4, building block consuming supply cross-correlation is studied more.

3.1 Distributer

Consider a PDN with a tree structure. All consumer block VDD pin are connected to each other and finally to the VRM through transmission lines in a tree shape graph. This tree ends in HEAD nodes. This node is directly connected to the VDD pin of each block. An example of PDN layout is shown in Fig. 7. In this PDN, there are five consumer blocks in position (X_i, Y_i) for $i = 1$ to 5, a VRM in position $(X_{\mathrm{VRM}}, Y_{\mathrm{VRM}})$, and a tree structure for PDN.

For mathematical derivations, first of all, some parameters should be defined as follows:

- Z_{Lk} : Load impedance k^{th}
- Z_{0k} : Characteristic impedance of transmission line connected to load k^{th}
- γ_k : Propagation constant of transmission line connected to load k^{th}
- l_k : Length of transmission line connected to load k^{th}
- $Z_{0\mathrm{MN}}$: Characteristic impedance of transmission line between nodes M and N
- γ_{MN} : Propagation constant of transmission line between nodes M and N
- l_{MN} : Length of transmission line between nodes M and N
- Z_{ink} : The input impedance seen from a plain transmission line (no junction) connected to load k^{th}:

$$Z_{ink} = Z_{0k}\frac{Z_{Lk} + Z_{0k}\tanh(\gamma_k l_k)}{Z_{0k} + Z_{Lk}\tanh(\gamma_k l_k)} \quad (27)$$

- $Z_{l\mathrm{MN}@Z_{\mathrm{N}}}$: The input impedance seen from a complex transmission line between nodes M and N, which its load is Z_{N}:

$$Z_{lMN@Z_N} = Z_{0MN}\frac{Z_N + Z_{0MN}\tanh(\gamma_{MN} l_{MN})}{Z_{0MN} + Z_N\tanh(\gamma_{MN} l_{MN})} \quad (28)$$

- Z_{N} : The impedance seen in junction node N. It's the parallel impedance of all branches (plain and/or complex transmission lines; Z_{ini}s and $Z_{l\mathrm{NM}@Z_{\mathrm{M}}}$s) connected to the junction node N:

$$Z_N = Z_{ini} \parallel Z_{inj} \parallel \ldots Z_{ink} \ldots \parallel Z_{lNM@Z_M} \parallel Z_{lNO@Z_O} \parallel \ldots \parallel Z_{lNP@Z_P} \quad (29)$$

The decoupling capacitance can be inserted on each junction node N as C_{DEN}. Therefore, Equation 29 will change to Equation 30:

$$Z_N = Z_{ini} \parallel Z_{inj} \parallel \ldots Z_{ink} \ldots \parallel Z_{lNM@Z_M} \parallel Z_{lNO@Z_O} \parallel \ldots \parallel Z_{lNP@Z_P} \parallel \frac{1}{sC_{DEN}} \quad (30)$$

The position of junction node (X_{bN}, Y_{bN}) is important for decoupling capacitance placement.

- Z_{HEAD} : The impedance seen from the VDD pin of connected block into the distribution network. Node HEAD is the top node which all transmission lines end there. Each PDN has M+1 HEAD nodes, including M consumer block and one VRM node.

For the PDN shown in Fig. 7, we can write,

$$Z_D = Z_{in1} \parallel Z_{lDC@Z_C} \quad (31)$$

$$Z_C = Z_{in5} \parallel Z_{ICB@Z_B} \quad (32)$$
$$Z_B = Z_{in4} \parallel Z_{IBA@Z_A} \quad (33)$$
$$Z_A = Z_{in3} \parallel Z_{in2} \quad (34).$$

The transmission line effects on the current distribution can be modeled as follows. Having the i_{DD} of each device and impedance of each node, the voltage of each node and current of each transmission line can be derived, [31]. For a transmission line shown in Fig. 8-A, the ABCD matrix can be written for the voltage and current of input/output as Equation 35, [34]

$$\begin{bmatrix} v_i \\ i_i \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} v_o \\ i_o \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z_0 \sinh(\gamma l) \\ \frac{1}{Z_0}\sinh(\gamma l) & \cosh(\gamma l) \end{bmatrix} \begin{bmatrix} v_o \\ i_o \end{bmatrix} \quad (35)$$

where v_i, i_i, v_o, and i_o are input/output voltage/current, respectively. Also, γ, Z_0, and l are transmission line propagation constant, characteristic impedance, and physical length, respectively.

For a plain (no junction) transmission line connected to the load k^{th}, as shown in Fig. 8-B,

$$\begin{bmatrix} v_{ik} \\ i_{ik} \end{bmatrix} = \begin{bmatrix} \cosh(\gamma_k l_k) & Z_{0k} \sinh(\gamma_k l_k) \\ \frac{1}{Z_{0k}}\sinh(\gamma_k l_k) & \cosh(\gamma_k l_k) \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{Lk}} & 1 \end{bmatrix} \begin{bmatrix} v_{DDk} \\ i_{DDk} \end{bmatrix} \quad (36).$$

For k^{th} active devices, considering the package parasitic ($R_{PKGk}L_{PKGk}C_{PKGk}$) and the decoupling capacitances C_{DEk}, as shown in Fig. 9, we write,

$$Z_{Lk} = (Z_{DDk} + R_{PKGk} + sL_{PKGk}) \parallel \frac{1}{sC_{DEk}} \parallel \frac{1}{sC_{PKGk}} \quad (37).$$

Now, for a transmission line connected to the block k^{th}, we have,

$$v_{ik} = (\cosh(\gamma_k l_k) + \frac{Z_{0k}\sinh(\gamma_k l_k)}{(Z_{DDk} + R_{PKGk} + sL_{PKGk}) \parallel \frac{1}{sC_{DEk}} \parallel \frac{1}{sC_{PKGk}}}) v_{DDk} + Z_{0k}\sinh(\gamma_k l_k) i_{DDk} \quad (38)$$

$$i_{ik} = (\frac{1}{Z_{0k}}\sinh(\gamma_k l_k) + \frac{\cosh(\gamma_k l_k)}{(Z_{DDk} + R_{PKGk} + sL_{PKGk}) \parallel \frac{1}{sC_{DEk}} \parallel \frac{1}{sC_{PKGk}}}) v_{DDk} + \cosh(\gamma_k l_k) i_{DDk} \quad (39).$$

Special case I:

For a plain (no junction) transmission line connected to the block k^{th}

$$\begin{bmatrix} v_{VRM} \\ i_{VRM} \end{bmatrix} = \begin{bmatrix} 1 & Z_{VRM} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cosh(\gamma l) & Z_0 \sinh(\gamma l) \\ \frac{1}{Z_0}\sinh(\gamma l) & \cosh(\gamma l) \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{Lk}} & 1 \end{bmatrix} \begin{bmatrix} v_{DDk} \\ i_{DDk} \end{bmatrix} \quad (40).$$

Special case II:

For a series of N plain (no junction) transmission lines connected to the block k^{th}

$$\begin{bmatrix} v_{VRM} \\ i_{VRM} \end{bmatrix} = \begin{bmatrix} 1 & Z_{VRM} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cosh(\gamma_1 l_1) & Z_{01} \sinh(\gamma_1 l_1) \\ \frac{1}{Z_{01}}\sinh(\gamma_1 l_1) & \cosh(\gamma_1 l_1) \end{bmatrix} \cdots \begin{bmatrix} \cosh(\gamma_N l_N) & Z_{0N} \sinh(\gamma_N l_N) \\ \frac{1}{Z_{0N}}\sinh(\gamma_N l_N) & \cosh(\gamma_N l_N) \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{Lk}} & 1 \end{bmatrix} \begin{bmatrix} v_{DDk} \\ i_{DDk} \end{bmatrix} \quad (41).$$

Package parasitic for each device VDD pin can be considered in PDN, as a load impedance in HEAD node. Table II shows some package parasitic for common IC packagings.

3.2 Modifier

An ideal voltage source is capable of delivering any demanded current while it has a constant voltage. In practice, due to non-ideality of input power source and the PDN parasitic, it is impossible to provide the high frequency current components for consumers. Because of increase in PDN impedance in high frequency, it acts like a low-pass filter and blocks the current component. In general case, decoupling capacitance C_{DE} as close as possible to the power consumer block, is a solution for alleviating this issue. Also, decoupling capacitance can be distributed in PDN, especially in junction nodes. This capacitor decreases the impedance of PDN impedance and provides the demanded current in high frequency. Another functionality of decoupling capacitor can be the filtering the unwanted currents produced with differnet blocks and restrics its distribution and propagation in entire board. In DC point of view, the decoupling capacitance can be placed where a node voltage violates a predefined value. This value depends on the sensitivity of connected consumer block. It can be a predefined X percent of the power supply v_{DD}. In other word, if a node violates this criterion, i.e. $|v_{DDN} - v_{DD}| > X.v_{DD}$, therefore the node N needs a decoupling capacitance C_{DEN}.

3.3 Generator

In an electronic system, for supplying a required power for different building blocks, a regulated voltage with appropriated current should be provided. In every system, different blocks may need a specific voltage level, i.e. 1V, 3.3V, 5V, 12V, and etc. Therefore, system needs to have a block which produces different levels. This duty is on a voltage regulated module (VRM) which changes the system input constant voltage to different voltage levels with appropriate power capability. This module can increase or decrease the level of an input constant voltage. In this work switching regulators are chosen because they have switching frequency components in their output spectrum content. This frequency component can propagate through the PDN and reach to the circuit devices and degrades and/or violates their operations.

The general concept in these VRM is to make the input constant voltage ON and OFF with a specific switching frequency f_s. The $V_{VRM\text{avg}}$ and ΔV_{VRM} are the output DC voltage level and its ripple in a period, respectively and summarized in Table III. Also, $f_s = 1/T$ is the frequency of VRM transistor switching and k is the duty cycle of VRM transistor in a period T, as shown in Fig. 10. Parameter k may vary from 0% to 100%. Some of the main switching VRMs include Boost, Cuk, Buck, and Buck-Boost, as shown in Fig. 11, [35]. A conceptual model for VRM model is depicted in Fig. 11-E. The output voltage of VRM can be divided in two parts, AC (ripple) and DC, and be written as Equation 42

$$v_{VRM|@I_{VRM}=cte} \cong V_{VRMavg} + \Delta V_{VRM} \sum_{k} triangle(t - kT) \qquad (42)$$

where $\text{triangle}(f_s t)$ is the base function for the ripple of VRM output voltage.

Up to here, all necessary information for extraction of PDM is obtained. In the following sub-section, the extraction process of PDM is explained in a simple algorithm and summary.

3.4 Algorithm for Extraction of PDM

Following steps should be passed for extraction of PDM:

1. Determine blocks and their position (X_i, Y_i):
   a. Estimate i_{DD} for each block ($i = 1$ to M).
   b. Extract device package parasitic.
2. Using the board/die physical parameters, $(\varepsilon_r, \mu_r, \tan\delta, and \text{ thickness})$:
   a. Extract the characteristic impedance and propagation constant of each layout traces.
   b. Determine and enumerate plane and complex transmission line and their physical length.
3. Extract Z_{ink} for each block considering its load impedance and plain transmission line parameters.
4. Extract $Z_{l\text{MN}@Z_\text{N}}$ for each nodes:
   a. Extract $Z_{l\text{MN}@Z_\text{N}}$ for each nodes considering its load impedance Z_N and its transmission line parameters.
   b. Extract Z_N for each nodes considering all the connected plain and complex transmission lines.
5. Extract Z_VRM for HEAD node of the given PDN tree.
6. Extract v_{ik} and i_{ik} for each node and branch in position (X_i, Y_i) by using Equation 38 and Equation 39.

Conducting proposed algorithm for a system PCB, results the PDM and gives valuable information about the quality of PDN.

4. Block Current Supply Cross-Correlation and Ground Plane Pollution

Clean supply is a vital necessity for proper operation of every building block in an electronic system. The own power supply fluctuation in switching regulators is a major source of power deficiency. In addition, simultaneous operation of different blocks in a system, worsen the condition. The following of this section is dedicated to analytic estimation of these phenomena.

4.1 Current Supply Cross-Correlation

The supply voltage v_{DDk} delivered to the block *k* can be estimated from Equation 43

$$v_{DDk} = Z_{HEADk} i_{DDk} + \sum_{\substack{j=1 \\ j\neq k}}^{M} Z_{jk} i_{DDj} + T_{VRMk} v_{VRM} \qquad (43)$$

where i_{DDk} and i_{DDj} are the currents of block *k* and *j*, respectively. Also, $Z_{\mathrm{HEAD}k}$ is the impedance of HEAD node of block *k* and Z_{jk} is the impedance transfer function from HEAD node *j* to HEAD node *k*. Also, T_{VRMk} is the voltage transfer function from VRM to HEAD node *k*.

In a matrix representation, we define Z_{PDN} as,

$$Z_{PDN} = \begin{bmatrix} Z_{HEAD1} & Z_{12} & \dots & Z_{1M} & Z_{1M+1} \\ Z_{21} & Z_{HEAD2} & \dots & & Z_{2M+1} \\ \dots & & \dots & & \dots \\ Z_{M1} & & \dots & Z_{HEADM} & Z_{MM+1} \\ Z_{M+11} & Z_{M+12} & \dots & Z_{M+1M} & Z_{HEADM+1} \end{bmatrix} \qquad (44)$$

where diagonal elements of Z_{PDN} are $Z_{\mathrm{HEAD}k}$ (the impedance of HEAD node of block *k*) and off-diagonal elements are Z_{jk} (the impedance transfer function from HEAD node *j* to HEAD node *k*). Also, $Z_{\mathrm{HEADM+1}}$ is the impedance of the node VRM. For a given distribution network, this matrix can be extracted using a conventional field-solver CAD tool.

The voltage transfer function form the VRM output fluctuation to the desired block *k*, T_{VRMk} can be estimated from Equation 45

$$T_{VRMk} = \frac{v_{DDk}}{v_{VRM}} = \frac{Z_{LK}}{B + AZ_{LK}} \qquad (45)$$

where *A* and *B* are the corresponding elements of ABCD matrix from Equation 35. For a given PDN and its tree structure, the ABCD matrix should be estimated from Equation 40 or Equation 41 (or the procedure explained in Section 3.4) and be used in Equation 45 for transfer function extraction.

Having T_{VRMk} and v_{VRM} for VRM and Z_{PDN} and i_{DDk} and for each building block and Equation 43, one can find the cross-correlation of consuming supply.

4.2 Ground Plane Pollution

In a worst-case condition, the simultaneous injection of building block supply current in ground plane will change its voltage and violate the zero voltage assumption. This will degrade the operation of the entire system. For a simple analysis of grounding quality, we propose that this insertion will change the ground plane electric potential as

$$v_{GND}(X,Y) = \sum_{k=1}^{M} i_{DDk} Z_{GNDk} \qquad (46)$$

where *M* is the total number of system blocks and i_{DDk} is their corresponding supply current signal. Also, Z_{GNDk} is the impedance in location of block *k*, (X_k, Y_k), from GND pin seen into the ground plane respected to the VRM position. In Equation 46, only the effect of supply return current is considered and other return path currents like ordinary signal trace injection to the ground plane is ignored.

In Equation 46 it is assumed that the circuit reference voltage (zero electric potential) is in location of the VRM and all other electric potential is compared to this point potential. The VRM location is the origin of the Cartesian coordinate tied to the PCB, as shown in Fig. 12. Therefore, $(X_{VRM}, Y_{VRM}) = (0,0)$. The return current will path in least impedance route. Each block inserts

its supply current to the ground plane and changes its electric potential. The ground plane impedance (resistance) seen from the block k^{th} respected to the origin, Z_{GNDk} (in DC condition) can be estimated from Equation 47

$$Z_{GNDk}(X,Y) = Z_{p0}D_k = Z_{p0}\sqrt{X_k^2 + Y_k^2} \quad (47).$$

In Equation 47, (X_k, Y_k) is the location of block k and Z_{p0} is the ground plane impedance. For a simple estimation, it can be considered as ohmic resistance of the ground plane, as

$$Z_{p0} = \frac{\rho}{W \times Th} \quad (48).$$

In Equation 48, ρ is the resistivity of the ground plane conductor, and W and Th are the plane width and thickness, respectively.

5. VERIFICATION AND DISCUSSION

For a better insight about stochastic signals and their PSD, for two PAM and RTW signals and a CMOS buffer gate in 90nm technology node with parameters in Table IV, $P_i(f)$, $P_v(f)$, the PSD of $V_{in}(f)$ and the PSD of $i_{DD}(f)$ for both PAM and RTW signals are derived based on Equation 26, Equation 24, Equation 23, Equation 25, and Equation 21, respectively, and shown in Fig. 13. Also for an analog stochastic process as input signal of a general single stage amplifier with parameters in Table V, $G_i(f)$ and the PSD of $i_{DD}(f)$ are derived based on Equation 6 and Equation 16, and shown in Fig. 14.

A test board is designed and fabricated to verify the presented analytic model for the PDM. The board includes two ring oscillators, a digital buffer, a Colpitz oscillator, and a single transistor amplifier, as summarized in Table VI. The fabricated test board is shown in Fig. 15. The FR4 PCB dielectric thickness in 1.6mm and trace copper thickness is 35µm. The impedance seen from each node in the PDN layout is depicted in Fig. 16. For extraction of scattering parameters between different blocks, the test board is designed and simulated in CST Studio Suite, as shown in Fig. 17. The magnitude of diagonal element of Z_{PDN} is extracted using in this CAD tool and shown in Fig. 18. Also, distribution network individual constituting trace characteristic impedance Z_{0k} are extracted and shown in Fig. 19. Each trace length and width is brought in Table VII. The voltage of different nodes in time domain are depicted in Fig. 20.

The voltage fluctuation due to simultaneous operation of digital and analog sections on different PDN nodes is shown in Fig. 20, as predicted analytically. The triangle wave shape of the PDN signal is due to charge/discharge of the VRM inductance and capacitance. The noisy wave shape modulated on this triangle is the result of two ring oscillators and single stage amplifier. The amplitude of triangle signal is about 9mV in 50kHz. The noise shape signal has a spectrum in 1MHz to 61.8MHz, mainly due to two ring oscillators in 8.3MHz and 19.4MHz. This signal has different amplitude in PDN tree structure nodes. As shown in Fig. 20, the node v_{DD4} tolerates a much more noisy Vdd signal in comparison with the node D; This is because of its vicinity to the Block 4, i.e. the ring oscillator. The reliability of power delivered to each block relies on the PDN and also other operating sections.

6. CONCLUSION

A mathematical method was proposed for analytic extraction of power distribution map of a system PCB layout. This is conducted in three steps, including derivation of supply current of building blocks with stochastic input signaling, power distribution network tracing and interconnection modeling, and switching voltage regulator module modeling. The worst-case simultaneous operation of all consumers were considered for PDM extraction. The approach was applied to a specific designed and fabricated mixed signal board. The effect of cross-correlation between different block supply loading is considered with PDN impedance matrix. Also, a simple model was proposed for evaluation of ground plane pollution, generated by sinking the building block supply currents. The PDM helps to have a basic and analytic consideration about the quality of PCB power integrity and delivery. The model is appropriate in the first stage of product design for a fast EMC standard validation. An important achievement of the model was its fast estimation of power distribution map for a given PCB layout, rather time/cost consuming experimental measurements and software simulations. Also, in many cases, it is impossible to simulate all digital, analog, and power distribution network traces, simultaneously, because of unknown and random signaling and layout trace excitation. Therefore, a rough and fast estimation is a guiding and effective choice to predict upcoming EMC/EMI standard violations and concerns.

REFERENCES

[1] Song, J., Jung, D. H., Shin, J., et al. "Novel target-impedance extraction method-based optimal PDN design for high-performance SSD using deep reinforcement learning", *IEEE Trans. Signal and Power Integrity*, **2**, pp. 1-12 (2023).

[2] Zhang, L., Juang, J., Kiguradze, Z., et al. "Efficient DC and AC impedance calculation for arbitrary-shape and multilayer PDN using boundary integration", *IEEE Trans. Signal and Power Integrity*, **1**, pp. 1-11 (2022).

[3] Wada, S., Hayashi, Y., Fujimoto, D., et al. "Measurement and analysis of electromagnetic information leakage from printed circuit board power delivery network of cryptographic devices", *IEEE Trans. Electromagn. Compat.*, **63**(5), pp. 1322-1332 (2021).

[4] Suenaga, H., Tsukioka, A., Jike, K., et al. "Compact simulation of chip-to-chip active noise coupling on a system PCB board", *IEEE Letters Electromagn. Compat. Practice and Applications*, **2**(1), pp. 15-20 (2020).

[5] Zhou, P., Pei, X., Chen, Q., et al. "EMI behavioral model based CM noise prediction method for DC power system considering multi-noise coupling", *IEEE Trans. on Power Electronics*, **38**(4), pp. 4658-4667 (2023).

[6] Li, N. and Miao, M. "Design of EMI and suppression structure based on bar-via," *Microelectronics Journal*, **112**, pp. 1-9 (2021).

[7] Yousaf, J., Nah, W., Majali, E. R. A., et al. "Rapid characterization of efficient system level ESD protection strategy using coupling transfer function", *Microelectronics Journal*, **110**, pp. 1-13 (2021).

[8] Zhu, Z., Zhao, Y., Yan, W., et al. "Modeling of line impedance stabilization network impedance characteristic based on genetic algorithm", *Microelectronics Journal*, **113**, pp. 1-8 (2021).

[9] Kerrouche, B., Bensetti, M., and Zaoui, A. "EMI modeling considering the impedance behavior of isolated off-line converter", *Microelectronics Reliability*, **105**, pp. 1-9 (2020).

[10] Benfca, J., Vargas, F., Soares, M. F., et al. "Conducted EMI susceptibility analysis of a COTS processor as function of aging", *Microelectronics Reliability*, **114**, pp.1-7 (2020).

[11] Kraiem, S., Hamouda, M., and Slama, J. B. H. "Conducted EMI mitigation in transformer-less PV inverters based on intrinsic MOSFET parameters", *Microelectronics Reliability*, **114**, pp. 8-14 (2020).

[12] Sun, J., Wang, H., Wu, K., et al. "A pattern-based analytical method for impedance calculation of the power distribution network in mobile platforms", *IEEE Trans. Electromagn. Compat.*, **63**(3), pp. 912-921 (2021).

[13] Yang, S., Cao, Y. S., Ma, H, et al. "PCB PDN pre-layout library for top-Layer inductance and the equivalent model for decoupling capacitors", *IEEE Trans. Electromagn. Compat.*, **60**(6), pp. 1898-1906 (2018).

[14] Cao, Y. S., Makharashvili, T., Cho, J., et al. "Inductance extraction for PCB pre-layout power integrity using PMSR method", *IEEE Trans. Electromagn. Compat.*, **59**(4), pp. 1339-1346 (2017).

[15] Paulis, F. D., Zhang, T., and Fan, J. "Signal/power integrity analysis for multilayer printed circuit boards using cascaded S-parameters", *IEEE Trans. Electromagn. Compat.*, **52**(4), pp. 1008-1018 (2010).

[16] Archambeault, B., Brench, C., and Connor, S. "Review of printed-circuit-board level EMI-EMC issues and tools", *IEEE Trans. Electromagn. Compat.*, **52**(2), pp. 455 – 461 (2010).

[17] Mehri, M. and Masoumi, N. "Statistical prediction and quantification of radiated susceptibility for electronic systems PCB in electromagnetic polluted environments", *IEEE Trans. Electromagn. Compat.*, **59**(2), pp. 498-508 (2017).

[18] Hoyos, S., Garcia, J. A., and Arce, .G R. "Mixed-signal equalization architectures for printed circuit board channels", *IEEE Trans. on Circuits and Syst. I: Reg. Papers*, **51**(2), pp. 264-274 (2004).

[19] Rabaey, J. M., Chandrakasan, A., and Nikolic, B., in *Digital Integrated Circuits, A Design Perspective*, 2nd Edn., Pearson Education, (2003).

[20] Mehri, M., Kouhani, M. H. M., Masoumi, N., et al. "New approach to VLSI buffer modeling, considering overshooting effect", *IEEE Trans. Very Large Scale Integr. Syst.*, **21**(8), pp. 1568-1572 (2013).

[21] Bisdounis, L. and Koufopavlou, O. "Short-circuit energy dissipation modeling for sub-micrometer CMOS gates", *IEEE Trans. on Circuits and Syst. - Part I: Fundamental Theory & Applications*, **47**(9), pp. 1350-1361 (2000).

[22] Rossello, J. L. and Segura, J. "Charge-based analytical model for the evaluation of power consumption in submicron CMOS buffers", *IEEE Trans. Computer-Aided Design of Integr. Circuits and Syst.*, **21**(4), pp. 433-448 (2002).

[23] Bowman, K. A., Austin, B. L., Eble, J. C., et al. "A physical alpha power law MOSFET model", *IEEE Journal of Solid-State Circuits*, **34**(10), pp. 1410-1414 (1999).

[24] Turgis, S. and Auvergne, D. "A novel macro-model for power estimation in CMOS structures", *IEEE Trans. Computer-Aided Design of Integr. Circuits and Syst.*, **17**(11), pp. 1090-1098 (1998).

[25] Wang, J., Lu, J., Chu, X., et al. "Modeling and simulation of planes with decoupling capacitors", *IEEE Trans. on Components, Packaging and Manufacturing Technology*, **6**(7), pp. 1087-1098 (2016).

[26] Park, H., Park, J., Kim, S., et al. "Deep reinforcement learning-based optimal decoupling capacitor design method for silicon interposer-based 2.5-D/3-D ICs", *IEEE Trans. on Components, Packaging and Manufacturing Technology*, **9**(9), pp. 1835-1846 (2019).

[27] Tripathi, J. N., Sharma, V. K., and Shrimali, H. "A review on power supply induced jitter", *IEEE Trans. on Components, Packaging and Manufacturing Technology*, **9**(9), pp. 511-524 (2019).

[28] Zhang, M., Li, Y., and Li, L. "Analyze and design high-speed power delivery networks using new multi-input impedances in printed circuit boards", *IEEE Trans. Microw. Theory and Techn.*, **57**(7), pp. 1818-1831 (2009).

[29] Zhang, M., and Mao, J. "A new systematic method for the modeling, analysis, and design of high-speed power-delivery networks by using distributed port", *IEEE Trans. Microw. Theory and Techn.*, **58**(11), pp. 2940-2951 (2010).

[30] Mehri, M., "Stochastic estimation of total radiated power from PCB signal/PDN layout using EMI radiation resistance", *Microelectronics Journal*, **116**, pp. 1-10 (2021).

[31] Mehri, M., "A circuit level analysis of power distribution network on a PCB layout exposed to intentional/unintentional electromagnetic threats", *Integration*, **89**, pp. 25-36 (2023).

[32] Heidari, S., Mehri, M., and Masoumi, N. "Statistical prediction of planar power consumption distribution in digital system layout/PCB", *The 21th IEEE Workshop on Signal and Power Integrity, (SPI2017)*, Italy, May 2017.

[33] Carlson, A. B., Crilly, P. B., and Rutledge, J. C., in *Communication systems: an introduction to signals in electrical communication*, 4th Edn., McGraw-Hill, (2002).
[34] Chen, G., and Friedman, E. G. "An RLC interconnect model based on Fourier analysis", *IEEE Trans. on Computer-Aided Design of Integr. Circuits and Syst.*, **24**(2), pp. 170-183 (2005).
[35] Rashid, M. H., in *Power Electronics: Circuits, Devices & Applications*, 4th Edn., Pearson, (2013).

LIST OF CAPTIONS

FIGURES

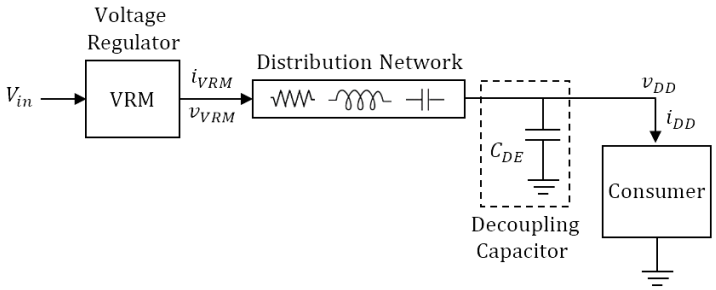
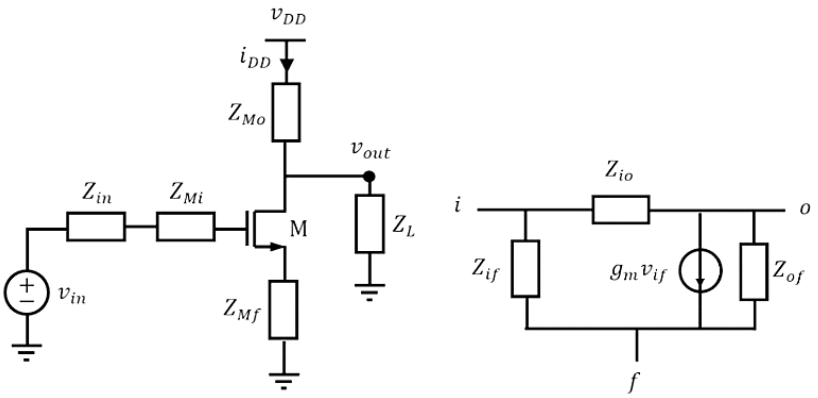
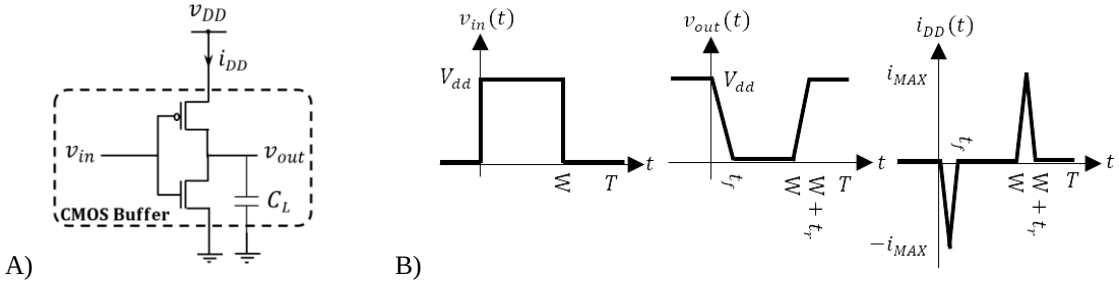


Fig. 1. Power distribution network.



A) B)

Fig. 2. A) Simple model of single stage amplifier B) General small signal model for a transistor.



A) B)

Fig. 3. A) CMOS buffer gate, B) waveform of v_{in}, v_{out}, and i_{dd} in a CMOS buffer.

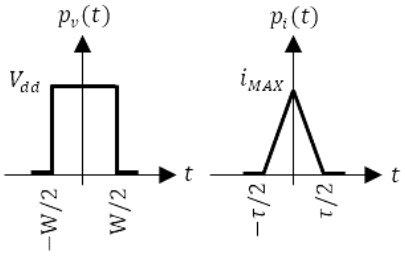


Fig. 4. Base functions for input voltage and supply current signals.

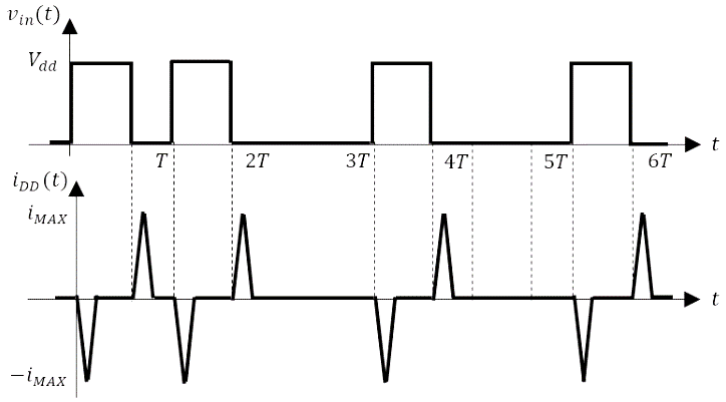


Fig. 5. The PAM signal as input voltage and resultant i_{DD}, [30].

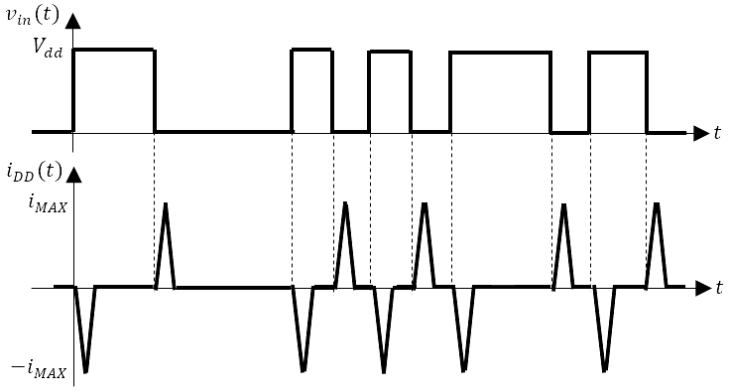


Fig. 6. The RTW signal as input voltage and resultant i_{DD}, [30].

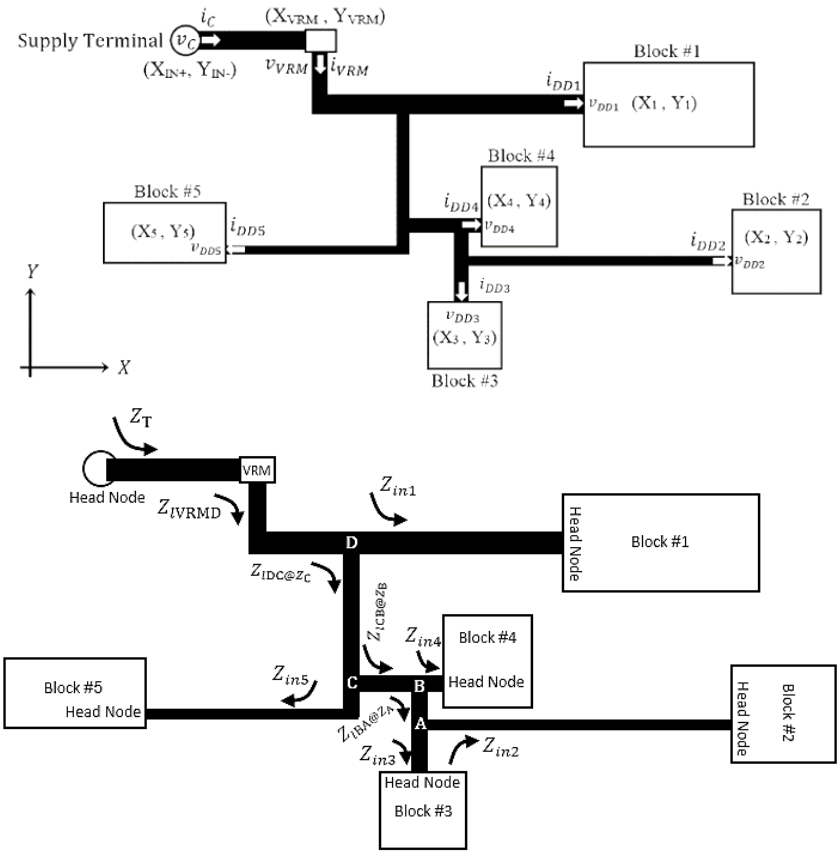


Fig. 7. An example of PDN. Node HEAD is the top node which all transmission lines end there. Each PDN has M+1 HEAD nodes, including M consumer block and one VRM node.

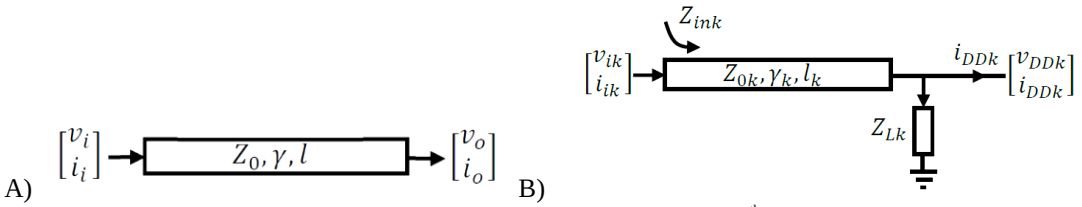


Fig. 8. Transmission line connected to the block k^{th}.

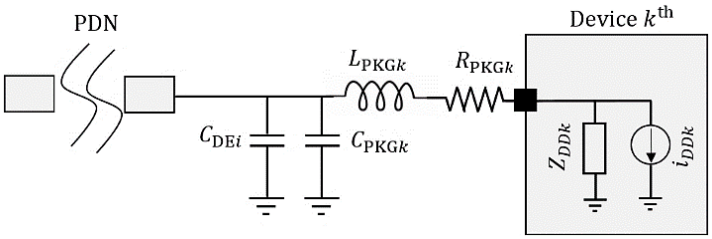


Fig. 9. k^{th} component package parasitic and decoupling capacitance.

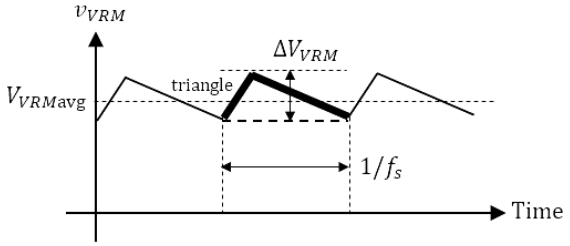
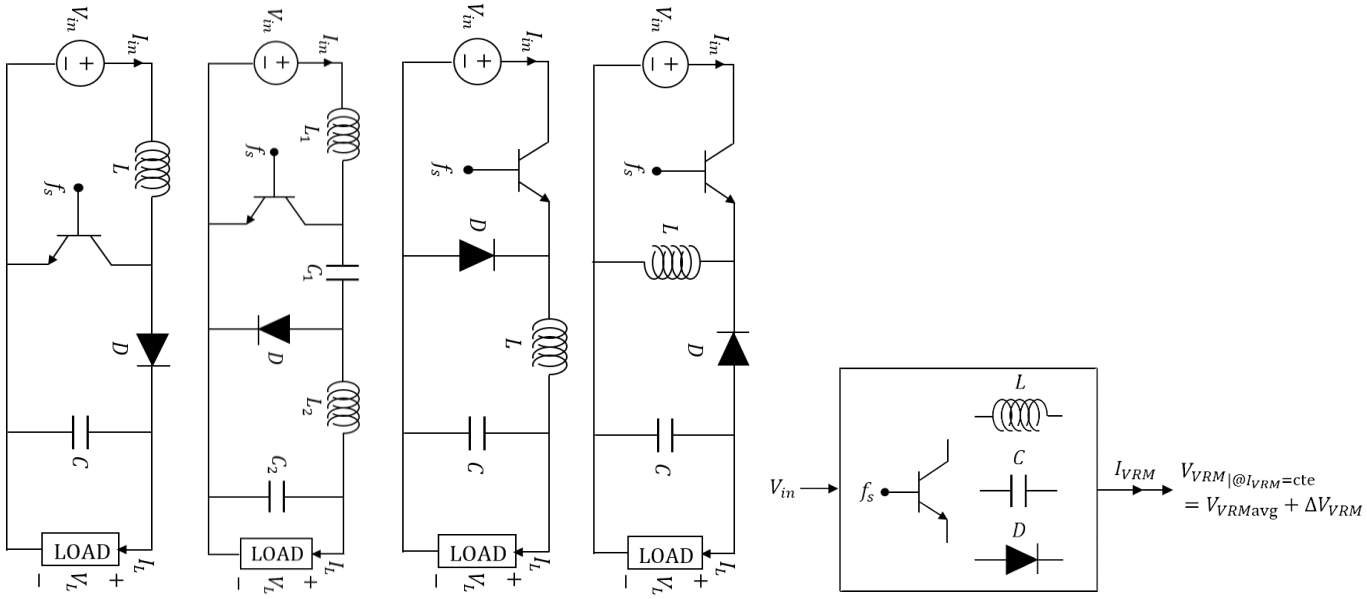


Fig. 10. Output voltage of a general switching voltage regulator modules.



A) B) C) D) E)

Fig. 11. Switching voltage regulator modules, [35], A) Boost, B) Cuk, C) Buck, D) Buck-Boost, and E) conceptual model of VRMs.

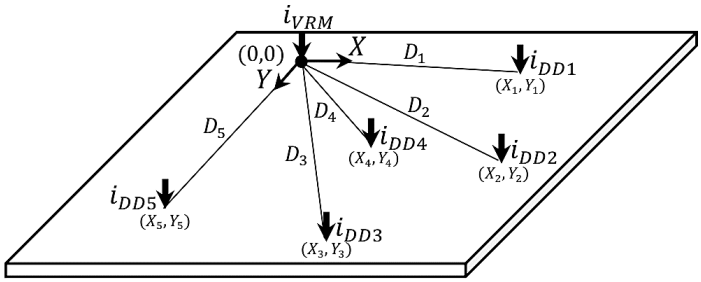


Fig. 12. The injection of different blocks current to the ground plane.

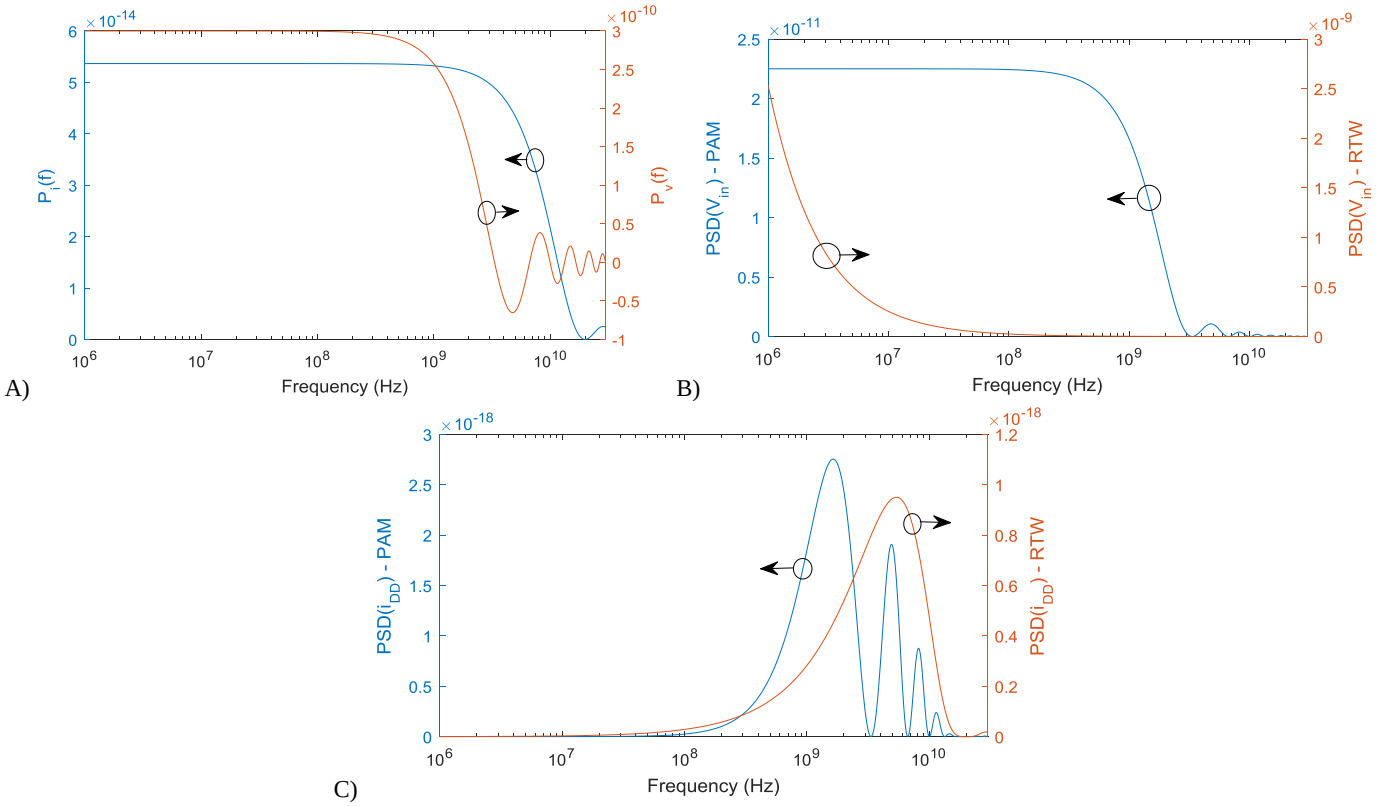


Fig. 13. Signals for CMOS buffer in 90nm technology: A) $P_i(f)$, $P_v(f)$ B) The PSD of $V_{in}(f)$ for PAM and RTW signals, and C) The PSD of $i_{DD}(f)$ for PAM and RTW.

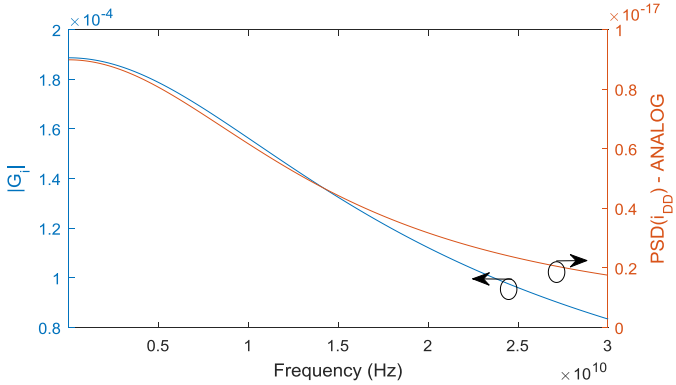


Fig. 14. General single stage amplifier $G_i(f)$ and the PSD of $i_{DD}(f)$ for analog stochastic process with normal amplitude distribution.

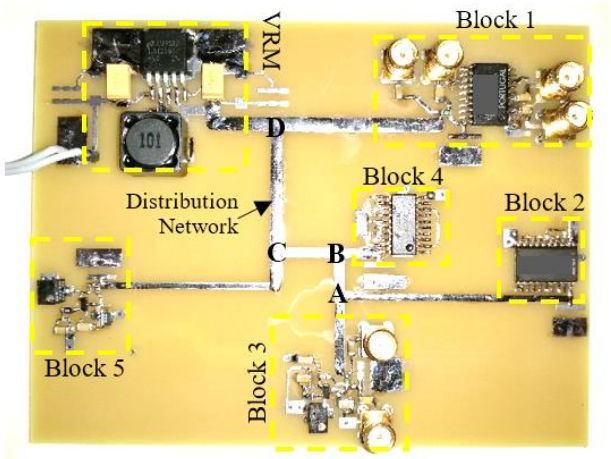


Fig. 15. Fabricated test board for verification.

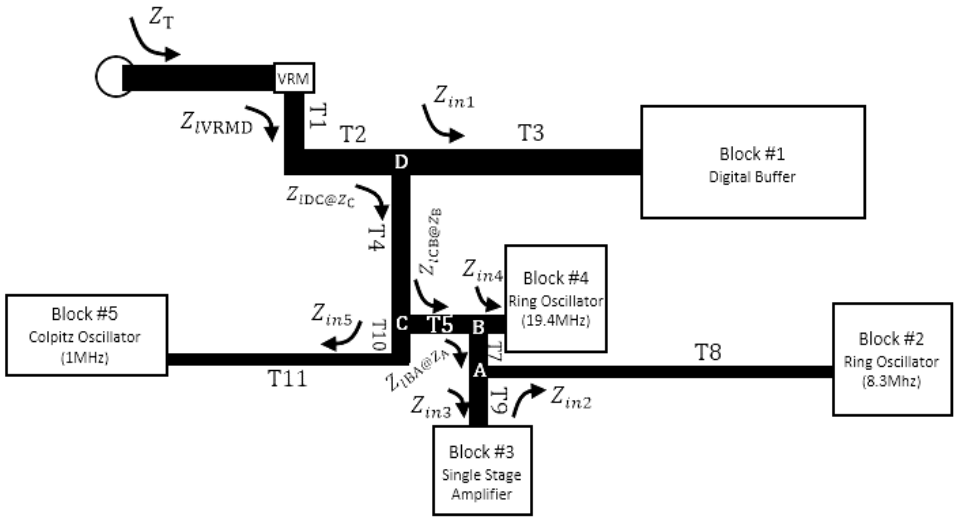


Fig. 16. The PDN layout of the fabricated test board.

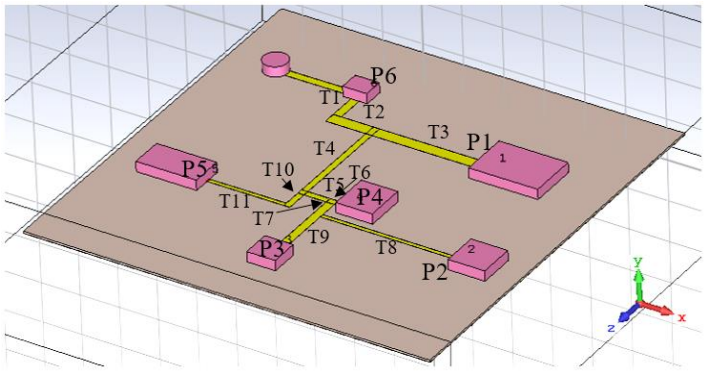


Fig. 17. Test board in CST Studio Suite.

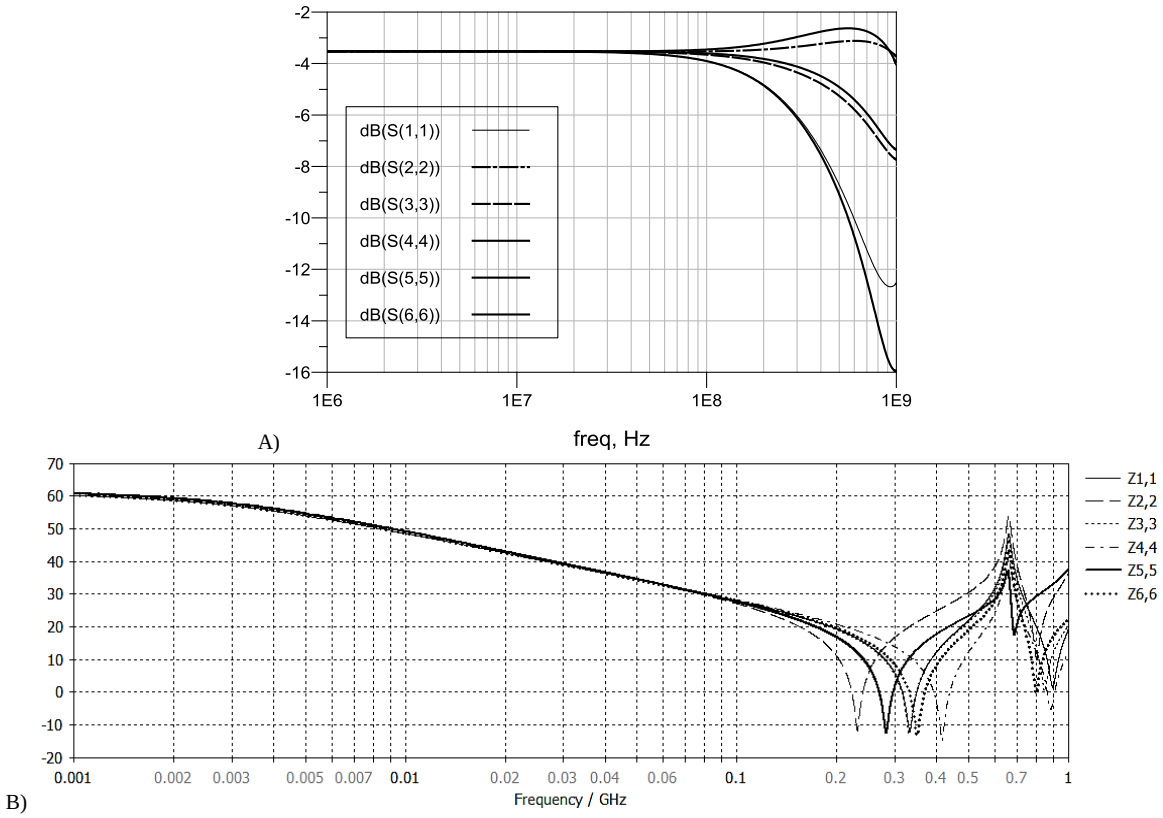


Fig. 18. The magnitude of A) S_{kk} and B) $Z_{\mathrm{HEAD}k}$ for the test board PDN

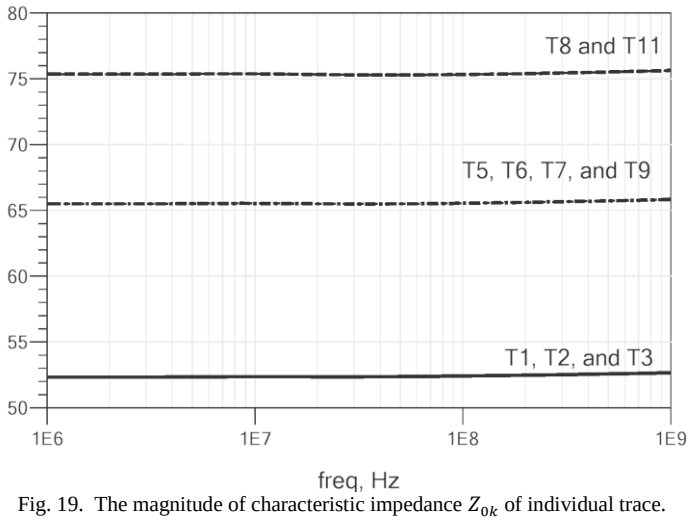


Fig. 19. The magnitude of characteristic impedance Z_{0k} of individual trace.

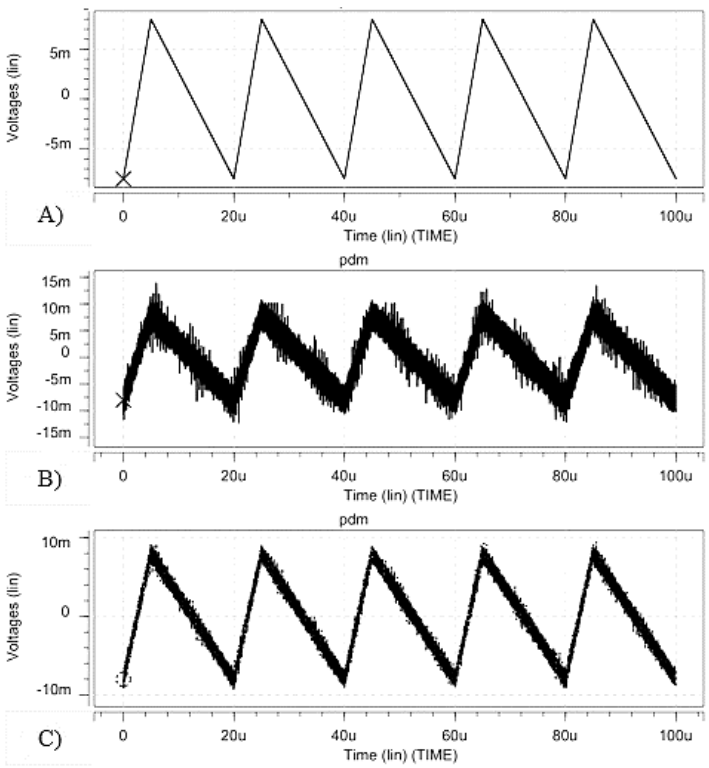


Fig. 20. The voltage of different nodes in time domain A) v_{VRM} B) v_{DD4} C) v_D.

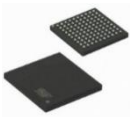
TABLES

TABLE I PARAMETERS FOR MOS AND BJT TRANSISTOR

Parameter	MOS	BJT
Z_{if}	$\frac{1}{sC_{GS}}$	$r_\pi \parallel \frac{1}{sC_\pi}$
Z_{io}	$\frac{1}{sC_{GD}}$	$r_\mu \parallel \frac{1}{sC_\mu}$
Z_{of}	r_o	r_o

[1] C_{GS}, C_{GD}, and r_o are gate-source capacitance, gate-drain capacitance, and drain-source resistance, respectively.
[2] C_π, C_μ, r_π, r_μ, and r_o are base-emitter capacitance, base-collector capacitance, base-emitter resistance, base-collector resistance, and collector-emitter resistance, respectively.

TABLE II PACKAGE PARASITIC FOR COMMON IC PACKAGING

Package Name	Package Picture	Number of Pins	C_{PCK} (pF)	R_{PCK} (Ohm)	L_{PCK} (nH)
Thin Quad Flat Package (TQFP)		100	0.46	0.94	4.91
		144	0.60	0.16	8.24
Ball Grid Array (BGA)		256	1.2	0.27	6.5
		956	0.80	0.30	2.89
Quad Flat No-Lead (QFN)		32	0.2	-	1

Wafer-Level Package (WLP)		196	0.04	0.01	0.14

TABLE III DIFFERENT CONVENTIONAL SWITCHING VRMS PARAMETERS, [35]

Parameter	Boost	Cuk	Buck	Buck-Boost
ΔV_{VRM}	$\frac{kI_L}{Cf_s}$	$\frac{kV_{in}}{8L_2C_2f_s^2}$	$\frac{k(1-k)V_{in}}{8LCf_s^2}$	$\frac{kI_L}{Cf_s}$
V_{VRMavg}	$\frac{V_{in}}{1-k}$	$\frac{kV_{in}}{k-1}$	kV_{in}	$\frac{kV_{in}}{k-1}$

TABLE IV SIGNAL AND CMOS BUFFER PARAMETERS IN 90NM

Signal and Timing parameters	CMOS buffer parameters
$T = 1ns$	$V_{dd} = 1\text{V}$
$W = 0.3T$	$v_{TH} = 0.397\text{V}$
$\tau = 0.1T$	$k_s = 1.67\text{E} - 2$
$\mu = 0.1f$	$\lambda = 0.2738$
$i_{MAX} = 1.1m\text{A}$	$\alpha = 1.264$

TABLE V SIGNAL AND GENERAL AMPLIFIER PARAMETERS

Signal and Frequency parameters	General Amplifier parameters	
$Z_{in} = 50\Omega$	$C_L = 50f\text{F}$	$r_o = 10k\Omega$
$\sigma_X = 0.1\text{V}$	$C_{GS} = 3f\text{F}$	$r_\mu = r_\pi = \infty$
$m_X = 1\text{V}$	$C_{GD} = 1f\text{F}$	$Z_{Mi} = 0.1\Omega$
$f_{MIN} = 1k\text{Hz}$	$C_{DB} = 2f\text{F}$	$Z_{Mf} = 0.1\Omega$
$f_{MAX} = 1G\text{Hz}$	$g_m = 5m\text{S}$	$Z_{Mo} = 5k\Omega$

TABLE VI TEST BOARD BLOCKS

Block	Function
1	Digital Buffer
2	Ring Oscillator with 7 buffers (8.3MHz)
3	Single Stage Amplifier
4	Ring Oscillator with 3 buffers (19.4MHz)
5	Colpitz Oscillator (1MHz)
VRM	Switching Voltage Regulator ($f_s = 50k\text{Hz}$) (Buck)

TABLE VII THE PARAMETERS OF TEST BOARD DISTRIBUTION NETWORK TRACES

Trace Name	Trace Width (mm)	Trace Length (mm)	Trace Name	Trace Width (mm)	Trace Length (mm)
T1	3	3.1	T7	2	8.0
T2	3	13.2	T8	1.5	47.8
T3	3	34.1	T9	2	15.1
T4	2.5	27.1	T10	2.5	6.2
T5	2	13.5	T11	1.5	35.8
T6	2	7.5			

BIOGRAPHY

Milad Mehri received the B.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 2009, the M.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2011, and the Ph.D. degree from the University of Tehran, Tehran, Iran, in 2016. He joined the Department of Electrical Engineering, Faculty of Engineering, Alzahra University in 2017. His current research interests include electromagnetic compatibility/interference (EMC/EMI) analysis of electronic systems, statistical modeling of radiated susceptibility/emission of high-frequency printed circuit boards (PCBs), and VLSI interconnects and nanowires modeling.