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Research Note

Figure-of-Merit (FoM) optimization in class-C oscillators

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Abstract. In this paper, a new approach to optimize phase noise and Figure-of-Merit (FoM) in class-C oscillators is presented. This approach recruits DC voltage of the common source node of the switching pair transistors as an indicator to achieve the best performance of a class-C oscillator. The proposed indicator has the advantages of not introducing any loading effect to the output node, and independency from PVT changes. The method is simple and applicable to any oscillator with class-C topology, and with some modifications it would be applied to other oscillator topologies like class-B. The idea is verified using theoretical analysis, and circuit simulations on 0.18 μm CMOS technology at 2 GHz oscillation frequency. Moreover, a discrete prototype is fabricated at 15 MHz and measurement results are provided which further validate feasibility of this approach.

1. Introduction

Modern standards for oscillators require high spectral purity, i.e., low phase noise, along with low power consumption. Achieving these specifications together, which is equivalent to maximizing Figure-of-Merit (FoM), is still considerably challenging for oscillator designers. Cross-coupled oscillators are among the most-used topologies in high performance applications due to their good FoM performance. The most common architectures in cross-coupled oscillators are class-B and class-C. Although designing of class-C oscillators is more challenging, they can achieve higher FoM due to lower power consumption. A comparative study between these two architectures is provided in [1].

There have been several works on improving FoM through decreasing phase noise or power consumption in cross-coupled oscillators [2–5]. For instance some methods like current reuse [6], incorporating a new resonator [7], using Darlington structure [8] and making the tail current source to work in sub-threshold region [9] can be used to lower the phase noise and thus improving the FoM. Ref. [10] optimized the sizing of the transistors to maximize the FoM.

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In [11] and [12] a negative feedback loop is proposed that senses the oscillation amplitude by an amplitude detector and gradually decreases bias voltage of the core transistors to make them work in class-C mode. Ref. [13] also used this method to ensure robustness of the oscillator startup. However, this approach loads the tank, decreasing both its quality factor and tuning range of the oscillator. A better approach in [14] takes the feedback from tail node and adjusts bias voltage of core transistors such that the tail node voltage tracks an external reference voltage, without perturbing the output nodes. In [15] and [16] two feedback loops are used to simultaneously ensure the robust startup and lower the phase noise. Ref. [17] used a digitally controlled circuit for the same purpose. However, in all of the above-mentioned works the exact criterion to determine the reference voltage to attain optimum FoM is not clear.

According to Ref. [2], forcing the tail node to oscillate at exactly twice the oscillation frequency ($2f_{osc}$) will minimize the phase noise, so it uses an extra LC filter at the tail node for this purpose. Using this fact, and given that dependency of the output frequency on the tail bias current would be minimum when the tail tank resonates at exactly $2f_{osc}$, Ref. [18] has proposed a technique to automatically set the tail tank to the desired frequency. A better approach is introduced in [19], taking into account that when the tail tank is trimmed to $2f_{osc}$, its voltage reaches the maximum amplitude. Thus, a peak detector is utilized and the variable capacitor bank of the tail tank is adjusted in order to achieve the optimum point of operation. But the common drawback of all these methods is their high sensitivity to any deviation from $2f_{osc}$; based on [19], a 6% error in tail tank would deteriorate the phase noise by 4dB. Also the method in [20] is applicable only when a tank circuit is used in the tail node, therefore cannot be used in typical LC oscillators.

All of the above mentioned methods cease to preserve the optimum performance point in presence of PVT changes. In this paper we introduce a new indicator to achieve the maximum FoM of a class-C oscillator and exploit it to ensure optimum performance in spite of PVT changes. We will focus on class-C oscillator to explain this idea since it demonstrates a better performance than conventional class-B oscillators in terms of phase noise and power consumption [21].

The paper is organized as follows: in Section 2 the important relation between FoM and DC voltage of the tail node ($V_{S,DC}$) will be obtained through theoretical analysis alongside with some intuitive arguments based on fundamental features of the class-C oscillator. Circuit simulations will also be presented to support the idea. Measurement results are presented in Section 3 and future works are discussed in Section 4. Finally Section 5 concludes the paper.

2. Concept demonstration

This section presents the main concept of this paper that is the "dependency of FoM on the DC voltage of the tail node". First, FoM is defined as follows [22]:

$$FoM = 20\log\left(\frac{f_{osc}}{\Delta f}\right) - L\{\Delta f\} - 10\log\left(P_{DC,mW}\right), \quad (1)$$

where f_{osc} is the oscillation frequency, Δf is the offset frequency from f_{osc}, $P_{DC,mW}$ is total power consumption in mW and $L\{\Delta f\}$ is the phase noise at offset Δf.

For the purpose of this section, first it will be proved that by sweeping the bias current of the oscillator, $V_{S,DC}$ will have a maximum value in a particular bias point. Then in the next part we will conclude this point is the very optimum bias point which we were looking for.

2.1. Tail node voltage analysis

Consider the class-C oscillator shown in Figure 1 we denote the tail voltage by V_S, bias voltage of core transistors by V_B and single-ended output voltage amplitude by A. Two output nodes have bias voltages of V_{DD} and a differential signal with amplitude A. Therefore, we can show them in one half-period as Figure 2, assuming a cosine waveform for each of them. As it is clear, falling V_{out-} may cause M_1 to operate in triode region for a fraction of this half-period. For this reason, writing the well-known condition for working MOS transistor in triode region, $V_D < V_G - V_{th}$, with V_{th} being threshold voltage of the transistor for M_1 in this half-period gives:

$$V_{DD} - A\cos\omega t < V_B + A\cos\omega t - V_{th}. \quad (2)$$

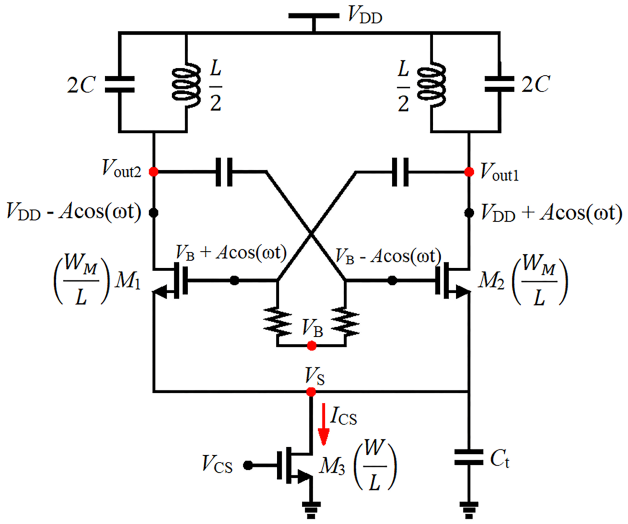

Figure 1. Class-C oscillator schematic for the following analysis.

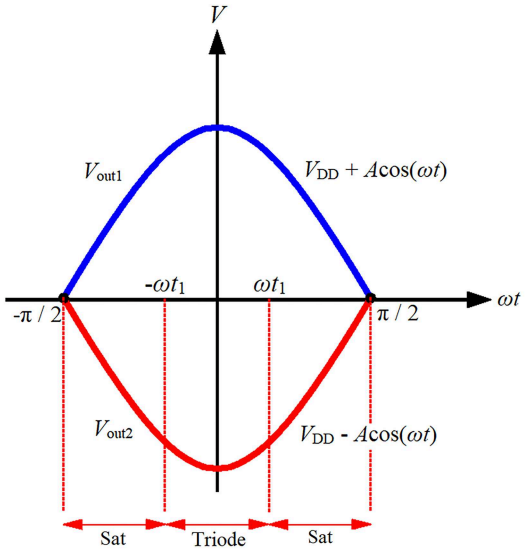

Figure 2. One half-period of output voltages of the oscillator shown in Figure 1; blue: out+, red: out-.

Assuming t_1 as the transition time of M_1 from saturation to triode we have:

$$t_1 = \frac{1}{\omega}\cos^{-1}\left(\frac{V_{DD} - V_B + V_{th}}{2A}\right). \quad (3)$$

This means in this half-period for $|t| > t_1$, M_1 is in saturation region, and for $|t| < t_1$, M_1 would operate in triode, as it is shown in Figure 2. Of course in the next half-period, M_2 will have this condition. However, if the argument of $\cos^{-1}$ function in Eq. (3) is greater than unity, the equation would be undefined. We can state this condition as:

$$A < \frac{V_{DD} - V_B + V_{th}}{2}. \quad (4)$$

So if Eq. (4) is satisfied, the both transistors will stay in saturation region for their whole conduction time of the period. This is because the oscillation amplitude is too small. Note also that according to Ref. [21], A itself is an increasing function of I_{CS} (the bias current). This means for low values of I_{CS} which Eq. (4) is valid, transistors are totally in saturation region, but higher values of I_{CS} brings transistors into triode region for a portion of each cycle. Later in this section we will derive an approximate algebraic relation between A and I_{CS} using simulation results.

KCL (Kirchhoff's Current Law) equation at the tail node of the oscillator shown in Figure 1 provides (neglecting parasitic device capacitance compared to C_t):

$$I_{D1} + I_{D2} = I_{CS} + C_t\frac{dV_S}{dt}. \quad (5)$$

If $V_B = V_{th}$, for half-period of negative voltage swing in gate of a transistor, neglecting subthreshold conduction, that transistor can be assumed off. In our case, the gate AC voltage of M_2 in this half-period is negative, which renders our assumption further reasonable. Hence Eq. (5) is simplified to:

$$I_{D1} = I_{CS} + C_t\frac{dV_S}{dt}. \quad (6)$$

Assuming $|t| > t_1$ which means M_1 is saturated, Eq. (6) turns to:

$$\frac{\beta}{2} \times \frac{(V_B + A\cos\omega t - V_S - V_{th})^2}{1 + \theta(V_B + A\cos\omega t - V_S - V_{th})} = I_{CS} + C_t\frac{dV_S}{dt}, \quad (7)$$

with $\beta = (\mu_n C_{ox} W/L)$ being μ_n electron mobility, C_{ox} oxide capacitor, W/L ratio of width to length of the transistor. In Eq. (7) θ is the mobility reduction coefficient modeling short channel effects of the transistor. This equation is a first order differential equation for variable $V_S(t, I_{CS})$ with respect to time. Next, we rewrite Eq. (6) for $|t| < t_1$, when M_1 is in triode (in the case that condition of Eq. (4) is not satisfied). So we have:

$$\frac{\beta}{2}\Big[2\,(V_B + A\cos\omega t - V_S - V_{th})\,(V_{DD} - A\cos\omega t - V_S) - (V_{DD} - A\cos\omega t - V_S)^2\Big] \Big/ \Big[1 + \theta\,(V_B + A\cos\omega t - V_S - V_{th})\Big] = I_{CS} + C_t\frac{dV_S}{dt}. \quad (8)$$

These two differential equations do not have explicit answers, so numerical methods should be exploited. For this purpose, design values defined in Table 1 and $V_B = V_{th} = 0.52$ V, $f_{osc} = 2$ GHz, $\mu C_{ox} = 357.6$ μA/V^2 and $\theta = 1$ are substituted in Eq. (7) and (8). This will provide the final piece-wise differential equation shown in Eq. (9) bellow this page. In this equation, V_S is in Volts, I_{CS} in mA and t in ns. Only in case $A < V_{DD}/2 = 0.9$ V (according to Eq. (4)), M_1 will always work in saturation region and t_1 will

Table 1. Values of class-C oscillator circuit in Figure 1.

V_{DD} (V)	V_{th} (V)	C (pF)	L (nH)	C_t (pF)
1.8	0.52	2.3	2.7	10
L (Technology) (μm)		**W_M (μm)**	**Q of inductor**	
0.18 (CMOS)		30	14	

$$\frac{dV_S}{dt} = \begin{cases} \frac{2.98(A\cos 4\pi t - V_S)^2}{1+1(A\cos 4\pi t - V_S)} - \frac{I_{CS}}{10} & |t| \geq t_1 \\ \frac{2.98[2(A\cos 4\pi t - V_S)(1.8 - A\cos 4\pi t - V_S) - (A\cos 4\pi t - V_S) - (1.8 - A\cos 4\pi t - V_S)^2]}{1+1(A\cos 4\pi t - V_S)} - \frac{I_{CS}}{10} & |t| < t_1 \end{cases} \quad (9)$$

Box I

not exist, so Eq. (9) will be defined solely by the first expression in Box I. According to Eq. (3), t_1 in Eq. (9) can be expressed as:

$$t_1 = \frac{1}{\omega}\cos^{-1}\left(\frac{V_{DD}}{2A}\right). \quad (10)$$

Eq. (9) is also dependent on variable A. So in order to have an equation describing V_S in terms of t and I_{CS}, the relation between A and I_{CS} needs to be extracted. Keeping V_{DD} and V_B constant, A would be just a function of I_{CS}. For deriving the relation between them, we can use the simple linear formula below:

$$A = R_p I_{\omega 0} = R_p I_{CS}. \quad (11)$$

In Eq. (11) R_p is the whole parasitic resistance in the tank and the fundamental current component passing through the tank equals to the bias current in a class-C oscillator [4]. However, this simple relation does not account for the voltage limited regime shown in Figure 3(a) where the oscillation amplitude saturates for high bias currents. Thus, a higher order polynomial relation that could model this behavior is required. As such model was not found in any reference, we performed a simulation on the circuit represented in Figure 1 with $V_B = V_{th} = 0.52$ V and $f_{osc} = 2$ GHz, to extract the coefficients for the third order polynomial approximation which is provided in below equation.

$$A = -0.0013I_{CS}^3 + 0.0078I_{CS}^2 + 0.2228I_{CS} - 0.032. \quad (12)$$

Now the final piece-wise two-variable differential equation can be driven by substituting Eq. (10) and (12) in Eq. (9). Numeric solvers in Matlab have been used to obtain $V_S(t)$ function for each bias current (I_{CS}) with 0.1mA current step. Finally the average of $V_S(t)$ ($V_{S,DC}$) which is achieved in this way is plotted in Figure 4. The boundary condition in Eq. (4) for $V_B = V_{th}$ can be written as $A = V_{DD}/2 = 0.9$, which according to Eq. (12) occurs at $I_{CS} = 4$ mA. At this point, core transistors start entering triode region when the oscillation amplitude reaches its peak. As it is clear from Figure 4, after this point the percentage of a period in which the core transistors work in triode region starts to increase. A key observation from the curve in Figure 4 is that at the peak point of the analytical $V_{S,DC}$, the core transistors are in triode region in 40% of their conduction period and the bias current is $I_{CS} = 5$ mA, a little more than the boundary

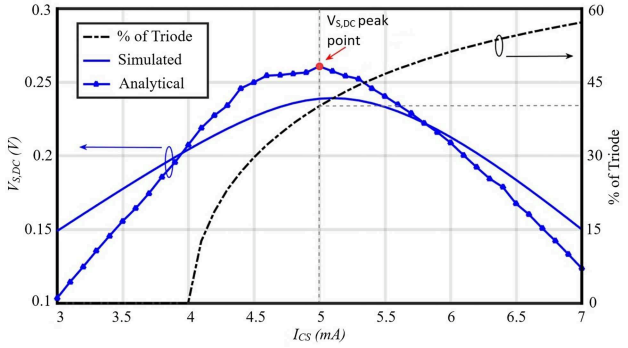

Figure 4. Analytical DC voltage of the tail node ($V_{S,DC}$) versus bias current (I_{CS}) and the simulated one with design values of Figure 1 (left axis), and the percentage of a period in which transistors are in triode region (right axis).

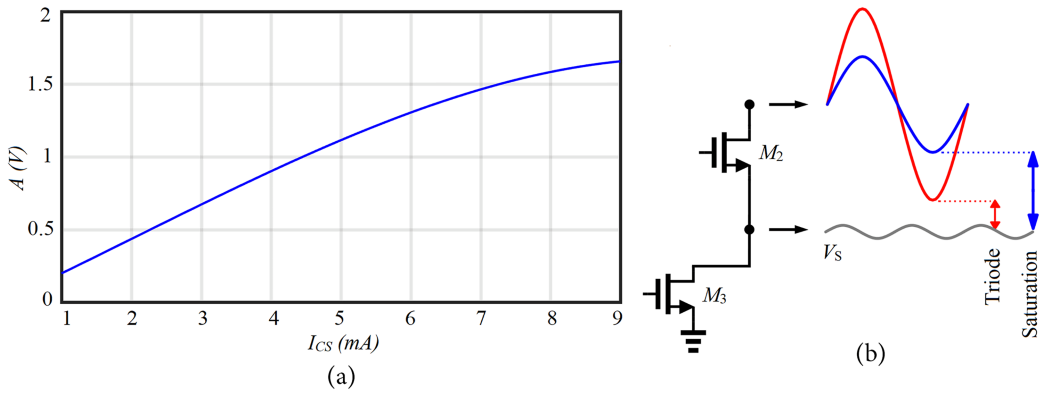

Figure 3. (a) The typical relation between oscillation amplitude (A) and bias current (I_{CS}) and (b) Illustration of entering core transistors into triode region for high values of oscillation amplitude and I_{CS}.

value of 4 mA. This significant point will be deliberated more carefully in the next section.

Simulated $V_{S,DC}$ is also plotted in Figure 4 for comparison. The key point is coincidence of peaks of these two curves with a good approximation. But there is some mismatches between their levels, which can be linked to model simplifications such as neglecting channel length modulation and effects of working in high frequencies. Nevertheless, the simulated curve trend is well approximated by the analytical one.

2.2. Finding the optimal point

By optimal point in this section we mean the maximum FoM point, and we are going to show the maximum $V_{S,DC}$ is this optimal point. Shown in Figure 3(a) as the bias current increases, the output voltage amplitude is also grows up. So there will be a point at which each core transistor enters triode region while reaching its negative peak drain voltage, as it is illustrated in Figure 3(b). For low values of bias current, core transistors are always in saturation region, and output voltage amplitude is a linear function of bias current [21]. However, for high values of bias current, each core transistor enters triode region for a fraction of its conduction period. This enforces output amplitude to saturate gradually. It also has been emphasized in [21] that the phase noise would not be impaired if core transistors only *moderately* (and *not deeply*) enter triode region. In this work we quantify *moderate* and *deep* triode as the percentage of a period in which the core transistors are in the triode region. In the peak of analytical $V_{S,DC}$ (see Section 2.1) this percentage was **40%** and the associated bias current was **5 mA**. So this has to be an approximate standard for *deep* triode region (of course for our setup and element values), as we will show in this section.

Four significant phenomena which directly affect the phase noise and FoM behavior of a class-C oscillator are mentioned below. The main common feature among all of them is starting their effect in the *boundary* of saturation and triode regimes, and completing it in *deep* triode region.

First: as it can be seen from Figure 1, there is a large capacitance in class-C oscillator from tail node to the ground, creating a low impedance path for tank circuit if core transistors become triode, which adversely effects both tank quality factor and phase noise generated by the transistors. Commonly this is referred to as "Q-degradation" effect [2].

Second: Referred to [21], by entering transistors in triode region, their conduction time (i.e., time which their current is non-zero) grows up. And since a transistor contributes noise only when it is conducting, their total noise also increases. In fact, this shows the benefit of working in class-C topology while transistors are kept in their active region; since the conduction time is very small, ideally near zero, their contribution to the phase noise is minimal, even negligible. One may justify this effect also in terms of Noise Modulation Function (NMF) in ISF theory [23]. Using this theory, [21] has shown that the effective ISF of the switching transistor shows a huge increment when these transistors enter triode region. Noting that the transistors' ISFs do not show a considerable change, we can link this transition to their NMFs, which have a direct dependency on their conduction time.

Third: The main superiority of class-C over class-B is its impulse-like currents [21], which will be vanished if core transistors enter triode region.

Forth: The switching pair noise and the Flicker noise of the tail transistor contribute significantly to the total phase noise when the core transistors work in triode region for a considerable portion of oscillation period. To illustrate this, we conducted a noise contribution simulation on the circuit of Figures 1 and 5 shows the simulation results. The circuit oscillates at $f_{\text{osc}} = 2$ GHz and phase noise has been obtained at 1 MHz offset and is plotted versus the bias current I_{CS}. Noting Figure 5(a),

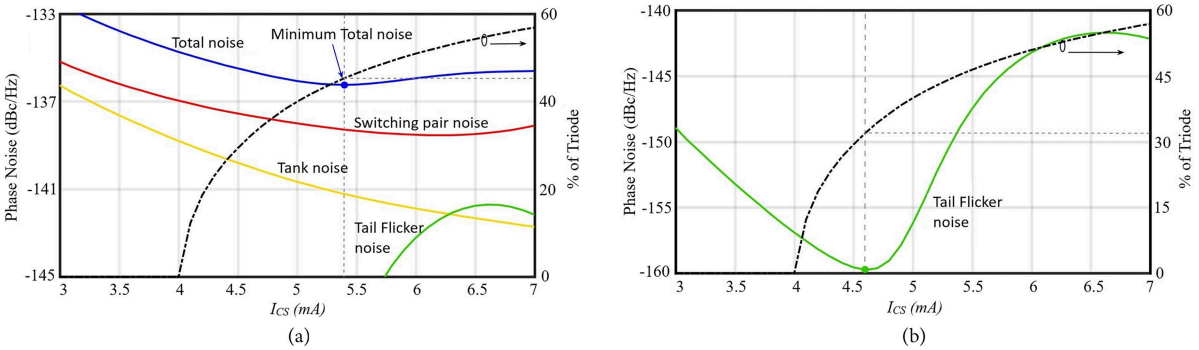

Figure 5. (a) Noise contribution simulation results in circuit of Figure 1. Center frequency is 2 GHz and the design variables are specified in Figure 1. V_B is set close to V_{th} and (b) The tail flicker noise with full dimension.

noise of tank circuit barely has an effect on the total noise behavior, as its decreasing trend does not change once the core transistors enter triode. In this case, noise behavior is defined mostly by the tail transistor's Flicker noise and the core transistors' thermal noise; the tail Flicker noise was totally negligible in low bias currents (see Figure 5(b)), whereas becomes an effective contributor in high bias currents [20] has used Groszkowski effect [24] to justify this phenomenon and referred to it as "Incremental Groszkowski" effect. It has shown that the mentioned effect occurs only at high bias currents, where the oscillator is working in voltage limited regime (see Figure 3(a)), and core transistors have entered triode region. Under this condition, Flicker noise of the tail current source can be converted to phase noise through Incremental Groszkowski effect, whereas in low bias currents this mechanism is absent which is consistent with the noise contribution result shown in Figure 5. Also the switching pair noise is the most determinant part especially when it gets the increasing trend in high bias currents (deep triode region).

Now we wish to take a closer look at Figure 5. From Figure 5(a) it can be inferred that at the minimum total phase noise point, the core transistors work in triode region for 45% of their conduction period. In the previous section, we obtained 40% as the triode percentage of core transistors in analytical $V_{S,DC}$ peak point (which has to be the maximum FoM point). How can this 5% difference be interpreted?

To answer this question, first note that the maximum FoM always happens in a lower bias current than the minimum phase noise; since it also depends on power consumption which increases linearly with the bias current. So starting from the minimum phase noise point (I_{CS}=5.4 mA), the I_{CS} is deceased by 0.1 mA current step. At each point, ΔFoM_+ (FoM increment due to less power consumption) and ΔFoM_- (FoM decrement due to more phase noise) will be calculated and compared using the following formulas.

$$\begin{aligned}\Delta FoM_+ &= 10[\log(V_{DD}I_{CS} - \log(V_{DD}(I_{CS} - 0.1mA)] \\ &= 10\log\left(\frac{I_{CS}}{I_{CS}-0.1}\right) \\ &\cong 10\log(1+\frac{0.1}{I_{CS}}) \cong \frac{1}{I_{CS}\times\ln 10},\end{aligned} \tag{13}$$

$$\Delta FoM_- = \Delta PN_+. \tag{14}$$

In Eq. (13) we have assumed the bias current in each step is decreased from I_{CS} to $I_{CS} - 0.1$ mA and then twice using the Taylor approximation provides $1/(I_{CS} \times \ln 10)$ for ΔFoM_+. Also Eq. (14) states that the FoM decrement is directly equal to the phase noise increment. The results are provided in Table 2. According to this table decreasing I_{CS} until 5 mA improves the FoM, but further lowering will start to deteriorate it. Therefore, the optimal bias current is 5 mA, equal to that extracted from the analytical curve of Figure 4 in Section 2.1. So maximum FoM happens at the bias current which maximizes $V_{S,DC}$.

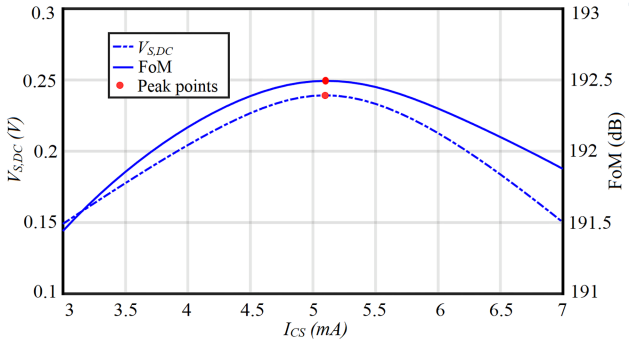

Figure 6. Simulated FoM and $V_{S,DC}$ versus I_{CS} in the circuit of Figure 1. Center frequency is 2 GHz with design variables specified in Figure 1 and $V_B \cong V_{th}$.

Table 2. Transferring from the minimum phase noise point (I_{CS}=5.4 mA) to the maximum FoM point (I_{CS}=5 mA).

Change of current (mA)	ΔFoM_+	ΔFoM_-	FoM trend
5.4 → 5.3	0.080 dB	0.01 dB	↑
5.3 → 5.2	0.082 dB	0.03 dB	↑
5.2 → 5.1	0.084 dB	0.06 dB	↑
5.1 → 5.0	0.085 dB	0.07 dB	↑
5.0 → 4.9	0.087 dB	0.10 dB	↓

Finally, Figure 6 shows the simulated $V_{S,DC}$ and the FoM versus bias current. Exact coincidence of peaks of these two curves again verifies the validity of our concept.

3. Simulated and measurement results

In order to provide an evidence for the integrity of the proposed idea, a proof-of-concept class-C oscillator prototype (based on Figure 1) using discrete components is fabricated. The discrete transistors used in the oscillator are FDN335N by ON-Semi corporation. The values of tank capacitor and inductor are $C = 1$ nF and $L = 100$ nH. Hence the calculated oscillation frequency becomes $f_{osc} = 15.9$ MHz, but the measured oscillation frequency is between the range of 14 MHz to 15 MHz (varies by the bias current) due to parasitic capacitance of the active devices.

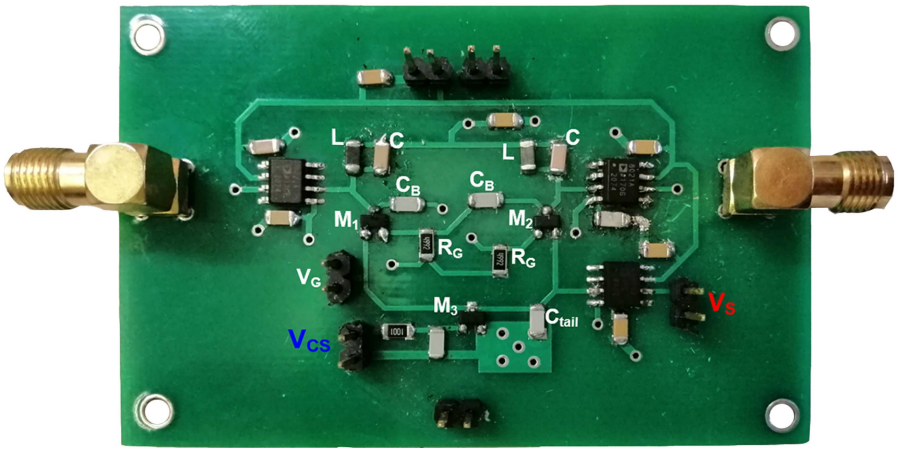

Figure 7. PCB photograph from the implemented class-C prototype oscillator.

A photograph of the implemented PCB is shown in Figure 7. Component names are corresponding to Figure 1. Output signals (including output oscillator voltage and common source node voltage) are shown in red and input signal V_{CS} (bias voltage of the current source transistor for controlling I_{CS}) is shown in blue. Three op-amps (AD8021 by Analog Devices) have been used as buffers to isolate output signals from the oscillator and drive the 50 Ω input impedance of measurement equipment.

To provide measurement data supporting previous claims, the bias current of the oscillator has been swept by varying the gate bias voltage of the current source transistor (V_{CS}) within the oscillator operational range. The gate bias of the core transistors (V_B) has been fixed to 1 V. For each V_{CS}, the associated phase noise has been measured with Agilent E5052B Signal Source Analyzer in 1 kHz to 1 MHz offset frequency range. For instance, the measured phase noise with $V_{CS} = 1.5$ V is shown in Figure 8.

The measurement results are provided in Figure 9. The oscillation amplitude (parameter A in previous discussions) is plotted in Figure 9(a). The gradual saturation trend in oscillation amplitude is obvious from this figure. Also the phase noise in 1 kHz offset is measured and shown in the same plot. For V_{CS}=1.3 V, the phase noise has its minimum. In Figure 9(b), the FoM and $V_{S,DC}$ are plotted along the same interval of V_{CS}. This plot demonstrates both FoM and $V_{S,DC}$ have their maximum values at $V_{CS} = 1.3$ V point. So $V_{S,DC}$ reaches to its peak when the FoM is maximum, and this is the optimal point of operation for oscillator. This confirms the idea through paper. This graph also shows that optimizing the bias current in this case can lead to 10 dB improvement in FoM.

Furthermore, the simulated FoM of the oscillator in Figure 1 with values in Table 1 which is shown in Figure 6 (with the maximum point of 192 dB) has been compared with some simulated FoM of previous works, and the result is expressed in Table 3. Also, referred to Figure 6 optimizing the bias current can lead to 1dB FoM improvement in the shown interval. Extensive simulations show that in other technology corners this improvement can be increased up to 6 dB.

Table 3. Simulation results comparison on FoM with previous works.

This work	Tech. (nm)	Freq. (GHz)	FoM (dB)
	180	**2**	**192.5**
[1]	130	2.68	192
[7]	130	3.4	188.1
[3]	180	1	186.4
[19]	65	10.8	190-191

4. Future work

Using the proposed idea as the criterion, a robust self-optimized oscillator may be designed using a feedback loop that maximizes DC voltage of the tail node in order to gain the maximum achievable FoM. If the frequency of the feedback loop is considerably lower than the frequency of the oscillator itself, then in each period of the oscillator its bias remains unchanged and so the oscillator would be stable. Therefore, if the oscillator works in GHz, then a several KHz feedback loop (updating the bias point in less than 1ms) guarantees that the oscillator remains stable.

5. Conclusion

A novel way to gain the maximum Figure-of-Merit (FoM) from a class-C oscillator with the related theoretical analysis has been presented in this paper. The validity of this approach has been confirmed through both simulation and measurement results. The new idea, unlike some of the mentioned literatures does not

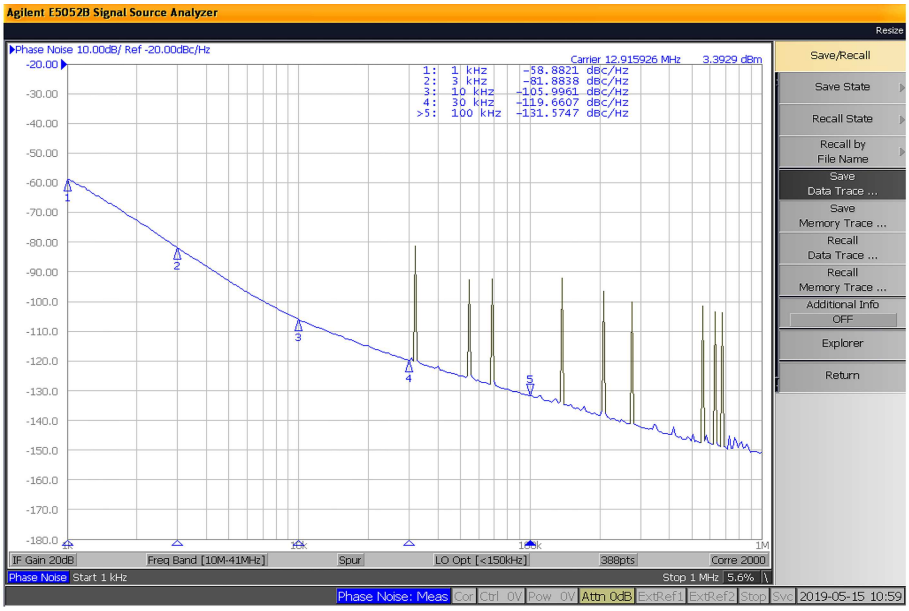

Figure 8. Measured phase noise of the prototype with Agilent E5052B Signal Source Analyzer at 1 kHz to 1 MHz offset, with $V_B = 1.5$ V. A 20 dB attenuator is used to protect the Signal Source Analyzer, so the carrier power should be added with 20 dB. Also note that this result is obtained for single ended output. Differential output phase noise values would be 3dB lower due to doubling the output power.

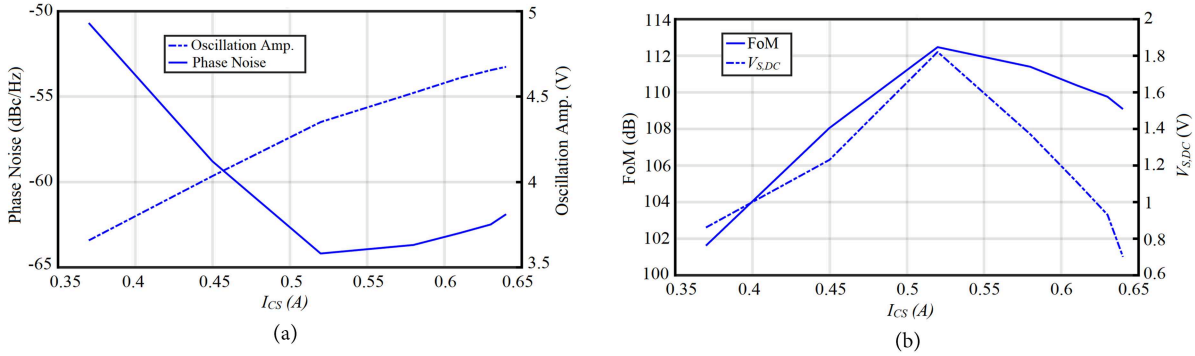

Figure 9. Measured (a) oscillation amplitude and phase noise, (b) FoM and $V_{S,DC}$ of the prototype oscillator.

introduce any loading effect on the output tank and is also authentic in any PVT situations. The feedback loop designed based on the proposed idea can be added to any previous work on class-C oscillator to optimize its bias point and FoM.

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