Low Power 10-Bit Flash Analog-to-Digital Converter with Divide and Collate Subranging Conversion Scheme

Farhana Begum¹, Sandeep Mishra², and Anup Dandapat¹*

¹Department of Electronics and Communication Engineering
National Institute of Technology Meghalaya, Shillong 793003, IN

²Department of Electronics and Communication Engineering
Indian Institute of Information Technology Pune, Saswad-Bopdev Rd, Pune 411048, IN

email: farhanajubi@gmail.com, ssandeep.mmishra@gmail.com, *anup.dandapat@nitm.ac.in
Mobile: +919706767077, +919436359828, +919485177019

Abstract

The sampling rate plays a key role in wireless applications at very high-frequency range. Flash analog-to-digital converter (ADC) betters the slow converter counterparts in this regard but bulky at inevitable high resolutions. A state-of-the-art Divide and Collate (DnC) algorithm is proposed to design the flash ADC at subranging levels. The offset voltage is kept at a minimum through the comparators used for novel coarse and fine conversion separately. The kick-back noise is also reduced by using sample and hold switches at the input. The 10-bit ADC architecture is designed with 45-nm CMOS technology and analyzed in the SPECTRE environment. A trivial variation in the transconductance with temperature is observed and consequently the offset drift with temperature is found to be 0.015 mV/°C. The design improves the INL by 0.42 LSB and DNL by 0.3 LSB. Signal-to-noise-and-distortion (SNDR) ratio and spurious-free-dynamic-range (SFDR) are 51.8 dB and 62 dB respectively at a frequency range near the Nyquist rate with a supply voltage of 1 V and input frequency of 500 MHz. Subranging scheme minimizes the comparator requirements which is reflected in the 44% reduction in the power dissipation.

Keywords

Analog-to-digital converter (ADC), comparator, Differential Non-Linearity (DNL) flash-ADC, Integrated Non-linearity (INL), Kick-back noise, reference level, subranging ADC.

I. INTRODUCTION

Exponential growth in the usage of battery operated devices like cell phones, laptops and portable medical instruments has made power consumption and speed as prominent design issues. The modules that are commonly used in a system on chip process all the data within the chip. However, when the system needs to interact with the outer world, an analog-to-digital converter (ADC) is used [1]. The ADC stands as a fundamental interfacing device to communicate with real world applications. A good synchronization with the digital sub-modules is of primary consideration while operating an ADC. Therefore, high sampling rate is taken as a major architectural constraint by many designers [2], [3].
Successive-approximation-register (SAR)-ADCs [4] have several circuitries like digital-to-analog circuits, control circuitries, and comparators. High resolution ADCs can be implemented with lesser complexity using sigma-delta (Σ∆) [5] counterparts but maintaining a good power efficiency is a challenging task [6]. Σ∆ ADCs produce an average output from a stream of band-limited inputs. Mapping between the output and input thus becomes decisive and can cause conversion error. Time-interleaved, pipelined and flash ADCs are used for carrying out high speed conversions, which provide high sampling frequency ($f_s$) in excess of 2 GHz [7]–[8]. Effective Number Of Bits (ENOB) is dependent on the noise components present in a signal. The primary design strategy is to maintain ENOB of 95% for input frequencies up to ($\frac{f_s}{4}$) and better than 90% with Nyquist frequency ($\frac{f_s}{2}$). Time-interleaved ADC architecture is also used widely nowadays to make the circuit functional faster with lower power dissipation. One major advantage of time-interleaving is its integrity with all ADC types. Time-interleaved ADC [7] can operate in high speeds, however, it imposes stringent gain-bandwidth requirements. Any synchronization mismatch between these interleaved channels would cause malfunctioning of entire architecture. Another alternative is the usage of pipelining [8] which allows the evaluation of least significant bits (LSBs) during determination of most significant bits (MSBs).

Flash converter stands to be one of the most viable option for high speed medium resolution conversion suitable for wireless communications [8]. The number of comparators increases exponentially in the order of $2^N - 1$ as depicted in Figure 1. Subranging architectures can reduce the requirement of excessive amount of comparators. Additional strategies such as assisted low power ADCs and partial switching are used to improve the energy efficiency [9]–[14]. In [9], time interleaved architectures using capacitive based digital to analog converters (DAC) have been used. A temperature non-varying subranging ADC through switching algorithm has also been proposed in [10]. Both algorithmic and architectural developments have been carried out in integrating flash ADCs. A reference voltage based calibration is presented in [15], while an optimized comparator offset combination to achieve the highest ENOB is shown in [16]. An adjustment scheme is incorporated between differential and common-mode reference voltages for improving the ADC linearity. Using excessive number of comparators in flash ADCs [17]–[20] with higher resolutions lead to high power requirement and integration space.

Studies have shown that all reference levels are not necessary for determining the MSBs. In the design of sub-ranging architecture, initial levels are termed as coarse levels and sub-divisions of the coarse levels are termed as fine levels [21]–[24]. A two-step time-interleaved ADC is introduced by Figueiredo et al. to reduce the number of comparators [21]. Two fine ADCs of same size are connected after the MSB generation with a time gap of 1 phase required for settling. It reduces power dissipation to a great extent but additional delay limits the resolution limit. An additional offset calibration scheme is employed in [22] to correct non-linearity and gain error generated by the residue amplifier used. Offset calibration eliminates the coarse ADC errors those are normally passed to the vulnerable fine ADCs. Digital subranging technique is proposed to speed up the ADC operation using the selected voltage levels generated after the coarse comparisons [23]. Above 50% of total power is dissipated in sample and hold (S/H) and fine converters. Thus, efforts have been made to reduce the height (number of comparators per stage) of fine comparators to reduce power consumption. These design considerations certainly improve subranging architecture performance, but organizing fine comparators in terms of both height and width still remains a challenging task.

Many algorithms for sub-ranging architectures have also been defined which are broadly categorized as the binary search and
frequency scaling algorithm [24]. In binary search algorithm input voltage level is searched using divide and search mechanism. Another sub-ranging methodology is dynamic architecture and frequency scaling (DAFS) based algorithm. In this method, the same resolution of binary search scheme is used. Improvement in the binary searching is made to achieve a performance which is in between traditional flash and binary search. It evaluates excess delay (EXD) which takes both the cycle delay and reset margin into consideration. The binary search versus flash ratio (BF) is also determined that helps in canceling the EXD generated in the algorithmic based subranging architectures [25]. As, coarse and fine levels are basic steps in the design of subranging ADC, two different comparators for coarse and fine levels are proposed. Arrangement of coarse and fine level comparators using the algorithmic approaches is explored in this paper. Power optimization at low additional conversion delay is targeted through a proposal of the state-of-the-art Divide and Collate (DnC) subranging conversion algorithm.

The remainder of the paper is structured as follows: Proposed Subranging level (coarse and fine) designed with different comparators (dynamic charge sharing based) is discussed in Section II. Conversion scheme using proposed DnC algorithm is elaborated in Section III with a comparison among algorithmic based subranging architectures followed by an in-depth analysis and performance comparison for proving the efficacy of the architecture. Section V concludes the paper.

II. DESIGN PROPOSAL OF COMPARATOR FOR COARSE AND FINE LEVELS

Comparators constitute a basic portion of ADC structure as these occupy approximately 70% sectional area of the ADC. The offsets present in comparators often affect the non-linearity performance of ADC namely the integrated-non-linearity (INL) and differential-non-linearity (DNL). Designs of two comparators using charge-sharing based mechanism as shown in Fig. 2 are used in this work throughout such that the offset characteristics change remains minimal with PVT (process, voltage, temperature) variations. However, this increases the kick-back noise as the gain of the comparator increases to large extent. So, sampling and hold switches are connected at the input terminals. At first, the coarse comparator (CCMP) is described in Figure 2(b) which has a large offset but it did not affect the comparison process as only the MSB bits are determined using this comparator. Subsequently, the fine conversion comparator (FCMP) is discussed as shown in Figure 2(a) that is necessary to keep the comparator offset to LSB/4, and therefore a calibration step of 0.07 mV is required.

Designs of many comparators have been shown in [26]-[32] of literature. The authors lucidly propose designs with low power but thereby has excessive delay also affecting the circuits’ functionality of working in low voltage. The single tail transistor [29] allows passage of current through both the differential pairs and the latch pairs which draws more amount of current through a single gate transistor thereby requiring a large gate area.

Another attempt to nullify the effect of a single transistor carrying both the current through the latch and differential stage is the usage of double tail comparator [30] but with the presence of an inverted clock. However, at any stage if the driven clock and the driving clock has a mismatch in timing there would be delay in regeneration of the process and the circuit would malfunction at that scenario. The reference voltages necessary for comparison purposes are generated using resistor-based array as these have slightest variation with temperature rather than the reference voltage generation using offset-variation of comparators whereby there are large variations with temperature.
A. Subranging Comparator Design

To overcome the latch regeneration speed, the authors in [32] propose a design where they use a charge sharing mechanism wherein the node immediately discharges to ground instead of creeping in through an inverter stage but with the presence of an inverted clock. However, this design suffers from the major drawback of clock slew.

If somehow, there is no proper synchronization of the driven and the driving clock, then there would be delay at the precharge phase and the regeneration process would malfunction at that scenario. Two charge sharing based comparators are used throughout. Comparators used for design of the subranging ADC have been depicted in Figure 2. LSBs [28] for the conversion are determined from the comparator design portrayed in Figure 2(a) due to their massive usage in the subranging structure compared to the number of coarse comparators. The operation of the used higher resolution charge shared circuits depicted in Figure 2(a) involves two phases: precharge and the evaluation. The operation is as follows:

1) **Precharge phase**: During this phase, CLK is in reset state; the transistors $T_1$ and $T_4$ are pulled up to $V_{DD}$.

2) **Evaluation phase**: This phase starts the mark of the evaluation phase with CLK value “1”. At the evaluation phase, the voltage applied goes to the input transistors namely $T_5$ and $T_6$ in Fig. 2(a). Depending on the applied voltage input, the transistors $T_5$ and $T_6$ discharge. When the path gets discharged, the voltage is sufficient to turn on the transistor $T_{10}$ and $T_{12}$, the nodes OUTA and OUTB gets immediately charged to $V_{DD}$.

Subsequently for coarse level comparisons, an energy efficient back feeding based comparator is presented in Figure 2(b). The precharge phase is similar to the previous comparator with the exception of the decoupling of evaluation transistors $T_7$ and $T_{10}$. During the evaluation phase, the node OUTA or OUTB discharges depending on the rate of the input voltage applied to the sensing input transistors, $T_7$ and $T_{10}$ respectively. The charge difference between back feed nodes C and D do not contribute to the operation speed of the evaluation process. The delay in the circuitry is reduced by adding a back feeding discharge circuitry formed by C-$T_9$-E or D-$T_8$-E which provides an immediate bypass for the discharge path. The $T_7$-$T_8$ paves a low resistance path to the tail current during the evaluation phase. This mechanism of back feed nodes discharging improves the regeneration and amplification process by minimizing the transistor parasitics. Unlike a conventional latch storage where $T_2$-$T_5$ and $T_3$-$T_6$ inverters carry the evaluation result output nodes (OUTA and OUTB) hold the result through strong pass transistor $T_2$-$T_5$ and $T_3$-$T_5$.

However, when a voltage difference of less than 0.01 mV is applied between the input nodes A and B, the difference between output nodes OUTA and OUTB are not sufficient enough to latch on to the value in Figure 2(b), so the circuit in Fig. 2(a) is used. The secondary amplifier comes into effect and the value then immediately turns on either of the transistors $T_{10}$ and $T_{12}$ thereby providing an immediate path for discharge. The process improves the regeneration time as the control circuitry comprises a charge sharing circuitry with transistors $T_1$-$T_4$. It is seen that as soon as the charge sharing circuit turns on, the value is latched on to the supply voltage. This makes the process faster as the charging and discharging time is less.

B. Analysis of Subranging Level Comparators

Current through the input transistors is pulled down due to the presence of the extra circuitry, thereby a low resistance path through the input is formed and results in high gain of the comparators which consequently yields high kick-back noise. The
comparators modeled maintain a constant current to transconductance ratio \( \frac{I_{d5}}{g_{m5}} \) (fine comparator) and \( \frac{I_{d7}}{g_{m7}} \) (coarse comparator) with variation in temperature as depicted in results and is discussed later. The mismatch parameter between a comparator and input referred offset can cause conversion errors. The conversion error is due to the inability to make difference in comparator input resolution. The error can be in any limits for any design. However, certain tolerance level can be neglected. The design here uses a tolerance limit of 0.5 LSB to -0.5 LSB.

The non-linearity performance is a prime metric in the design of ADC and it affects the performance of ADC. The problem degrades if the comparator offset is not removed. Therefore, several attempts are made to eliminate the offset based on the design topology. The input referred offset voltage before calibration \([33]\) is given by

\[
V_{os} = \delta V_{5,6} - \frac{I_{d5}}{g_{m5}} \left( \delta \frac{\beta M_{5,6}}{\beta M_{5}} \right) \tag{1}
\]

where \( \delta V_{5,6} \) and \( \beta M_{5,6} \) are the threshold and current mismatches respectively in the differential pair transistors \( T_5 \) and \( T_6 \). The transistors \( T_7 \) and \( T_8 \) are in strong inversion region. As a result the ratio is given as \( \frac{I_{d7}}{g_{m7}} \) is given by \([33]\)

\[
\frac{I_{D7}}{g_{m7}} = \frac{V_{gs7} - V_{T7}}{2} \tag{2}
\]

The threshold voltage is independent of temperature because the body effect is completely eliminated as the source and substrate are connected together. The transistors \( T_5 \) and \( T_6 \) are in weak inversion during regeneration phase. Since the transistor \( T_5 \) is in weak inversion, the current through \( T_5 \) is given by

\[
I_{d5} = \frac{W_5}{L_5} I_T \left( \frac{V_{GS5} - V_{T5}}{q} \right) \tag{3}
\]

\( k_T \) is the boltzman constant and \( q \) is the elementary charge. Therefore,

\[
V_{GS5} = V_{T5} + \frac{n k_T}{q} \ln \frac{I_{d5}}{I_T} \tag{4}
\]

### III. Proposed Divide and Collate Conversion Algorithm

Flash ADCs are widely used for high speed conversion though these are not a viable option from power perspective. As discussed, the traditional binary search conversion scheme performs with substandard EXD which is near non-feasible at higher sampling frequency. This scheme is later explored by Yoshioka et al. \([25]\) to reduce the excess delay. Subranging ADCs have a major limitation in the requirement of higher fine levels. The conversion delay is given as

\[
t_{FL} = 2t - \text{comp delay} \tag{5}
\]

Therefore, improvement in the conversion algorithm plays a pivotal role in reducing the architecture latency. A DnC conversion scheme is proposed to reduce EXD and achieve low stage level comparator requirement compared to traditional flash ADCs. All the comparators \((2^N-1)\) are activated at an instant in a flash ADC (e.g.: 15 comparators are activated in the
first cycle of a 4-bit flash ADC). The conversion process has several operating cycles. The power in flash ADC is given by:

\[ P_{FL} = (2^N - 1) P_{comp} \]  \hspace{1cm} (6)

The energy per conversion for flash ADC is high as more number of comparators are used for the conversion stage.

A. Binary Search Algorithm

The discussion starts with the binary search algorithm followed by the improved dynamic architecture. Thereafter, the proposed DnC is introduced and compared with respect to excess delay and conversion energy. The schematic of the binary search algorithm is shown in Fig. 3. In binary conversion, all the comparators are connected in a divide (voltage levels) and search (selection) mechanism. A sampled signal is provided as \( V_{IN} \) that goes through decisive circuit which activates the mid-level voltage to select the upper set or lower set of reference voltages. In this way, the conversion is carried out in multiple cycles unless the LSB is determined. A 4-bit flash architecture is illustrated in Fig. 3 wherein an input voltage of 630 mV is selected at the clock sampling instant with the resistive reference ladder voltage difference of 1 V (\( V_{REF^+} = 1 \), \( V_{REF^-} = 0 \)).

Each level has a voltage of 62.5 mV. Therefore, \( V_{IN} \) of 630 mV will activate the set of decisive circuits as highlighted in Fig. 3 (\( 8 \), \( 12 \), \( 10 \) and \( 9 \)) resulting in encoded digital outputs of ‘1010’. This means at one cycle of comparison not all the comparators are selected and hence the flash conversion is optimized. The figure-of-merit (FoM) is given by:

\[ FoM = \frac{P_{FL}}{f_s \times 2^{ENOB \text{ per cycle}}} \]  \hspace{1cm} (7)

where \( f_s \) is the sampling rate.

Thus, the FoM using this scheme is low compared to the flash-type but with higher conversion delay.

B. DnC Conversion Scheme

Despite the higher sampling rate, flash ADCs irrespective of the subranging scheme suffer from two major performance issues: 1) higher energy per conversion stage; 2) requirement of excessive number of comparators at higher resolutions. The attempt to combat the trade-off between power and delay discussed in previous section has driven to the development of DnC conversion algorithm. The proposed subranging 10-bit flash-ADC is shown in Fig. 4, which comprises a set of reference voltages, an array of comparators and multiplexers. This concept of subranging stems from the identification of a set of reference voltages around sampled input for the next step of fine mode conversion. The two intermediate fine mode reference voltages are determined by using a selector (MUX) which is controlled by the preceding coarse/fine mode output. The presence of fan-out of the MUX thereby increases, creating large capacitance at the output which limit the speed of optimization. This issue can be minimized by placing moderate number of comparators (8 or 4 as elaborated later) to provide the best energy delay trade off. These levels have been chosen after analysing other subranging schemes [34]–[37] those provide limits of per stage conversion/switching to maintain good power-delay trade-off. In the proposed architecture, the concept of voltage divisions and distribution are used. A set of resistors are well equally spaced with the nodes carrying voltages. However, the
Algorithm: Divide and Collate Subranging Conversion Scheme

1: RESOLUTION = N;
2: COARSE COMPARATOR = A;
3: FINE COMPARATORS = B1, B2;
4: ASSIGN A, S, B1 = 8;
5: ASSIGN B2 = 4;
6: ASSIGN C1 = 1;
7: ASSIGN C2 = 0;
8: ENSURE: M = 2^N
9: WHILE A × S < M DO
10: S = S × 8;
11: C1 = C1 + 1;
12: END WHILE
13: IF A × S = M THEN
14: ASSIGN STAGES = [A] [C1 times B1];
15: END OF CONVERSION (exit);
16: END IF
17: ASSIGN T = S;
18: WHILE A × T > M DO
19: T = T / 2;
20: C2 = C2 + 1;
21: END WHILE
22: ASSIGN STAGES = [A] [(C1-C2) times B1] [C2 times B2];
23: END OF CONVERSION (exit);

Voltage is not given to the comparator directly but are rather distributed to each comparators in a novel way through the Divide and Collate conversion algorithm presented below.

The algorithm is elaborated for a 10-bit ADC. The scheme goes through one level of coarse conversion and multiple levels of fine conversions. A 10-bit ADC has 1024 number of conversion levels out of which 8 coarse comparisons are performed at the first stage. Then the fine conversion starts with at most 8 levels at each stage. The minimum number of comparisons are limited to 4 for avoiding large loading at the previous stage. It may be noted that, only 2×1 MUX for most levels and 4×1 MUX for final and/or pre-final stages are used irrespective of the ADC resolution. Therefore, the distribution is 8×8×4×4 for this design. Hence, a 48 × reduction has been achieved with mere 3 more conversion stages. The comparator regeneration time plays a significant role in deciding the ADC performance in the subranging scheme due to the extra stages. Use of a modified inverter based comparator to reduce the power and area has been demonstrated when compared to op-amp based comparators. A secondary amplifier is introduced in the proposed comparator to perform at low regeneration time as shown in Figure 2(a). The design works well at low input voltage difference but at a the cost of extra power. The coarse comparison is common at all ADC resolutions. Therefore, for power optimization an energy efficient dynamic comparator is used for higher input voltage comparison.

IV. RESULTS AND DISCUSSIONS

A subranging ADC has been designed with the proposed DnC algorithm. Furthermore, the ADC has been structured with the two proposed comparators separately for both the coarse and fine levels. Performance analyses of the proposed comparators have shown robustness over environment variations and mismatches. A faster fine comparator is chosen to reduce the architecture
latency as it is responsible for LSB determination. The proposed DnC conversion scheme improves the FoM at low additional EXD. It requires lesser number of fine conversion stages and paves an optimized comparator array distribution to provide the best power delay trade-off.

A. Performance Analysis of Subranging Level Comparators

The comparators used for conversion have been designed using the generic process design kit (GPDK) 45-nm technology. The referred designs ([29]–[32]) have been re-scaled in 45-nm design technology and their performances have been compared in the same environment as they have found a feasible platform compared to others in relevance to the parameters of power, delay and subtle kick-back noise. Table I is a depiction of comparators discussed.

The maximum operating frequency of the proposed comparator [Figure 2(a)] is higher compared to ([29]–[32]) as shown in Table I. The regeneration speed affects the output settling time; the lower value of the proposed comparators thereby improves the operating frequency. The number of transistors, power consumption, and energy consumption is lower than [30], [31] and [32] but it is seen to be more than [29]. The kick-back noise is higher than [29], [30], [31] and [32], however its gets reduced with the sampling switch connected. The kick-back noise is more without the sampling switch (worst case) and is around 0.84 mV, it gets reduced to 0.12 mV after using the sampling switch (best case) as it isolates the regeneration nodes during the evaluation phase of the comparison for the FCMP. However, the kick-back noise is quantitatively high for best case with 0.07 mV and 0.91 mV with the worst case respectively. The process corner variation performance for the two proposed comparators is noted in Table II. The design is moderately sensitive to delay with a mean deviation of 38% in the conversion of both coarse and fine level comparators and least sensitive to energy dissipation with variation of 14.5% and 21.7% respectively.

Table III is a description of state of art of various ADCs. The sampling frequency is seen to be higher compared to other architectures. The design is also capable of functioning at a low supply voltage of 0.5 V. The FoM is seen to be best amongst all the compared architectures. Figures 5(a) and 5(b) shows the temperature dependence of offset voltage with varying temperature. It shows that the offset does not drift much with respect to temperature. The ratio of current to transconductance is almost constant. \( I_{D5} \) is generated by the band gap and the temperature co-efficient where the comparators are calibrated at 27°C. The diffusion capacitance of the transistor is therefore minimized of the operating frequency. Figure 5(a) shows the change of \( I_{d5} \) with change of temperature. Putting this value in Equation (1), the temperature dependence is found very small 0.015 mV/^\circ\text{C} and can be neglected. Thus, the addition of the secondary amplifier circuitry changes \( \frac{I_{d5}}{g_{m5}} \) slightly and does not depend on temperature. Though the second order effects at high temperature affects the offset of the comparator which in turn effects the ADC performance. Thus, offset voltage becomes less at high temperatures. Figure 5(b) shows the temperature dependence on the bias point of transistor \( T_5 \). Current \( I_{d5} \) has a small temperature dependence in low temperature range. The offset voltage is seen to be high in lower temperatures and low in high temperatures with secondary amplifier. Second order channel effects come into picture at high temperature. It comprises the channel length modulation effect and the buffer size. In this work, the temperature dependence of the proposed comparator and conventional comparator are shown.

The comparator design is made in such a way that the offset is zero for a common mode voltages below 100 mV. To improve the calibration accuracy, the voltage converter is added which acts like a buffer. When a voltage is applied to the input and
a capacitor builds up a voltage and then sends the voltage to the capacitor. The capacitor charges it and sends to the drain of the NMOS. The voltage is either low or high for it. Now this voltage is applied to the transistor ends [29]. For eg, the output of the comparator when the common mode voltage is 100 mV, the output from the comparator 10 mV. The multiplexer input will take this voltage to be high and yield a high output. Then as soon as the output from the inverter goes high or low, then accordingly the NMOS turns on and the voltage from the buffer will get transmitted to the output. This will yield a low output. Thus, the introduction of the voltage down converter improves the non-linearity performance by 0.42 LSB. However, the addition of this contributes to the overall power consumption by 10%. The DNL deviation has been found to be 0.28 LSB. The standard deviation of the input-referred offset noise is less than 0.24 LSB but error of around 3.5 LSBs from Monte Carlo simulation results shown in Figure 6. Few designs are used whereby the differential and latch stage are separated from each other [24]-[26]. This separation introduces less delay and the circuit can function in better way with an offset variation of 0.52 LSBs [26] however at the cost of high power dissipation.

The Monte Carlo simulation from Figure 6(a) shows a mean offset deviation of 3.5 LSBs for fine comparator and 5.6 LSBs for coarse comparators with 1000 trials as shown in Figure 6(b).

EXD for subranging ADC is illustrated in Figure 7 which can be defined as

\[
EXD = \text{Reset margin} + \text{conversion delay}
\]  

(8)

The scheme works fine for even higher resolution ADC provided the comparison delay is at permissible limit since EXD is proportional to it and ultimately affects the sampling rate. The excess delay is greatly suppressed due to the faster discharge rate of comparators. The excess delay is primarily due to the searching of fine levels of voltage. ADC conversion consists of S/H circuit, coarse conversion and fine conversion steps. The operation is shown for a 4-bit ADC. Each cycle consists of three phases (P): S/H, coarse and fine stage. The sampling switch is closed and the applied input signal is sampled to capacitance and the switch opens at the start of the cycle P[N]. At the next phase of operation, P[N+1], MSB is determined using coarse conversion. Remaining bits are evaluated in the subsequent fine conversion. The cycle P[N+2] determines the next two fine mode of bits and in this way the process goes on [32]-[37].

Since the output is greatly dependent on the number of voltage levels, flash operation continues for another cycle when the conversion at the phase P[N+2] is prolonged. Flash ADC converts fully in the coarse level (P[N+1] phase) that allows it to cancel the EXD for the other subsequent stages. A higher reset margin is however set to synchronize with the sampling frequency. Timing diagram (Figure 7) presents energy per conversion step over various operational cycles in EXD of different flash architectures. Number of subranging stages are estimated from the following:

\[ Subranging \text{ stages (Flash)} = \frac{\text{Number of Flash conversions (M)}}{\text{Number of searches}} \]

\[ \left[ \frac{16}{16} = 1 \right] \]  

(9)
\[ \text{Subranging stages (Binary)} = \frac{\text{Number of Flash conversions (M)}}{\log_2(M^2)} + 1 \tag{10} \]

\[ \text{Subranging stages (Prop. Subranging)} = \log_2 M - Y \quad (Y \text{ is calculated from DnC algorithm}) \tag{11} \]

Equation (9)–(11) show the stage requirements (coarse + fine) of compared flash architectures. As design demonstration, 4-bit flash ADCs are discussed and the performances are summarized in Figure 7. Higher number of fine levels using binary search scheme degrades the conversion speed which may dither the conversion at higher sampling frequency. Subranging flash on the other hand has two stages and can perform with lower additional delay of 5.8 ps. Faster flash ADC dissipates higher cycle energy (FoM of 39.72 fJ in just 5 cycles) that makes it less efficient at higher resolution converters. The proposed subranging flash ADC provides the best energy-delay trade-off at medium to high resolutions.

The ADC converts a 500 MHz input signal at a sampling rate of 2.5 GS/s with a power supply of 1 V. A resistive based reference ladder as depicted in Figure 4 is used as it is quite stable over temperature mismatches with an input range of 300 mV. At this range, first division of 8 coarse levels are carried out which indicates the value of 7A, 6A, … 1A as 37.5 mV, 74.9 mV … will be compared with the input and this stage generates the MSBs \((M_{10} - M_8)\). Since the DnC scheme assigns three fine comparison stages, 8-4-4 number of comparators are used at level 1-2-3 respectively. During the test cycle, input was at 75.5 mV at the start of evaluation phase (CLK=1). Thus, the lower voltage limits are selected to be 75 mV (level-1), 77.34375 mV (level-2) and 75.5859 mV (level-3). 290 \(\mu\)V is used for 1 LSB representation.

The behavioral characteristics of compared designs have been tested at various process corners as depicted in Figure 8. The flash ADC has the highest power dissipation over all corners. The power consumed is least for all flash and binary search based ADC in slowest (SS) process corner. The power consumed is more than binary search for the proposed design but lower than flash based ADC. However, owing to the higher EXD which contributes to the overall delay in the binary search scheme, the resolution must be limited to moderate range. Figure 9 depicts the average power variation with variation of frequency and supply voltage. The average power increases by 2.36 mW/GHz over the 2.5 GHz bandwidth. The average power increment over supply voltage variation is found to be 0.10 mW/V. Figure 10 (a) depicts the power consumption of the system with temperature variation. The average power dissipation increases with increase in temperature. The power also increases for the proposed DnC based ADC except a drop at 60°C. The delay variation with frequency is depicted in Figure 10(b). The average delay is seen to be decreasing with increase in supply voltage. The rate of decrease of delay with supply voltage is 3 ps/V.

### B. Static Errors

The primary static errors in ADC are INL and DNL which arise due to the comparators difficulty in estimating below a certain voltage limit level. The input referred offset voltage is low but the common mode offset voltage is high which is removed through the use of voltage down converters as shown in Figure 4. This leads to a lower value of non-linearity errors. Even the kick-back noise is also compensated using a sample and hold switch. The input referred offset deviation is noted
to be around 72.5 µV which yields DNL of 0.24 LSB. INL and DNL deviation in the subranging ADC have been found to be 0.3/-0.22 LSB and 0.24/-0.32 LSB with an input frequency of 500 MHz and sampling frequency 2.5 GS/s as noted from Figures 11 and 12 respectively.

Monte Carlo simulations are carried out with 1000 trials. The mean value found from the plot is set as the reference point for further calculations. The non-linearity variations are then plotted in Figures 11 and 12. The results have been collected after using offset compensation in the circuits. The kick-back noise is high but as discussed previously it is compensated using the sample and hold switches. The kick-back noise for the worst case has been noted with comparators inputs $\delta V_{in}=0.1$ mV is 0.84 mV and for the best case is 0.12 mV keeping $\delta V_{in}=10$ mV for FCMP.

C. Power Dissipation Analysis

One of the limitations in flash ADC is its high power dissipation owing to high resolution bits. It arises from the fact that $2^N-1$ number of comparators are used. The DnC on the other hand requires only 20 number of comparators (1023 in traditional flash) in one coarse and three fine levels. Subranging flash with binary search conversion scheme entails 510 number of low power digital comparators. But, the binary search requires 10 stages that increases the conversion latency excessively.

Figure 13 shows the distribution of power. Resistive ladder requires 58.7% amounting to a large section of power distribution. Subsequently, the comparators (CCMP and FCMP) utilize a sparse amount of 18.4% only.

D. Dynamic Analysis

Fast fourier transform (FFT) is an important attribute to determine the signal characteristics. The frequency response is seen with variation of input frequency with a sampling frequency 2.5 GHz. The digitized signal obtained for each sampled analog value is reconstructed as analog signal by passing it through a digital-to-analog converter (DAC) whose FFT is then obtained. The dynamic response plots determine the signal-to-noise-distortion (SNDR), spurious-free-dynamic range (SFDR), ENOB with 51.8 dB, 62 dB, and 8.3 respectively at an input frequency of 500 MHz, and sampling frequency of 2.5 GS/s as shown in Figure 14(a). The simulated SNDR is seen to be 51.8 equivalent to ENOB and SFDR is 62 dB. Spurs due to the harmonic components increases near the Nyquist rate and therefore SFDR decreases near the Nyquist rate while the spurs are less near the DC frequency showing an increase in SFDR amounting to 56 dB near 500 MHz.

ENOB is found to be 9.1 at low frequency of 500 MHz and 8.3 at Nyquist rate as seen in Figure 14(a). SNDR also drops by 4.5 dB due to spurs near the Nyquist frequency as we approach from DC frequency to Nyquist range. As observed from Figure 14(b) The dynamic parameters (SNDR and SFDR) drops by a trivial amount of 7 dB while increasing the input frequency. A stable ENOB of approximately 8.3 is seen in this range. The FoM is a prime metric to measure the ADC performance. The dynamic performance with varying supply voltages have been incorporated in Figure 15 as discussed in the following subsection. It is found to be 14 fJ/conv which is 44% more as compared to [18] and comparable to [19] and [24] as seen from Figure 16. Deguchi et al have designed a faster flash ADC involving a pre-amplifier that allows the ADC to operate at higher sampling rate but the resolution is limited to moderate range.
E. Low Voltage Considerations

Modern day ADCs are integrated in SoCs with wireless power supplies. The designs are expected to operate at lower supply voltages without significant performance degradation. Transistor threshold and comparator differential input level become significant at lower supplies. The proposed subranging ADC is simulated over a range of 500 mV to 1500 mV. The performance of load current shows a sharp decrease with increase in the supply voltages. This occurs because of the presence of the comparator. The load current depends on the fan-out of the comparator and increases with increase in fan out. With the increase in supply voltage the fan out of the comparator increases and thereby the load current decreases as plotted in Figure 15. However, the peak current response is reversed with respect to the supply voltage with low average change. This is evident as the comparator power and driving current is proportional to the supply voltage. Dynamic performance (SNDR and SFDR) illustrated in Figure 15(b) show a decrement while scaling the supply voltage down. The behaviour is primarily due to the use of comparators. The glitch and kick back noise of the proposed comparator increases with increase in supply voltage. The kick-back noise is attributed to the spurious noise which is associated with comparators too. The ENOB is also proportional to the noise. As the noise increases with increase in supply voltage, the ENOB decreases. However, this circuit is capable of functioning at low voltage of less than 600 mV as it does not have any transmission gates or pre-amplifiers. The excellent performance of the design in low supply voltage makes it feasible for practical applications.

V. Conclusion

Flash ADC has gained popularity amongst ADC designers owing to its vast applicability in SoC design platforms. Design at subranging level is a must inspite of its lower conversion speed as compared to the traditional flash counterparts. This work presents a 10-bit subranging scheme for flash ADC with an optimized DnC conversion scheme, which yields better performance than binary search and flash ADC. The constituent components of the module have been improved with the use of low power charge shared CCMP and faster FCMP thereby making it better than the referred conventional designs. Performance analyses of these subranging comparators have shown stable offset across environment variations. The DnC algorithm assigns optimized number of comparators even at higher resolutions. It reduces FoM to a great extent without notable degradation in the excess delay. The design is successful in achieving power consumption of 10.5 mW with a FoM of seemingly good value. Estimation on subranging stages is made with the consideration of resolution and conversion algorithm. It shows moderate amount of stage assignments in the proposed DnC. Low power subranging comparators lead to only 18% of the ADC dissipation. Furthermore, the design is functional at a low supply voltage though with degradation of SNDR subsequently affecting the ADC dynamic performance. The design entails the utility of a ADC with a sampling rate of 2.5 GS/s which is on an average 60% more than the conventional subranging ADC topologies. The time-interleaved and pipelined ADC seemingly provide a better sampling rate, however, at the cost of higher computational complexities. This ADC succumbs to low complexity although the loading effect is notably increased with the increase in the number of MUXes. Lesser number of comparators in combination with good static and dynamic performance certainly fits the DnC subranging flash ADC into the modern electronic systems.
REFERENCES


Farhana Begum has done her B. E. in Electronics and Telecommunication from Assam Engineering College, Guwahati, India in 2012. Thereafter, M. Tech in Electronics and Communication from Gauhati University, Guwahati, India in 2014. She is currently pursuing her PhD in National Institute of Technology Meghalaya in analog and mixed signal circuits.

Her research interests include low power circuits, analog and mixed signal designs, ultra wide transreceiver designs and high data rate communication.
**Sandeep Mishra** received the B.Tech and M.Tech degrees in Electronics and Communication Engineering from the Biju Patnaik University of Technology, Rourkela, India, in 2011 and 2013, respectively, and the Ph.D. degree in VLSI design from the National Institute of Technology Meghalaya at Shillong, in 2018. He is presently an Assistant Professor with the Department of Electronics and Communication Engineering, Indian Institute of Information Technology Pune, India.

His research area of interest covers low-power VLSI design, memory design, mixed signal circuits, analog-to-digital converters, and intelligent transportation systems.

**Anup Dandapat** received the Ph.D. degree in Digital VLSI Design from Jadavpur University, Kolkata, India, in 2008.

He is presently an Associate Professor with the Department of Electronics and Communication Engineering, National Institute of Technology Meghalaya at Shillong, India. Dr. Dandapat has authored over 50 national and international journal papers. His current research interests include low-power VLSI design, low-power memory design, and low-power digital design.
Fig. 1: Flash ADC architecture with single stage coarse conversion.

Fig. 2: Proposed comparators for subranging ADC design. (a) fine level comparator. (b) coarse level comparator.
Fig. 3: Binary search based flash A/D converter (a 4 bit flash architecture is designed with decision circuits comprising comparators and selectors).
Fig. 4: Proposed 10-bit subranging ADC design with Divide and Collate conversion scheme.

Fig. 5: Decision transistor current performance variation over temperature.
Fig. 6: Comparator offset variation over 1000 runs of Monte Carlo sampling method.

Fig. 7: Energy-delay performance of various A/D conversion algorithms.

Fig. 8: System variation comparison with process corners.
Fig. 9: Average power responses over variation.

Fig. 10: Power-delay response over temperature-voltage.

Fig. 11: Integrated-non-linearity (INL)

Fig. 12: Differential-non-linearity (DNL)
Fig. 13: Power distribution among various operational modules.

Fig. 14: Dynamic responses with varying system response.

Fig. 15: ADC performance analysis with supply voltage variation.
Fig. 16: Energy-delay performance of various A/D conversion schemes.
TABLE I: Performance comparison summary with referred comparators

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[29]</th>
<th>[30]</th>
<th>[31]</th>
<th>[32]</th>
<th>FCMP</th>
<th>CCMP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. Freq. (MHz)</td>
<td>900</td>
<td>1000</td>
<td>2000</td>
<td>2500</td>
<td>2500</td>
<td>2500</td>
</tr>
<tr>
<td>Delay (ps./dec)</td>
<td>54</td>
<td>24</td>
<td>110</td>
<td>27</td>
<td>16</td>
<td>21</td>
</tr>
<tr>
<td>Power (nW)</td>
<td>27</td>
<td>2061</td>
<td>4060</td>
<td>317</td>
<td>68</td>
<td>27</td>
</tr>
<tr>
<td>Supply Vol. (V)</td>
<td>1</td>
<td>1</td>
<td>1.2</td>
<td>1</td>
<td>0.5</td>
<td>0.6</td>
</tr>
<tr>
<td>Energy/ Conv. (fJ/conv)</td>
<td>3.03</td>
<td>17.07</td>
<td>19.07</td>
<td>38</td>
<td>5.8</td>
<td>4.13</td>
</tr>
<tr>
<td>No. of trans.</td>
<td>9</td>
<td>14</td>
<td>15</td>
<td>14</td>
<td>12</td>
<td>11</td>
</tr>
<tr>
<td>Kick-back noise (worst-case(mV))</td>
<td>0.78</td>
<td>0.4</td>
<td>0.3</td>
<td>0.72</td>
<td>0.84</td>
<td>0.91</td>
</tr>
<tr>
<td>Kick-back noise (best-case(mV))</td>
<td>0.64</td>
<td>0.23</td>
<td>0.3</td>
<td>0.43</td>
<td>0.12</td>
<td>0.07</td>
</tr>
</tbody>
</table>

TABLE II: Energy-delay analysis of subranging comparators under process variation

<table>
<thead>
<tr>
<th>Comparator</th>
<th>Parameter</th>
<th>SS</th>
<th>SF</th>
<th>FS</th>
<th>FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coarse level</td>
<td>Energy (fJ/convstep)</td>
<td>0.065</td>
<td>0.079</td>
<td>0.078</td>
<td>0.087</td>
</tr>
<tr>
<td></td>
<td>Delay (ps)</td>
<td>16.6</td>
<td>16.9</td>
<td>6.3</td>
<td>4.9</td>
</tr>
<tr>
<td>Fine level</td>
<td>Energy (fJ/convstep)</td>
<td>0.077</td>
<td>0.099</td>
<td>0.098</td>
<td>0.107</td>
</tr>
<tr>
<td></td>
<td>Delay (ps)</td>
<td>16</td>
<td>15.4</td>
<td>6.7</td>
<td>5</td>
</tr>
</tbody>
</table>

TABLE III: Comparison with state of art

<table>
<thead>
<tr>
<th>Feature</th>
<th>[1]</th>
<th>[8]</th>
<th>[21]</th>
<th>[22]</th>
<th>[23]</th>
<th>[20]</th>
<th>[25]</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>90-nm</td>
<td>28-nm</td>
<td>90-nm</td>
<td>90-nm</td>
<td>55-nm</td>
<td>65-nm</td>
<td>65-nm</td>
<td>45-nm</td>
</tr>
<tr>
<td>Resolution</td>
<td>10</td>
<td>11</td>
<td>6</td>
<td>10</td>
<td>8</td>
<td>8</td>
<td>7</td>
<td>10</td>
</tr>
<tr>
<td>Sampling freq. (GS/s)</td>
<td>0.1</td>
<td>0.02</td>
<td>1</td>
<td>0.1</td>
<td>1</td>
<td>1.5</td>
<td>1.22</td>
<td>2.5</td>
</tr>
<tr>
<td>Min. supply voltage (V)</td>
<td>1.2</td>
<td>1.8</td>
<td>1.2</td>
<td>1</td>
<td>1.2</td>
<td>1</td>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td>Input range [mV]</td>
<td>1600</td>
<td>280</td>
<td>-</td>
<td>2</td>
<td>800</td>
<td>-</td>
<td>-</td>
<td>300</td>
</tr>
<tr>
<td>INL [LSB]</td>
<td>0.95</td>
<td>1.2</td>
<td>-</td>
<td>0.9/-0.9</td>
<td>-1.2/1.2</td>
<td>0.5/-0.5</td>
<td>-</td>
<td>0.25/-0.3</td>
</tr>
<tr>
<td>DNL [LSB]</td>
<td>0.83</td>
<td>0.7</td>
<td>-</td>
<td>0.6/-0.5</td>
<td>-0.8/0.8</td>
<td>0.28/-0.25</td>
<td>-</td>
<td>0.28/-0.21</td>
</tr>
<tr>
<td>SNDR [dB]</td>
<td>56.4</td>
<td>61.8</td>
<td>33.8</td>
<td>58</td>
<td>43.5</td>
<td>38</td>
<td>36.2</td>
<td>51.8</td>
</tr>
<tr>
<td>SFDR [dB]</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>75</td>
<td>55</td>
<td>47</td>
<td>-</td>
<td>62</td>
</tr>
<tr>
<td>Power [mW]</td>
<td>68.3</td>
<td>2.24</td>
<td>55</td>
<td>6</td>
<td>16</td>
<td>35</td>
<td>8.11</td>
<td>10.5</td>
</tr>
<tr>
<td>FoM [pJ/conv]</td>
<td>-</td>
<td>0.111</td>
<td>-</td>
<td>0.092</td>
<td>0.125</td>
<td>0.42</td>
<td>0.125</td>
<td>0.014</td>
</tr>
<tr>
<td>ENOB [Bits]</td>
<td>9.08</td>
<td>-</td>
<td>5.3</td>
<td>9.34</td>
<td>7</td>
<td>6</td>
<td>-</td>
<td>8.3</td>
</tr>
</tbody>
</table>