

# Performance Improvement of AC-DC Power Converters under Unbalanced Conditions

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**Abstract**— In this paper, a single synchronous reference-frame based control method is proposed to improve the performance of AC-DC interlink converters feeding DC loads under unbalanced AC grid conditions. Unbalanced grid voltages cause undesirable double frequency ( $2\omega_0$ ) oscillations on the DC link voltage in AC-DC converters. In the medium/high power applications, low switching frequency, and the oscillatory power of the input filter considerably degrade the functionality of the existing methods for removing  $2\omega_0$  ripples from DC link voltage. In this paper, an analytical equation for the terminal active power is derived considering the input filter inductance. Accordingly, suitable current references for the control are proposed to eliminate the undesirable  $2\omega_0$  ripples from DC-link voltage considering also low switching frequency. It is shown that the filter inductance adds a non-linear term to the active power equation which complicates the current reference calculation. Also, a real-time recursive method is proposed to solve the equations and find the current references. To evaluate the performance of the proposed method, different grid unbalanced conditions, including asymmetrical short circuit faults, are applied to a test system in the PSCAD/EMTDC environment. Furthermore, the functionality of the proposed method is compared with an existing method for unbalanced conditions.

**Keywords**— AC-DC power converters; Asymmetrical short circuit faults; DC link voltage control; interlink converter; unbalanced input voltages.

## I. NOMENCLATURE

$m_{abc}$	Modulation indices in “ $abc$ ” frame
$m_d, m_q$	Modulation indices in grid voltage oriented synchronous “ $dq$ ” frame
$V_{gabc}$	Grid voltages in “ $abc$ ” frame
$i_{tabc}$	Terminal currents in “ $abc$ ” frame
$i_{oabc}$	Output currents in “ $abc$ ” frame
$V_{gdq}$	Grid voltages in grid voltage oriented synchronous “ $dq$ ” frame
$i_{tdq}$	Terminal currents in grid voltage oriented synchronous “ $dq$ ” frame
$i_{odq}$	Output currents in grid voltage oriented synchronous “ $dq$ ” frame
$i_{td}^*, i_{tq}^*$	Terminal current references in grid voltage oriented synchronous “ $dq$ ” frame
$V_{td}^*, V_{tq}^*$	Terminal voltage references in grid voltage oriented synchronous “ $dq$ ” frame produced by current controller
$V_{DC}$	DC link voltage

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$P_g$	Instantaneous active power in the grid connection point
$P_{in}$	Instantaneous active power in converter terminal point
$P_{out}$	Instantaneous active power in DC loads side
$\omega, \theta$	Frequency and angular frequency produced by phase locked loop
$R_f$	Equivalent for input filter resistance and conduction and switching losses of the converter.
$L_f, C_f$	Converter filter inductance, and capacitance.
$P_{ref}^*$	Active power reference produced by DC-link voltage control loop
$Q^*$	Reactive power reference
$C_{DC}$	DC link capacitor capacitance
$abc/dq$	“abc” to “dq” transformation

## II. INTRODUCTION

Voltage source converters (VSC) provide efficient and controllable power conversion from AC power to DC and vice versa. DC power has been used in industrial plants [1-3], and HVDC systems [4-6]. However, in recent years, trends to use DC power in the DC grid and DC microgrid are on the rise. DC grids are a future alternative to AC grids, which benefit from high efficiency, lower weight structure and less footprint [7-10]. Specifically, medium voltage DC grids are mainly preferred in the high power industry applications.

A VSC is responsible for regulating the DC voltage and controlling the exchanged power with the AC grid [11, 12]. Therefore, any AC grid short circuit fault or disturbance directly affects the DC voltage. This becomes a more challenging issue considering the unbalanced nature of distribution systems and various asymmetrical temporary short circuit faults in AC systems [13-15]. This problem is intensified in high power applications where the DC-link voltage control-loop bandwidth (BW) is limited due to the low switching frequency [16]. A low control BW deteriorates the disturbance rejection capability of the converter [17]. Also, under unbalanced conditions, the effect of the power absorbed by the input filter inductor cannot be ignored. In this condition, the sum of the instantaneous active powers of the three phases is not zero anymore, which results in ripples with the frequency of  $2\omega_0$  ( $\omega_0$ : fundamental frequency) on the instantaneous active power injected into the DC side and DC link capacitor. Furthermore, the filter inductance introduces a right-side zero in the linearized dynamic equation of the system, which can affect the stable operation of the converter [18]. To avoid this problem, the bandwidth of the DC link voltage control loop must be lowered, which again, decreases the disturbance rejection capability of the converter. As a result, the conventional control of the DC link could not work properly under unbalanced conditions [18].

Under an unbalanced condition and during asymmetrical short circuit faults, due to the unbalanced grid voltages, the absorbed power from the grid has a pulsating component with the frequency of  $2\omega_0$ . This pulsating component flows through the DC link capacitor and causes the same frequency components on the DC link voltage. These components degrade the converter functionality and impose more stress on the capacitor, converter switches, and the DC loads (in DC microgrids application). The power converter control methods under unbalanced conditions can be divided into five categories, as follows [19-24].

1- *Instantaneous Active Reactive Control (IARC)*: In this method, the converter behaves like a symmetric resistance on all three phases and absorbs instantaneous constant active power from the grid. Also, the reactive power ripple is considered to be zero under unbalanced conditions. Although this approach provides ripple-free instantaneous active power, the output currents are highly distorted.

- 2- *Instantaneously Controlled Positive-Sequence (ICPS)*: In this method, the converter instantaneously controls the positive-sequence current in order to control the active power by forcing the negative sequence to zero. This method does not limit the reactive power ripples, and less distorted currents are drawn. However, power quality of the currents is not satisfactory yet.
- 3- *Positive–Negative-Sequence Compensation (PNSC)*: This method takes an active power from the grid by producing positive- and negative-sequence sinusoidal currents. In this scheme, sequence current components are selected such that active power  $2\omega_0$  ripples are forced to zero.
- 4- *Average Active-Reactive Control (AARC)*: In this method, the converter controls the average of the instantaneous active power. Since this method filters the active power ripples in the control system, the ripples still exist in the actual instantaneous active power.
- 5- *Balanced Positive-Sequence Control (BPSC)*: In this method, the converter only absorbs a positive sequence current from the grid. Absorbing balanced currents from unbalanced grid results in instantaneous active power with relatively large ripples.

Among the five approaches, the first three ones (IARC, ICPS, and PNSC) provide a flow of ripple-free instantaneous active power from the grid at the point of connection. However, the first two ones result in harmonic polluted currents taken from the grid, which is not permitted due to the power quality limits. The absorbed currents are sinusoidal if the PNSC method is employed. In this method, the positive and negative sequence components are selected to force the active power  $2\omega_0$  ripples to zero.

Comparing the different strategies, the PNSC method is the widely-used method in the literature to control the power converter under unbalanced conditions [19-24]. The PNSC scheme is implemented in the double synchronous reference frame (DSRF) scheme proposed by [25-27]. A DSRF simultaneously employs two clockwise and counterclockwise synchronous reference frames to control the positive and negative sequence currents. References [26] and [28] derive an instantaneous power expression at the grid connection point to calculate the current references to remove the pulsating components of the active power. They improve the converter performance under unbalanced conditions, but they do not consider the input AC filter effect. Having used the same method, [16] introduces a unified dynamic model and control strategy for the power converter. Nevertheless, because of using band trap filters in the control structure, the bandwidth of the system inherently is low. To overcome this, [29] employs an approach based on the  $\alpha\beta$  frame. Changing the frame from the grid voltage oriented synchronous  $dq$  frame to the stationary  $\alpha\beta$  frame loses the inherent benefit of the synchronous  $dq$  frame, which is the decoupling between the  $d$  and  $q$  axes and also complicates the control of the converter. Furthermore, improving the current controller in [30], the DC voltage regulation for asymmetric wind power PMSG systems in [31], instantaneous power control for suppressing the second-harmonic DC-Bus voltage in [32], power control of three-phase rectifiers under non-ideal grid conditions in [33], direct power control of PWM rectifier in [34, 35] have also been mentioned assuming PNSC method. However, none of these methods consider the input filter inductance. References [27, 29, 36] propose control methods that controlling the instantaneous active power at the converter terminals by using the terminal voltages instead of the grid voltages. Using the terminal voltages, the filter inductance is considered, and the power equations are linearized. However, the proposed controllers are non-linear. References [37-39] propose methods based on single grid voltage oriented synchronous  $dq$  frame. They propose to use a resonant compensator in the voltage control loop to mitigate the  $2\omega_0$  DC link voltage oscillations. This remedy requires high bandwidth for the voltage control loop resulting in a high switching frequency. Furthermore, this method is presented for only the inverter mode of operation, and the rectifying mode of operation has not been considered.

In this paper, first, the problem is analytically formulated in a grid voltage oriented single synchronous “dq” reference frame, which reduces the number of transformations and gives a better insight into the problem. Then, the inverter current references are calculated to remove the undesirable ripples from the active power. It is shown that the filter inductance adds a non-linear term to the instantaneous active power equation, which complicates the current reference calculation. Then, a recursive real-time strategy is proposed to find the current reference considering the filter inductance, which avoids undesirable ripples in the DC link voltage during unbalanced input voltages conditions. Furthermore, the current controller is changed in order to track the proposed current references.

The rest of the paper is organized as follows. The conventional control of the converters including the DC link voltage control strategy is introduced in section II. Section III describes the effects of the unbalanced AC grid on the DC link voltage quality. In section IV, the proposed current references calculation and the current control strategy are presented. Finally, simulation results and the conclusion of the study are provided in sections V and VI, respectively.

### III. CONVENTIONAL CONTROL OF THE POWER CONVERTERS IN NORMAL BALANCED GRID CONDITION

Fig. 1 shows the converter power circuit with its control loops and elements. In this structure, a grid voltage oriented control

strategy is used, which aligns the d-axis of the reference frame with the grid voltage space vector. Then, the working frame in this study is based on grid voltage oriented synchronous “dq” reference frame. Based on Fig. 1, the dynamic equations of the converter input filter in the grid voltage oriented synchronous “dq” frame are:

$$L_f \cdot \frac{di_{td}}{dt} = -R_f \cdot i_{td} + L_f \cdot \omega \cdot i_{tq} + m_d \cdot \frac{V_{DC}}{2} - V_{gd} \quad (1)$$

$$L_f \cdot \frac{di_{tq}}{dt} = -R_f \cdot i_{tq} - L_f \cdot \omega \cdot i_{td} + m_q \cdot \frac{V_{DC}}{2} - V_{gq} \quad (2)$$

In these equations, there are couplings between the  $d$  and  $q$  axis frames ( $+L_f \cdot \omega \cdot i_{tq}$  and  $-L_f \cdot \omega \cdot i_{td}$ ). To obtain independent dynamics, decoupling signals are fed to the current control block. Also, to compensate the load dynamics, a feed-forward from the grid voltages ( $V_{gd}, V_{gq}$ ) is used (see the current control block in Fig. 1) [40].

A PI compensator is a commonly used controller in the literature for the current control block. The optimum PI coefficients are computed from the *amplitude optimization* method [41]. Based on [41], an optimum current control PI compensator is:

$$PI = \frac{1}{\tau} \cdot \frac{L_f s + R_f}{s} \quad (3)$$

where  $\tau^{-1}$  is the bandwidth of the current control loop, which is limited by the converter switching frequency.

Considering (3) along with equations (1)-(2) and the current control block in Fig. 1, the closed-loop transfer function of the current control loops, which is of a first-order dynamic, is obtained as follows after applying the feed-forward and decoupling signals cancellation [18]:

$$\frac{i_{td}}{i_{td}^*} = \frac{i_{tq}}{i_{tq}^*} = \frac{1}{1 + \tau \cdot s} \quad (4)$$

where  $i_{td}^*$  and  $i_{tq}^*$  are the current references in the  $d$  and  $q$  axis frames in the Laplace domain, respectively.

The other blocks in Fig. 1 are described in the following subsections.

#### A. Phase Locked Loop

Converters can control the DC link voltage and inject a predefined reactive power only when they are properly synchronized with the AC grid. Therefore, a proper synchronization algorithm must be utilized. A phase-locked loop (PLL) is a commonly used method for synchronization purposes, which estimates the angle of the grid voltage space vector. In three-phase systems, a PLL processes  $v_{gq}$  with a compensator and creates a synchronous phase angle,  $\theta$ , using a resettable integrator, whose output is reset to zero whenever it exceeds  $2\pi$  as shown in Fig. 1. This integrator is implemented by means of a voltage-controlled oscillator (VCO) [41]. It is worth noting that a PLL compensator has an integrator, which guarantees a zero steady-state error in extracting the phase angle. Then, considering the grid voltage oriented control scheme,  $v_{gq}$  is settled at zero by the correct operation of the PLL [25].

#### B. Reactive Power Control Block

As shown in Fig. 1, the current reference in the  $q$  axis is computed from the reactive power set-point. The converter apparent power can be calculated in the grid voltage oriented synchronous “dq” frame as:

$$P_g + jQ_g = \frac{3}{2} \cdot (v_{gd} + jv_{gq}) \cdot (i_{td} + ji_{tq})^* \quad (5)$$

Employing the grid voltage-oriented control scheme and considering the PLL operation,  $v_{gq}$  will be derived to zero and the input active and reactive power equations can be simplified as:

$$P_g = \frac{3}{2} \cdot v_{gd} \cdot i_{td} \quad (6)$$

$$Q_g = -\frac{3}{2} \cdot v_{gd} \cdot i_{tq} \quad (7)$$

Using (7) and considering the reactive power injected by the AC filter capacitance, the current reference in the  $q$  axis will be obtained from the reactive power set point as:

$$i_{tq}^{ref} = \frac{Q_g^*}{-\frac{3}{2} \cdot v_{gd}} + \frac{3}{2} \cdot C_f \cdot \omega \cdot v_{gd} \quad (8)$$

where  $Q_g^*$  is the converter reactive power.

### C. DC Link Voltage Control Block

As mentioned earlier, control of the DC link voltage is the main duty of the converter to provide DC loads with a reliable power. The dynamic equation of the DC link capacitor can be rewritten as:

$$P_{in} = P_{out} + \frac{1}{2} \cdot C_{DC} \cdot \frac{d}{dt} (V_{DC}^2) \quad (9)$$

The conventional control scheme assumes that  $P_m$  can be replaced by  $P_g$  that is the absorbed power by the converter at grid connection point [18]. Therefore, using (6) and (9) one can write:

$$\frac{3}{2} \cdot v_{gd} \cdot i_{id} = P_{out} + \frac{1}{2} \cdot C_{DC} \cdot \frac{d}{dt} (V_{DC}^2). \quad (10)$$

In (10),  $P_{out}$  can be considered as a disturbance that can be compensated by a feed-forward signal, as shown in the DC link voltage control block in Fig. 1. The second term in the right-hand side of (10) contains a nonlinear term that complicates the DC link voltage controller design. To remove this nonlinearity and to simplify the controller design, the energy stored in the DC link capacitor  $W_{DC}$  ( $\propto V_{DC}^2$ ) is defined as a new control variable instead of the DC link voltage [42, 43]. This remedy converts the nonlinear equation (10) to a linear one as:

$$\frac{3}{2} \cdot v_{gd} \cdot i_{id} = P_{out} + \frac{d}{dt} (W_{DC}) \quad (11)$$

Equation (11) shows that  $i_{id}$  is the single control input by which  $W_{DC}$  settles at its set-point. Hence, the reference value of  $i_{id}$  must be obtained from the DC link voltage control loop as given in (12) [42] and it is shown in Fig. 1 (see DC link voltage control block).

$$i_{id}^* = \frac{P_{out}}{(\frac{3}{2}) \cdot v_{gd}} + PI \cdot (W_{DC}^* - W_{DC}) \quad (12)$$

As mentioned earlier, the first term in the right-hand side of (12) is a feed-forward signal to compensate the effect of  $P_{out}$ . Also, the PI compensator with proper tuning ensures that  $W_{DC}$  reaches its reference value with a zero steady state error.

## IV. EFFECTS OF AC GRID ASYMMETRICAL FAULTS AND IMBALANCES ON THE CONVERTER OPERATION AND THE DC LINK VOLTAGE CONTROL

The interlink converter regulates its DC side voltage and reactive power. Also, it is mentioned that asymmetrical faults and imbalances in the AC grid can disturb the DC side voltage control functionality. To discuss this challenge, assume that the AC grid voltages and currents in stationary “abc” reference frame are unbalanced as follows:

$$\begin{cases} v_{ga} = V_1 \cdot \cos(\theta) + V_2 \cdot \cos(\theta + \delta) \\ v_{gb} = V_1 \cdot \cos(\theta - \frac{2\pi}{3}) + V_2 \cdot \cos(\theta + \delta + \frac{2\pi}{3}) \\ v_{gc} = V_1 \cdot \cos(\theta + \frac{2\pi}{3}) + V_2 \cdot \cos(\theta + \delta - \frac{2\pi}{3}) \end{cases} \quad (13)$$

$$\begin{cases} i_{ia} = I_1 \cdot \cos(\theta - \alpha_1) + I_2 \cdot \cos(\theta - \alpha_2) \\ i_{ib} = I_1 \cdot \cos(\theta - \alpha_1 - \frac{2\pi}{3}) + I_2 \cdot \cos(\theta - \alpha_2 + \frac{2\pi}{3}) \\ i_{ic} = I_1 \cdot \cos(\theta - \alpha_1 + \frac{2\pi}{3}) + I_2 \cdot \cos(\theta - \alpha_2 - \frac{2\pi}{3}) \end{cases} \quad (14)$$

where subscripts 1 and 2 indicate positive and negative sequence components, respectively. Also,  $\alpha_1, \alpha_2, \delta$  are the corresponding phase angles.

Substituting (13) and (14) into (15) and some simplification results in (16), which is the total instantaneous active power flowing from the AC grid to the converter.

$$P_g = v_{ga} \cdot i_{ia} + v_{gb} \cdot i_{ib} + v_{gc} \cdot i_{ic} \quad (15)$$

$$\begin{aligned} P_g &= \frac{3}{2} \cdot [V_1 \cdot I_1 \cdot \cos(\alpha_1) + V_2 \cdot I_2 \cdot \cos(\alpha_2 + \delta)] \\ &+ \frac{3}{2} \cdot [V_2 \cdot I_1 \cdot \cos(2\theta + \delta - \alpha_1) + V_1 \cdot I_2 \cdot \cos(2\theta - \alpha_2)] \end{aligned} \quad (16)$$

The second part in the right-hand side of (16) has a pulsating nature with a frequency of  $2\omega_0$ .

Besides, the instantaneous power absorbed by the AC filter is also important in this regard. To more clarify the subject, the

instantaneous power of the input filter is:

$$P_{L_f} = L_f \left[ \frac{di_{ia}}{dt} \cdot i_{ia} + \frac{di_{ib}}{dt} \cdot i_{ib} + \frac{di_{ic}}{dt} \cdot i_{ic} \right]. \quad (17)$$

Using (14) and after some simplifications, equation (17) is changed to:

$$P_{L_f} = -3 \cdot L_f \cdot \omega \cdot I_1 \cdot I_2 \cdot \sin(2\theta + \alpha_1 + \alpha_2). \quad (18)$$

As shown in (18), the instantaneous power of  $L_f$  has a zero average value and an oscillating component with the frequency of  $2\omega_0$  in unbalanced current condition ( $I_2 \neq 0$ ). This oscillating component affects the DC side voltage, specifically, when there are severe faults and imbalances in the AC grid. In other words, flowing of an oscillating power into the DC side as well as the DC link capacitor, based on (9), causes the DC link voltage to have an undesirable ripple with the same frequency.

It is worth noting that the instantaneous power of  $P_{L_f}$  can be forced to zero by flowing balanced currents ( $I_2 = 0$ ) through the input filter. This control strategy is called BPSC scheme as described in section II which only absorbs a positive sequence current from the grid. As mentioned earlier, absorbing balanced currents from unbalanced grid results in instantaneous active power with relatively large ripples. For this reason, the studies in the literature have widely used PNSC scheme which absorbs both positive and negative sequence currents under unbalanced condition. However, the impact of filter instantaneous power  $P_{L_f}$  should be considered in the current reference calculation which is covered in this paper.

In the next section, the proposed control methods are presented to overcome the above challenges.

## V. PROPOSED CONTROL SCHEME FOR AC-DC CONVERTER UNDER UNBALANCED AC GRID CONDITION

In high power applications, the switching frequency of converters is limited to a few kHz, and therefore, the bandwidth of the current and DC link voltage control loops is rather low. This means that the DC link voltage control loop cannot compensate the pulsating components of the voltage ripples. Also, the ripples with a frequency of  $2\omega_0$  in the converter input filter are important in this case, since it affects the delivered pulsating power to the DC side of the converter.

Considering the limited BW and the input filter inductance effect, this paper proposes the current references in the grid voltage oriented synchronous “dq” reference frame to remove the ripples from the instantaneous active power and the DC link voltage. Also, the current controller ( $C_i(s)$ ) is modified to ensure an accurate reference tracking.

### A. Proposed Current References and their Calculation Approach:

In this part, the current references in the grid-voltage oriented synchronous “dq” reference frame are calculated such that the ripples with a frequency of  $2\omega_0$  in the instantaneous active power are removed. Equation (19) shows the power balance at the converter terminal.

$$P_{in} = P_g - P_{L_f} \quad (19)$$

where  $P_g$  and  $P_{L_f}$  are given in (16) and (18), respectively.

Substituting (16) and (18) into (19) and some simplification yields:

$$\begin{aligned} P_{in} &= \frac{3}{2} \cdot V_1 \cdot x_1 + \frac{3}{2} \cdot V_2 \cdot [x_3 \cdot \cos(\delta) + x_4 \cdot \sin(\delta)] \\ &+ \frac{3}{2} \cdot [V_2 \cdot x_1 \cdot \cos(\delta) - V_2 \cdot x_2 \cdot \sin(\delta) + V_1 \cdot x_3 \\ &+ 2 \cdot L_f \cdot \omega \cdot (x_2 \cdot x_3 + x_1 \cdot x_4)] \cdot \cos(2\theta) \\ &- \frac{3}{2} \cdot [V_2 \cdot x_1 \cdot \sin(\delta) + V_2 \cdot x_2 \cdot \cos(\delta) + V_1 \cdot x_4 \\ &- 2 \cdot L_f \cdot \omega \cdot (x_1 \cdot x_3 - x_2 \cdot x_4)] \cdot \sin(2\theta) \end{aligned} \quad (20)$$

where  $x_1$ ,  $x_2$ ,  $x_3$  and  $x_4$  are  $I_1 \cdot \cos(\alpha_1)$ ,  $I_1 \cdot \sin(\alpha_1)$ ,  $I_2 \cdot \cos(\alpha_2)$ ,  $I_2 \cdot \sin(\alpha_2)$ , respectively.

This equation in comparison with (6) shows the instantaneous active power at the terminal of the converter ( $P_{in}$ ) and not at the grid connection point ( $P_g$ ). As it is expected,  $P_{in}$  has a DC and a pulsating component. The DC component is equal to the constant active power reference of  $P_{ref}^*$  in Fig. 1, which comes from the DC link voltage control loop, and the pulsating part should be settled to zero. To do so, proper values of  $x_1$ ,  $x_2$ ,  $x_3$  and  $x_4$  can be obtained by solving equations (21)-(23).

$$P_{ref}^* = \frac{3}{2} \cdot V_1 \cdot x_1 + \frac{3}{2} \cdot V_2 \cdot [x_3 \cdot \cos(\delta) + x_4 \cdot \sin(\delta)] \quad (21)$$

$$V_2 \cdot x_1 \cdot \cos(\delta) - V_2 \cdot x_2 \cdot \sin(\delta) + V_1 \cdot x_3 + 2 \cdot L_f \cdot \omega \cdot (x_2 \cdot x_3 + x_1 \cdot x_4) = 0 \quad (22)$$

$$V_2 \cdot x_1 \cdot \sin(\delta) + V_2 \cdot x_2 \cdot \cos(\delta) + V_1 \cdot x_4 + 2 \cdot L_f \cdot \omega \cdot (x_2 \cdot x_4 - x_1 \cdot x_3) = 0 \quad (23)$$

Equations (22) and (23) ensure that the terminal power will not have a pulsating component, and thereby removing the pulsating component from the DC link voltage. To find the unknown four variables in equations (21)- (23), another equation is needed. By computing the grid voltage oriented synchronous “dq” frame components of the currents in (14) and substituting them into (7), the DC component of the reactive power gives the fourth equation as:

$$Q_{ref} = -\frac{3}{2} \cdot V_1 \cdot x_2 \quad (24)$$

Solving equations (21)- (24) gives the unknown variables  $x_1$ ,  $x_2$ ,  $x_3$  and  $x_4$ , which are equal to  $I_1 \cdot \cos(\alpha_1)$ ,  $I_1 \cdot \sin(\alpha_1)$ ,  $I_2 \cdot \cos(\alpha_2)$ ,  $I_2 \cdot \sin(\alpha_2)$ , respectively. Then, substituting these variables into (14) and calculating the grid voltage oriented synchronous dq frame equivalents of the currents give the current control references as:

$$\begin{aligned} I_d^{ref} &= x_1 + x_3 \cdot \cos(2\theta) - x_4 \cdot \sin(2\theta) \\ I_q^{ref} &= x_2 - x_3 \cdot \sin(2\theta) - x_4 \cdot \cos(2\theta) \end{aligned} \quad (25)$$

These current references will ensure that the undesirable oscillations on the DC link voltage will be removed.

It is worth noting that the grid voltage parameters of  $V_1$ ,  $V_2$ , and  $\delta$  are needed to solve the above equations. They can be obtained by measuring the grid voltage, transferring them to the grid-voltage oriented synchronous “dq” reference frame, and use a method based on virtual quadrature signal generator as described in [44]. Using this method ensures a minimum interference over the control loop with a fast response and a smooth overshoot [44].

As shown in (21)-(24), the equations for calculating the current references are nonlinear and cannot be solved by routine methods. To solve them, the following real-time recursive method is proposed.

#### ➤ STEP 1

Equation (26) is the first equation, which is used in the first step of calculation obtained from (21), where superscript “k” and “k-1” represent the values at “k” and “k-1” time steps. Using this equation,  $x_1^k$  can be obtained by substituting previous step values of  $x_3$  and  $x_4$  into (26). It should be mentioned that initial values of  $x_3$  and  $x_4$  ( $x_3^0$  and  $x_4^0$ ) are considered zero in the first step of simulation when running the system.

$$\frac{3}{2} \cdot V_1 \cdot x_1^k = P_{ref}^* - \frac{3}{2} \cdot V_2 \cdot [x_3^{k-1} \cdot \cos(\delta) + x_4^{k-1} \cdot \sin(\delta)] \quad (26)$$

#### ➤ STEP 2

Using  $x_1^k$  obtained by the previous step, and considering  $x_2^k$  from (24),  $x_3^k$  and  $x_4^k$  are as given in (27).

$$\begin{aligned} \begin{bmatrix} x_3^k \\ x_4^k \end{bmatrix} &= \frac{V_2}{(V_1 + 2 \cdot L_f \cdot \omega \cdot x_2)^2 + (2 \cdot L_f \cdot \omega \cdot x_1)^2} \times \\ &\begin{bmatrix} V_1 \cdot (-x_1^k \cdot \cos(\delta) + x_2^k \cdot \sin(\delta)) + 2 \cdot L_f \cdot \omega \cdot \sin(\delta) \cdot (x_1^{k2} + x_2^{k2}) \\ -V_1 \cdot (x_1^k \cdot \sin(\delta) + x_2^k \cdot \cos(\delta)) - 2 \cdot L_f \cdot \omega \cdot \cos(\delta) \cdot (x_1^{k2} + x_2^{k2}) \end{bmatrix} \end{aligned} \quad (27)$$

#### ➤ STEP 3

For the next step, the  $x_3^k$  and  $x_4^k$  values obtained from STEP 2 are used in STEP 1 to find  $x_1^{k+1}$ . By calculating  $x_1^{k+1}$ , the  $x_3^{k+1}$  and  $x_4^{k+1}$  values are computed by (27) according to STEP 2. This recursive process is continuously performed in each step, and the current references of (25) are updated correspondingly.

It is worth noting that the proposed current reference generation method is real-time, which takes the inputs and accordingly produces the proper current references under both balanced and unbalanced conditions. Under the balanced condition, according to (27), the resulting current references are also balanced since  $V_2 = 0$ . Following upon an occurrence of an unbalanced condition,  $V_2$  will take non-zero value, and then, the proposed method automatically updates the current references in a real-time scheme. Fig. 2 graphically represents the proposed procedure for obtaining the proposed current references.

#### B. Modified Current Controller:

As (25) shows, the derived current references have pulsating components in addition to a constant component. Then, the

controller should have a large gain for this pulsating component as well as for the constant component. To ensure this, the following modified compensator is suggested:

$$C_i(s) = \frac{1}{\tau} \cdot \frac{L_f \cdot s + R_f}{s} \cdot \frac{s^2 + 2\xi \cdot (2\omega_0) \cdot s + (2\omega_0)^2}{s^2 + (2\omega_0)^2} \quad (28)$$

where the gain  $1/\tau$  demonstrates the bandwidth of the current controller.

This compensator has an integrator, which ensures a zero steady-state error in tracking the constant component of the current references. Also, another resonant term is employed to ensure a zero steady-state error for the components with the frequency of  $2\omega_0$ . Finally, to improve the transient behavior of the current control loop, a zero at the value of the input filter pole ( $s = -(R_f + r_{on})/L_f$ ) is also added to this compensator.

Under unbalanced conditions, the input signal of the PLL ( $V_{sq}$ ) has  $2\omega_0$  term ripples, which may degrade the PLL operation and the synchronization process. In order to solve this problem, a modified PLL compensator is used as [18]:

$$C_{PLL} = k_1 \cdot \frac{s+z}{s} \cdot \frac{s^2 + (2\omega_0)^2}{s^2 + 2\xi \cdot (2\omega_0) \cdot s + (2\omega_0)^2} \quad (29)$$

where  $k_1$  and  $z$  are the compensator gain and zero, respectively.

This compensator has a mid-reject characteristic in the frequency of  $2\omega_0$ . Therefore, the negative sequence components with a pulsating nature at the frequency of  $2\omega_0$  will be removed. A pole at  $s = 0$  is also added to ensure a zero steady-state error in finding the synchronous angle. Moreover, to improve the frequency and time-domain characteristics of the PLL loop, a zero at  $s=-z$  has also been added.

## VI. SIMULATION RESULTS

This section examines the functionality of the proposed method. The test system of Fig. 1 is simulated, which consists of a 20 kV AC grid with its Thevenin equivalent, a 20/5 kV 16 MVA transformer ( $\Delta$ - $\Delta$  connection) with 5% leakage reactance and a 16 MVA converter that regulates the DC link voltage. The DC link voltage is selected 10 kV, and a total load of the DC grid is 10 MW (two 5 MW loads). It is further assumed that the AC grid is an unbalanced network with  $V^-/V^+$  ratio of 6%.

The modified and conventional PLL compensators are given in (30) and (31), respectively.

$$C_{PLL} = \frac{0.06 \times s + 2.21}{s} \cdot \frac{s^2 + (2\pi \times 100)^2}{s^2 + 1538 \times s + (2\pi \times 100)^2} \quad (30)$$

$$C_{PLL} = \frac{0.07 \times s + 5.17}{s} \quad (31)$$

The converter parameters are shown in Table I.

Also, the current controller and the DC link voltage controllers are:

$$C_i = \frac{2.19 \times s + 6.25}{s} \cdot \frac{s^2 + 620 \times s + (2\pi \times 100)^2}{s^2 + (2\pi \times 100)^2} \quad (32)$$

$$C_v = \frac{96 \times s + 3000}{s} \quad (33)$$

The AC grid is simulated with its Thevenin model with an equivalent impedance of  $0.8 \Omega$  and the voltage values of (in kV):

$$V_a = 11.55 \angle 0, V_b = 10.43 \angle -118, V_c = 12.36 \angle 122.$$

To show the performance of the proposed scheme, different scenarios are considered for the test system of Fig. 1, and it is compared with that of the existing method in the literature. The compared existing method works based on removing double frequency oscillations from instantaneous active power in the grid connection point. This method improves the converter performance under unbalanced conditions compared to the conventional method described in Section II. However, the input filter inductance effect has not been included.

### A. Evaluation of the PLL response

In this part, the operation of the conventional and modified PLL compensators are compared. Assume that the converter has been connected to the AC grid, and the grid voltages are unbalanced with an imbalance ratio of 6%. A temporary single line to ground (SLG) fault in the location shown in Fig. 1 with  $R_{\text{fault}} = 1 \Omega$  occurs at  $t=1.5$  sec. The stationary “*abc*” and the grid-voltage



oriented synchronous “dq” reference frames voltage waveforms in the converter side of the transformer are depicted in Fig. 3 (a) and (b), respectively. As shown in the figure, due to the delta connection of the transformer, the effect of an SLG fault in grid side of the transformer appears in other two phases in the converter side of the transformer. The output frequencies of the conventional and modified PLLs are depicted in Fig. 4. As shown in the figure, the conventional PLL finds the frequency of the AC grid with 5% ripple when the grid is unbalanced. However, during the fault, the frequency oscillates in a larger range, and then it adversely affects the power converter functionality. On the other hand, the modified PLL tracks the frequency of the AC grid with negligible ripple in both normal and faulty conditions. To provide a fair comparison in the following subsections, the modified PLL is employed for both proposed and existing methods.

### B. Operation under Unbalanced Condition

To investigate the steady-state operation of the proposed method, two 5 MW load step changes at times 0.75 sec and 1 sec are applied at the DC side of the power converter. The grid voltages are unbalanced with an imbalance ratio of 6%, which are shown in Fig. 5 (a). The DC link voltage waveforms for both the existing and proposed methods are depicted in Fig. 5 (b). As shown in this figure, there are oscillations ( $2\omega_0$  components) with a small amplitude (2.5 %) in the response of the existing method, which is allowed from the standard limits perspective. On the other hand, the proposed method has effectively eliminated these ripples.

### C. Operation under Moderate Short Circuit Faults

A single-line-to-ground (SLG) fault with  $R_{\text{fault}}=1 \Omega$  occurs in the grid side of the transformer at  $t=1.5$  sec. Fig. 6 (a) shows the power converter input voltages in which two phases “a” and “b” are affected by the fault due to the delta connection of the transformer. Fig. 6 (b) demonstrates the response of the proposed and the existing methods. As it was expected, the ripples on the DC side voltage is increased if the existing method is used, but it is eliminated by the proposed method.

### D. Operation under Severe Short Circuit Fault

In this part, a severe SLG fault with  $R_{\text{fault}}=0.1 \Omega$  is applied to the system at 1.5 sec. This fault extremely decreases the phase voltage at the grid side of the transformer. The converter side voltage of the transformer and the DC link voltages with the existing and proposed methods are presented in Fig. 7 (a) and (b), respectively. As it can be seen from this figure, there are pulsating voltage ripples with large amplitude when the existing control is employed, while the proposed method effectively eliminates these ripples. This large value of oscillation creates over-voltage on the DC link voltage, which may unnecessarily trigger the DC side over-voltage protection even under temporary short circuit faults with a small duration (of few hundreds of milliseconds).

The input currents are depicted in Fig. 7 (c) and (d) for the proposed and existing schemes, respectively. As shown in Fig. 7 (d), ignoring the impact of the filter inductance in the control scheme of the existing method results in current references with large amplitude. However, considering the filter inductance in the proposed control scheme considerably improves the current references and correspondingly the actual currents, as shown in Fig. 7 (c). This is also an important subject from a power converter over-current protection point of view. Power converters are protected against over-currents by means of current limiter incorporated into the current control scheme. The current limiter instantaneously applies a limit to output current, and in the case of an overload or a short circuit fault, limits the output current amplitude. In such circumstances, the DC link controller cannot maintain the control task, and the power converter should be tripped. According to the results of Fig. 7 (c)-(d), using the existing control scheme may result in activation of the current limiter, which is avoided by employing the proposed scheme. Therefore, using the proposed method not only avoids any unnecessary disconnection of the power converter due to the double frequency ripples in DC link voltage, but it also improves the power quality of the input currents drawn from the grid.

To further analyze the proposed real-time recursive method, the variations of the variables  $x_1$ ,  $x_2$ ,  $x_3$ , and  $x_4$  are depicted in Fig. 8. As shown in Fig. 8 (a), by applying the fault at  $t=1.5$  sec, the positive sequence voltage decreases from 4 kV to 2.78 kV, and the negative sequence voltage increases from 0.25 kV to 1.17 kV, which shows a severe unbalanced condition. As mentioned earlier, before the fault occurrence, the grid is unbalanced with an imbalance ratio of 6 % (i.e.,  $0.25/4=0.06$ ), and it increases to 42 % ( $1.17/2.78=0.42$ ) when the fault occurs. By occurring the fault, the proposed method automatically updates the  $x_1$ ,  $x_2$ ,  $x_3$ , and  $x_4$  values to find the proper current references as it works in real-time with a closed-loop manner. The variations of  $x_1$ ,  $x_2$ ,  $x_3$ , and  $x_4$  are depicted in Figs. 8 (b)-(e), respectively. As shown in these figures, when the fault occurs, the values are changed from previous steady-state values (unbalanced condition) to the new steady-state values (short circuit condition). As it can be seen from the results, the proposed method does not need any fault occurrence detection strategy, since the values are updated real-time in a closed-loop system as described in Fig. 2.

## VII. CONCLUSION

This paper improves the performance of the power converters by reducing the pulsating ( $2\omega_0$ ) ripples in the DC link voltage under unbalanced input voltage condition. This performance improvement becomes more essential in medium/high power applications in which the switching frequency is low, and the effect of the input filter cannot be neglected. In this paper, the

problem is analytically formulated considering the input filter inductance. Then, a recursive approach is proposed for solving the related nonlinear equations to determine the proper current references. Also, in order to ensure current reference tracking with a sinusoidal reference, the compensator performance is improved by adding a resonant transfer function with a mid-pass filter characteristic. The performance of the proposed method is examined using different time domain simulations in the PSCAD/EMTDC environment. The results indicate that with the changes made in the control system and determining proper current references, the performance of the overall system in removing the pulsating terms from the DC-link and the instantaneous output power is enhanced compared to the results of existing approach as in the literature.

## VIII. ACKNOWLEDGMENT

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**Fig. 8.** The variations on the waveforms of  $V_1$  and  $V_2$  and calculated values of  $x_1$ ,  $x_2$ ,  $x_3$ , and  $x_4$  when a severe single-line-to-ground fault with  $R_{\text{fault}} = 0.1 \Omega$  occurs at the grid side of the transformer at  $t = 1.5$  sec., (a)  $V_1$  and  $V_2$  variations, (b)  $x_1$  variation, (c)  $x_2$  variation, (d)  $x_3$  variation, (e)  $x_4$  variation.

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**Table I.** converter parameters

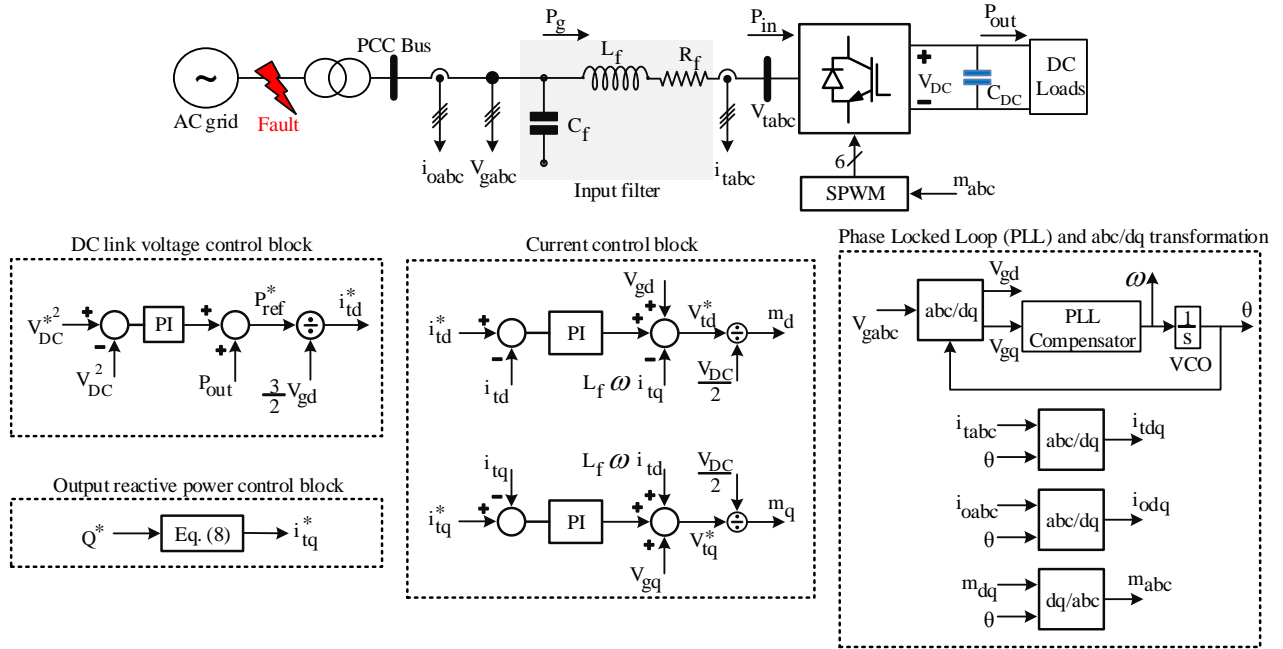


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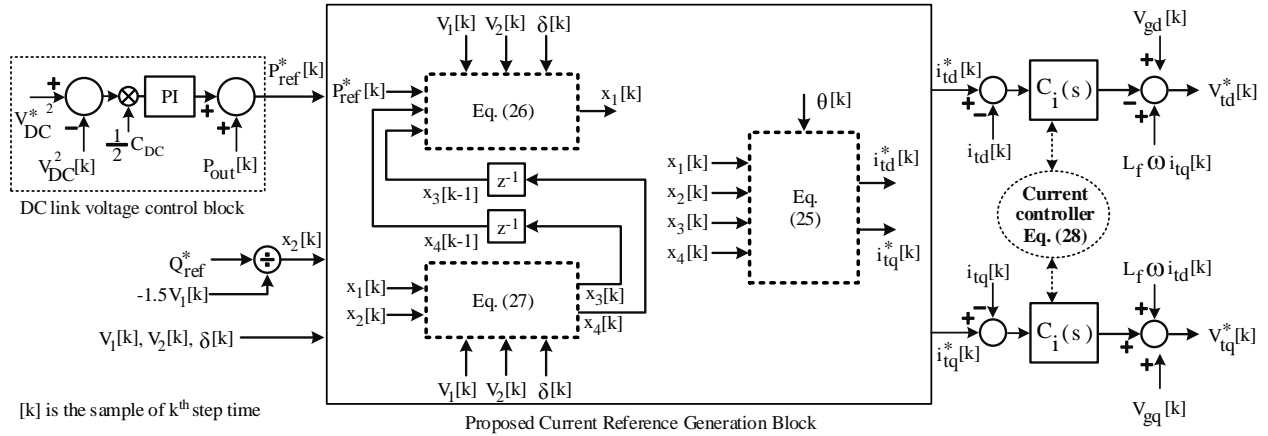


Fig. 2. The converter control structure considering the proposed current references for the removal of double frequency ripples from DC-link voltage.

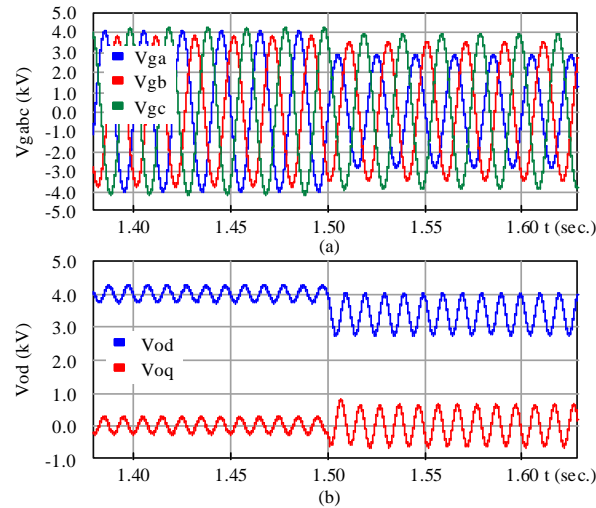


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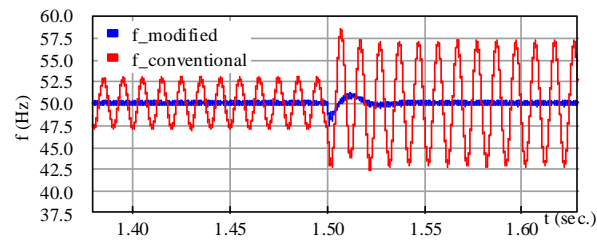


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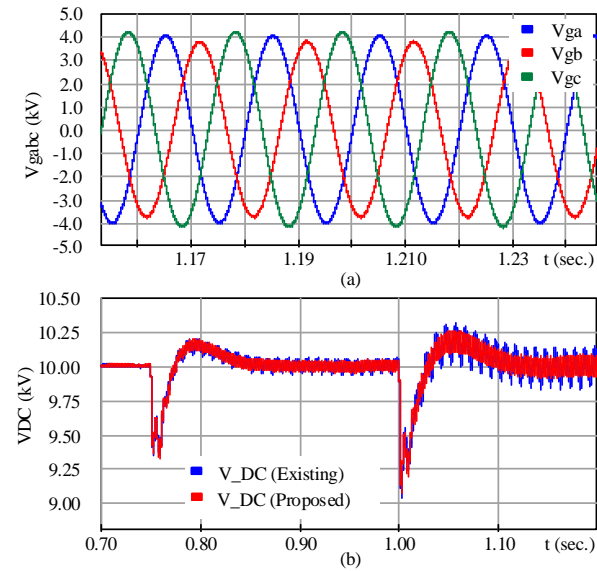


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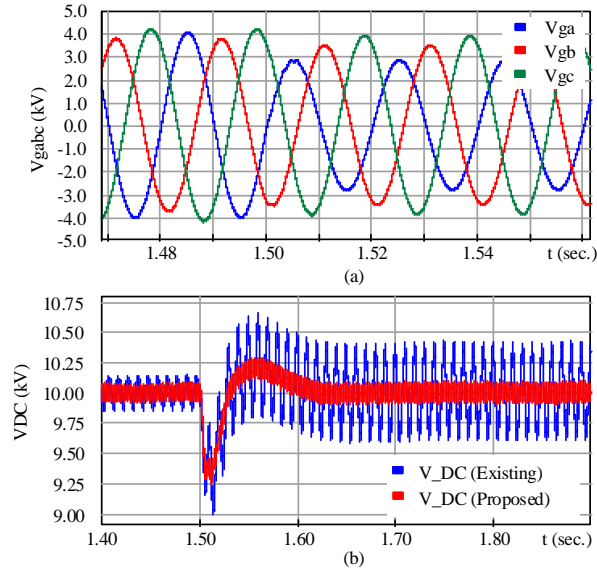


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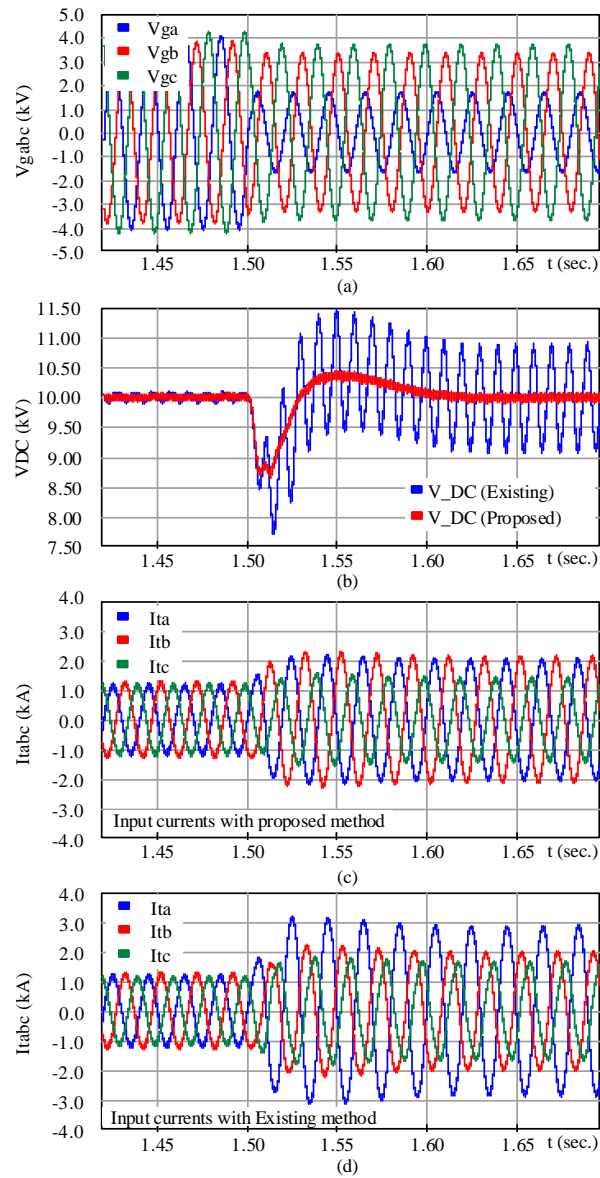


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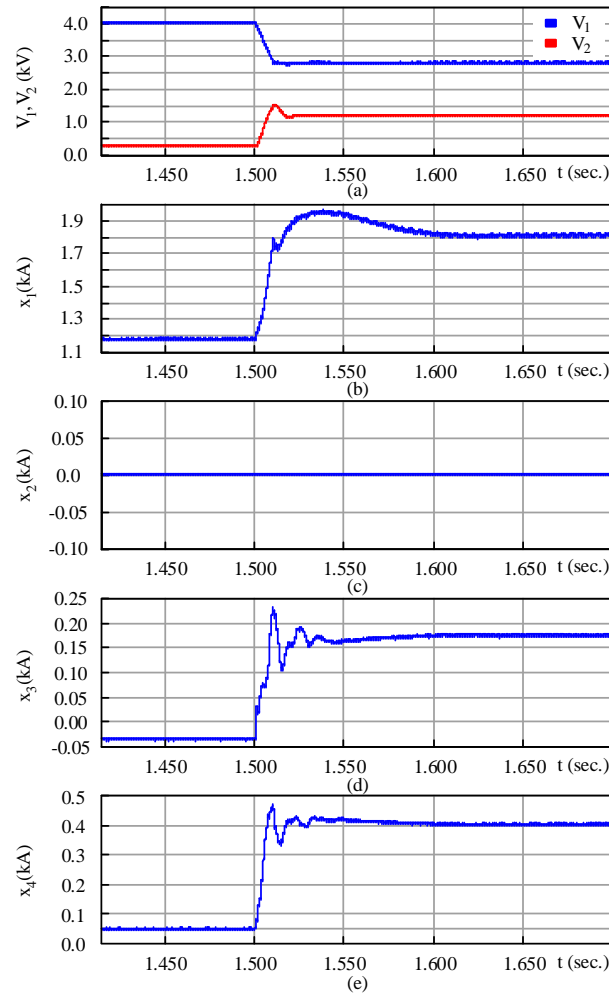


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TABLE I. CONVERTER PARAMETERS

Parameter	Value	Parameter	Value
$R_f$	$0.01 \Omega$	$C_{DC}$	$1000 \mu\text{F}$
$L_f$	$3.5 \text{ mH}$	$f_{sw}$	$2 \text{ kHz}$
$C_f$	$250 \mu\text{F}$	DC Load	$10 \text{ MW}$

### **Biographies:**

**Seyed Fariborz Zarei** received the B.Sc. degree in electrical engineering from Amirkabir University of Technology, Tehran, Iran, in 2012 and the M.Sc. degree in electrical engineering from the Sharif University of Technology (SUT), Tehran, in 2014, where he is currently pursuing the Ph.D. degree in electrical engineering. His fields of interest include control and protection of microgrids and renewable energy sources.

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From 1989 to 1992, he worked in the Consulting Division of Power Systems Dispatching Projects, Electric Power Research Center Institute, Tehran. Since 2000, he has been with the Department of Electrical Engineering, Sharif University of Technology, Tehran, where he is currently a Professor. He is also a Senior Consultant to several utilities and industries.

**Frede Blaabjerg** (S'86–M'88–SM'97–F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications.

He has received 29 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2018 he is President Elect of IEEE Power Electronics Society. He serves as Vice-President of the Danish Academy of Technical Sciences. He is nominated in 2014, 2015, 2016 and 2017 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.



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