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0.3 V tunable OTA and Gm-C filter in 0.13 μm CMOS

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Tunable.

Abstract. This study presents an ultra-low-voltage Operational Transconductance Amplifier (OTA) and Gm-C filter, both operating with a single supply voltage of 0.3 V. Using the pseudo-differential structure, the common mode rejection is the main challenge in the low-voltage condition and it is resolved by a new common mode feedback circuit. OTA can be tuned through the gate terminal of body-driven PMOS input transistors. Post-layout simulation showed 23.4 dB differential gain and 47.4 dB CMRR at low frequencies. By changing the tune voltage from 50 mV to 0 V, the transconductance of OTA could be tuned from 7.9 to 17.4 μA/V. By applying input voltages up to 0.36 Vpp, the Total Harmonic Distortion (THD) of the output current remained less than –60 dB. The proposed OTA was employed to implement a tunable low-pass Gm-C filter. The cut-off frequency of Gm-C filter could be tuned from 1.13 to 1.9 MHz, making it applicable to multi-standard direct conversion receivers as the channel selection filter. According to the results of post-layout simulations, the power consumption of the filter and its input-referred voltage noise were 111.3 μW and 168.7 nV/$\sqrt{\text{Hz}}$, respectively. The post-layout simulation showed the IIP3 with 8.5 dBm at a cutoff frequency of 1.9 MHz.

1. Introduction

Using low-voltage small batteries with a longer charge-discharge cycle is essential for portable devices such as cell phones, laptops, medical equipment, etc. [1–5]. Moreover, modern systems fabricated by deep sub-micron CMOS technologies must be designed such that they operate with low supply voltage due to the reliability issues regarding a layer of thinner gate oxide in transistors [3,6,7]. Operational Transconductance Amplifier (OTA) is a key building block of the analog parts of numerous circuits and systems [8–10]. The performance of OTA directly determines the overall performance of analog front-end parts of receivers such as Voltage-Controlled Oscillators (VCO), Gm-C filters, variable gain amplifiers, and mixers [11].

Utilization of weakly inverted devices, body biased transistors, charge pump methods, floating gate transistors, and pseudo-differential non-cascode structures are the main low-voltage design techniques [6,12]. However, the aforementioned techniques either degrade the performance of the circuit or prevent the designers from employing special technologies. While the subthreshold operation of devices slows down the circuit and increases the area usage on chip, the body-driven devices suffer from poor transconductance and large input capacitance [3,13–15]. The charge pump technique may be subject to reliability problems in some cases, and a low-voltage design using floating gate transistors is possible only with double poly technologies [6,16].

The channel selection filter is a significant building block of multi-standard direct conversion receivers

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and it is responsible for rejecting unwanted signals from the desired channel. The Gm-C structure is frequently used to implement the channel selection filter as it makes low-power and high-frequency operation. However, compared to their active-RC counterparts, the Gm-C filters suffer from poor linearity due to the open-loop operation of Gm cells [17,18]. Thus, OTAs that are used in Gm-C filters should be designed to have high linearity and wide tunability, both of which are hardly achievable under low-voltage conditions.

In this study, a 0.3 V single supply voltage OTA was designed, benefiting from low-power highly linear operation and tuning capability. OTA comprises a body-driven pseudo-differential-based transconductor core and a novel Common-Mode Feedback (CMFB) circuit. Through the body-driven technique, CMFB circuit senses the common-mode voltage of output nodes and returns two feedback voltages to the bias network of transconductor in order to effectively stabilize the common-mode voltage of output nodes. OTA was also employed to implement a tunable linear Gm-C filter. The cutoff frequency of the proposed Gm-C filter was tunable within the range of 1.13 to 1.9 MHz; thus, it was utilized in the multi-standard direct conversion receivers. The results obtained from the Monte Carlo simulation showed the robustness of the proposed circuits against the fabrication errors, and the outcome of the post-layout simulation pointed to good performance after the appearance of parasitic effects.

The rest of this paper is organized as follows. In Section 2, the subthreshold operation of the body-driven Metal-Oxide-Semiconductor (MOS) transistor is investigated. In Section 3, the proposed OTA and its physical layout are presented. The low-pass Gm-C filter design is presented in Section 4. The simulation results are shown in Section 5. Finally, Section 6 concludes the paper.

2. Subthreshold operation of a body-driven MOS transistor

When the gate-source voltage of an MOS transistor drops below its threshold voltage, the channel becomes weakly 0 and the diffusion current flows from drain to source. In low-voltage designs in which the supply voltage is lower than the threshold voltage of transistors, the transistors inevitably work in the "subthreshold region". The I/V characteristic of the subthreshold-mode transistor is given as follows [19]:

$$i_{DS} = I_S\left(\frac{W}{L}\right)exp\left(q\frac{v_{GS}-v_{TH}}{nkT}\right)\left[1-exp\left(-q\frac{v_{DS}}{kT}\right)\right], \quad (1)$$

where I_S is the characteristic current that depends on the technological parameters, n is the weak inversion slope, k is Boltzmann constant, q is the charge of electron, T is temperature, and other parameters keep their common signification. The gate and body transconductance g_m and g_{mb} are respectively obtained as follows [19]:

$$g_m = \frac{\partial i_{DS}}{\partial v_{GS}} = \frac{I_{DS}}{nv_t}, \quad (2)$$

and:

$$g_{mb} = \frac{\partial i_{DS}}{\partial v_{BS}} = \frac{\gamma}{2\sqrt{2\phi_F + V_{SB_{NMOS}}}}g_m, \quad (3)$$

where I_{DS} is the dc operating point current, v_t is the thermal voltage of 26 mV at room temperature, γ is the body effect coefficient, ϕ_F is the Fermi potential, and V_{SB} is the dc value of source-body voltage. The latter relation shows that g_{mb} increases at higher currents and lower values of V_{SB}. The drain-source small-signal resistance is directly proportional to the length and inversely to the current ($\sqrt{r_{ds}} \propto L/I_{DS}$); thus, the intrinsic gain of the transistor is proportional to $L/\sqrt{I_{DS}}$.

Since the proposed 0.3 V OTA is based on body-driven transistors, the transconductance g_{mb}, drain-source resistance r_{ds}, and intrinsic gain ($g_{mb} \times r_{ds}$) are evaluated using 0.13 μm CMOS technology at a constant aspect ratio of 100 and different transistor lengths. Through test circuits in Figure 1, g_{mb} and r_{ds} were simulated at four transistor lengths of 0.13, 0.5, 1, and 2 μm. The results including the intrinsic gain are shown in Figure 2. According to Eq. (1), the current depends only on the aspect ratio; however, according to the simulation results, it is significantly reduced at length values close to the minimum feature size due to the second-order effects. Hence, g_{mb} in the case of $L = 0.13$ μm is much lower than that at other lengths. Except for r_{ds} in $L = 0.13$ μm which is higher than that in $L = 0.5$ μm due to the lower current in the former one, the drain-source resistance increases when the transistor length increases. The intrinsic gain $g_{mb} \times r_{ds}$ accordingly is higher at larger length values of the transistor.

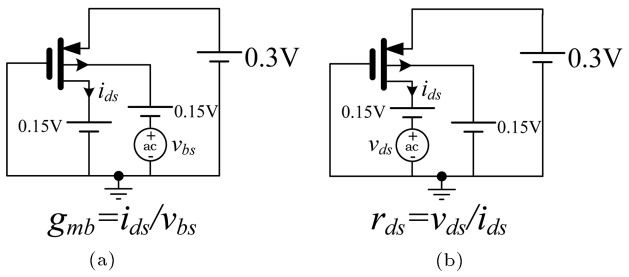

Figure 1. Test circuits for simulation of (a) g_{mb} and (b) r_{ds}.

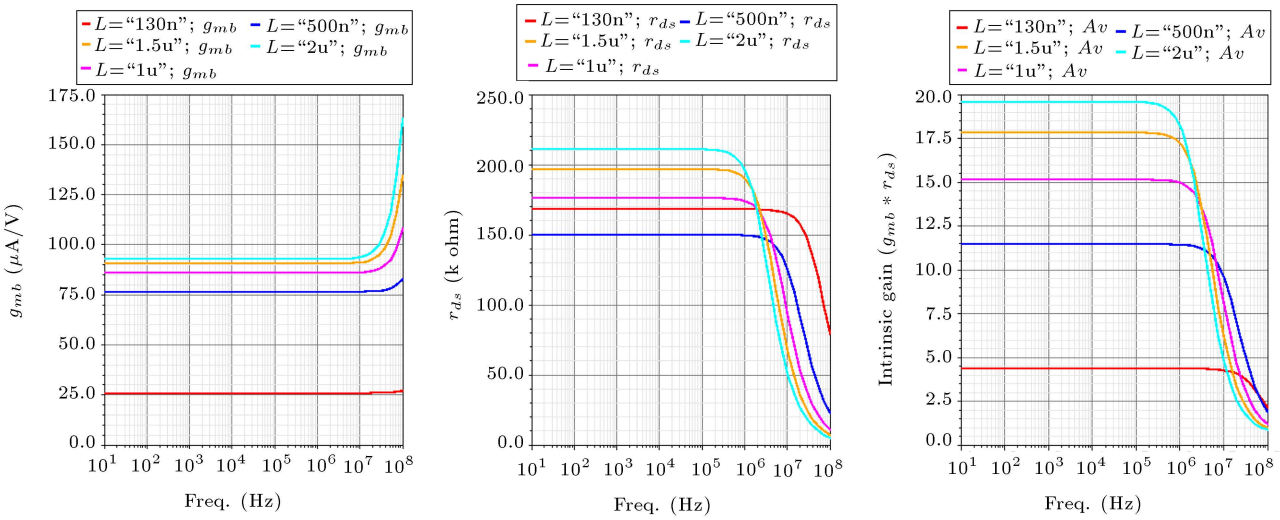

Figure 2. g_{mb}, r_{ds}, and intrinsic gain ($g_{mb} \times r_{ds}$) for PMOS transistor operating at 0.3 V with four length values.

3. Proposed 0.3 V OTA

3.1. OTA schematic

The proposed low-voltage OTA is shown in Figure 3. The transconductor core is composed of transistors M1 to M4 and the CMFB circuit is composed of M5 to M14. Using NWell technology, the input voltages are applied to the body terminals of PMOS transistors M1 and M2. In such a low-voltage condition, the body-driven technique seems to be the only solution for achieving a rail-to-rail linear operation. The output nodes are connected to the body terminals of M5 and M6, whose common drain node senses the common-mode voltage of output nodes. To effectively suppress the output CM voltage variations, the CM feedback is applied in two directions. First, the feedback voltage at node "cf1" is applied to the body terminals of M13 and M14. In the body-driven source follower stage, the second feedback voltage is made at node "cf2" and applied to the gates M3 and M4. In this regard, the output CM voltage would be stabilized at 0.15 V, equal to half of the supply voltage. The variation of output CM voltage resulting from either the input CM voltage variation or fabrication errors would be compensated by the CMFB circuit action. For instance, when the output CM voltage is more than 0.15 V, the voltages of nodes "cf1" and "cf2" increase proportionally. Consequently, the currents of M13 and M14 and those of M3 and M4 would decrease and increase, respectively, to return the output CM voltage to 0.15 V.

3.2. Differential and common mode gains

The differential gain can be obtained as follows:

$$A_d = -g_{mb_{1,2}} R_{out}, \tag{4}$$

where $R_{out} = r_{ds1}||r_{ds3}||r_{ds13}$. To achieve a higher differential gain, the channel length of transistors M1 to M4 is set to 2 μm. Regarding two CM feedback paths, the CM gain can be obtained as follows:

$$A_c = \frac{-g_{mb_{1,2}} R_{out}}{1 + \left(g_{mb13,14} A_{cf1} + g_{m3,4} A_{cf2}\right) R_{out}}, \tag{5}$$

where A_{cf1} and A_{cf2} are the voltage gains from the output CM voltage to the feedback nodes "cf1" and "cf2" which are given as follows:

$$A_{cf1} = \frac{v_{cf1}}{v_{ocm}} = \frac{2g_{mb5,6}}{g_{ds7} + g_{m8}} \frac{g_{m9}}{g_{ds9} + g_{ds10}}, \tag{6}$$

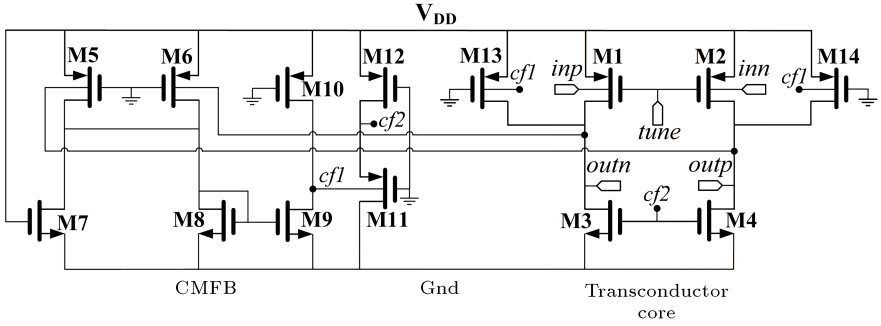

Figure 3. Proposed Operational Transconductance Amplifier (OTA).

Table 1. Aspect ratio of transistors.

Transistor	W/L (μm/μm)
M1,2	80/2
M3,4	200/2
M5,6	50/1
M7	60/0.5
M8	10/0.5
M9	90/2
M10	70/2
M11,12	30/0.5
M13,14	24/2

$$A_{cf2}=\frac{v_{cf2}}{v_{ocm}}=A_{cf1}\times\frac{g_{mb11}}{g_{mb11}+g_{m11}+g_{ds11}+g_{ds12}}. \quad (7)$$

To reduce the CM gain, the transistor M7 was incorporated into the CMFB circuit to decrease the current of M8 and g_{m8}, respectively. In addition, the length of transistors M9 and M10 was set to 2 μm to reduce g_{ds9} and g_{ds10}. The aspect ratio of the transistors of the proposed OTA is given in Table 1.

3.3. Linearity and tunability performance

The proposed OTA must include tunable transconductance so as to be applicable to tunable Gm-C filters. The tuning mechanism is fully achieved by applying the tuned voltage to the gate node of input transistors M1 and M2. According to Eqs. (2) and (3), voltage tuning changes the currents of M1 and M2 and consequently, changes $g_{m1,2}$ and $g_{mb1,2}$.

The first- to third-order coefficients of the power series that give the current of the body-driven subthreshold transistor as a function of its source-body voltage can be obtained by partial differentiating of Eq. (1), according to which the output current flowing into the load from "outp" to "outn":

$$i_{out}=\frac{1}{2}\frac{n-1}{n}\frac{I_D}{v_t}v_{in}+\frac{1}{8}\frac{I_D}{v_t^3}\frac{(n-1)^3}{6n^3}v_{in}^3. \quad (8)$$

The third-order harmonic distortion can be estimated as follows:

$$HD3=\frac{A^2}{96v_t^2}\left(\frac{\gamma}{\gamma+\sqrt{2\phi_F+V_{BS}}}\right)^2. \quad (9)$$

According to Eq. (9), at larger values of VBS, the HD3 is low and the output current is quite linear.

3.4. Noise performance

The thermal and flicker components of input-referred voltage noise can be obtained as follows:

$$\overline{v_{nth,in}^2}=\frac{8kT\gamma}{g_{mb1,2}^2}\Big(g_{m1,2}+g_{m3,4}+g_{m13,14}\Big), \quad (10)$$

$$\overline{v_{nf,in}^2}=\frac{2K}{C_{ox}g_{mb1,2}^2f}\Big(\frac{g_{m1,2}^2}{W_{1,2}L_{1,2}}+\frac{g_{m13,14}^2}{W_{13,14}L_{13,14}}+\frac{g_{m3,4}^2}{W_{3,4}L_{3,4}}\Big). \quad (11)$$

In Eq. (10), γ is the excess noise factor which is about $n/2$ in the subthreshold region. In Eq. (11), K is the process-dependent constant and f is the frequency. According to Eq. (10), thermal noise can be reduced by increasing the body-transconductance of M1-2. There is a trade-off between the differential gain/noise and the common-mode gain. The higher current for M1-2 and lower one for M13-14 would result in higher $g_{mb1,2}$, bringing about higher differential gain and lower thermal noise. However, this outcome also results in lower $g_{mb13,14}$ and consequently, higher common-mode gain regarding Eq. (5). As a compromise among the differential gain, noise, and common-mode gain, the ratio of M1-2 current to M13-14 is estimated as 10 to 3. However, according to Eq. (11), in case of flicker noise, this ratio can be minimized by enlarging transistors. For differential gain requirements, the sizes of transistors are sufficiently large with the flicker noise being negligible.

3.5. Physical layout of the proposed OTA

The layout of the proposed OTA, prepared with 1P8M 0.13 μm CMOS technology, is shown in Figure 4. The area usage is approximately 46 μm $\times$ 78.5 μm and two layers of metal are used for interconnections.

4. Gm-C filter design

The main features of the proposed OTA are ultra-low-voltage, high linearity, tuning capability, and high CMRR. However, as a significant building block, its applicability to larger circuits should be investigated. To this end, the proposed OTA was employed to implement a third-order low-pass Gm-C filter. The filter is shown in Figure 5, in which Gm3-6 utilized two floating inductors with the value of C_i/g_{m^2}. The capacitors C1 and C2 are set to 0.5pF and C3 and Ci are set to 0.2 and 0.6pF, respectively. Simulation results showed that the cutoff frequency of the filter could be tuned from 1.13 to 1.9 MHz by changing the tune voltage from 0 to 50 mV. The layout of the filter is shown in Figure 6 in which the MIMCAP has been used for all capacitors. The area usage of the filter is 247 μm $\times$ 155 μm.

5. Simulation results

5.1. OTA simulation results

The proposed OTA is post-layout simulated by 0.13 μm CMOS technology. At a single supply voltage of

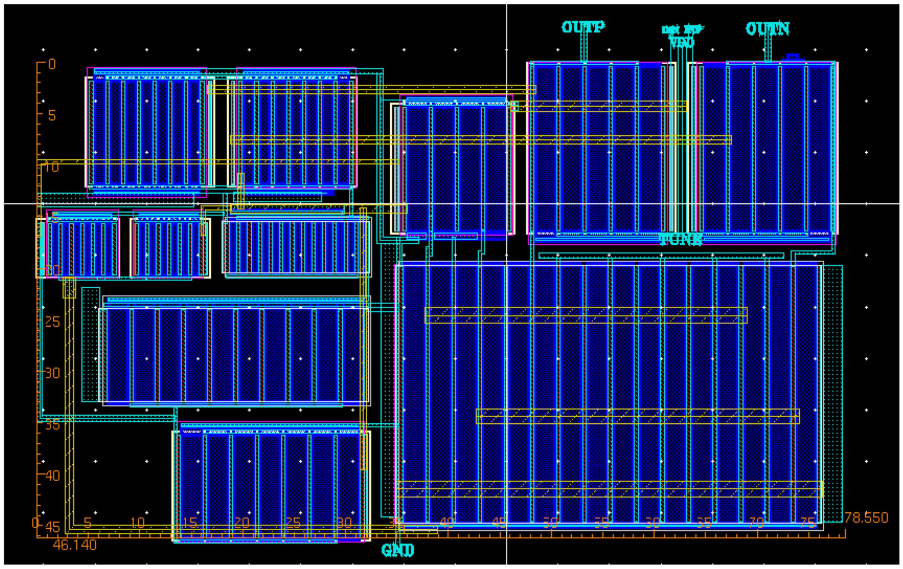

Figure 4. Layout of the proposed Operational Transconductance Amplifier (OTA).

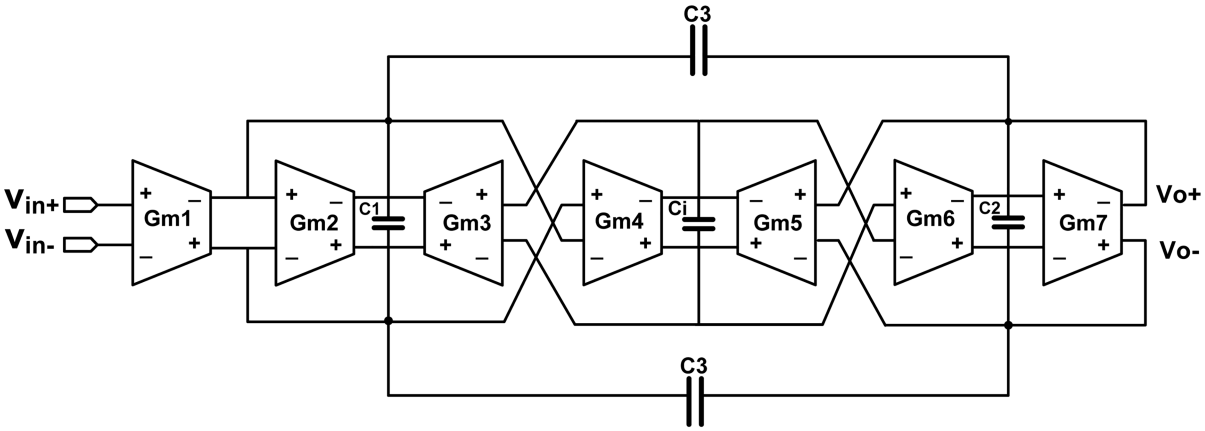

Figure 5. Third-order low-pass Gm-C filter.

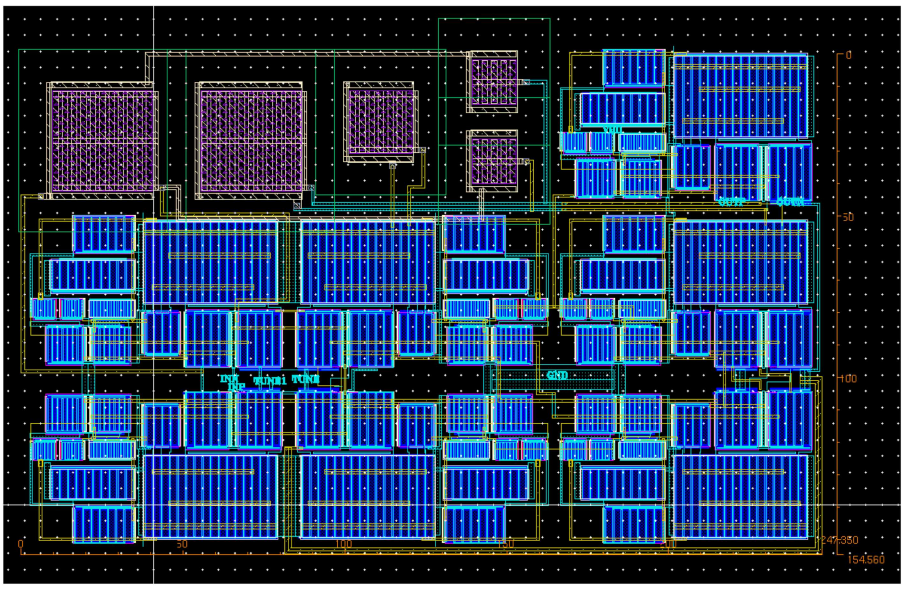

Figure 6. Physical layout of proposed third-order low-pass Gm-C filter.

0.3 V, the power consumption of OTA is 17.9 μW. The transconductance of the OTA was simulated versus the differential input voltage in six tuning conditions, the results of which are shown in Figure 7. According to the results, by changing the tune voltage from 50 mV to 0 V, G_m could be tuned from 7.9 to 17.4 μA/V. The flat curves up to about 0.3 Vpp input voltage show the high linearity of the proposed OTA for rail-to-rail input voltage.

By connecting 5pF capacitance load among the output terminals, the magnitude of the differential output voltage was simulated, as shown in Figure 8. The results showed that the gain and Unity Gain Bandwidth (UGBW) were 23.4 dB dc and 1.04 MHz, respectively. As shown in Figure 9, the voltage of the input-referred noise was 35.3 nV/p(Hz) at 100 kHz.

The Total Harmonic Distortion (THD) of the output current of OTA was simulated for various input voltage amplitudes, the results of which are shown in Figure 10. The THD values are lower than –58 dB for input voltages up to 0.4 Vpp. The post-layout simulation results are summarized in Table 2.

To evaluate the performance of the proposed OTA against the fabrication errors, the Monte Carlo simulations were performed on the main features of OTA in the standard process and mismatch errors. By applying a 0.2 Vpp input voltage at 100 kHz to the OTA which was already tuned at the highest transconductance, the THD of output current was simulated 100 times and the histogram plot of results is shown in Figure 11.

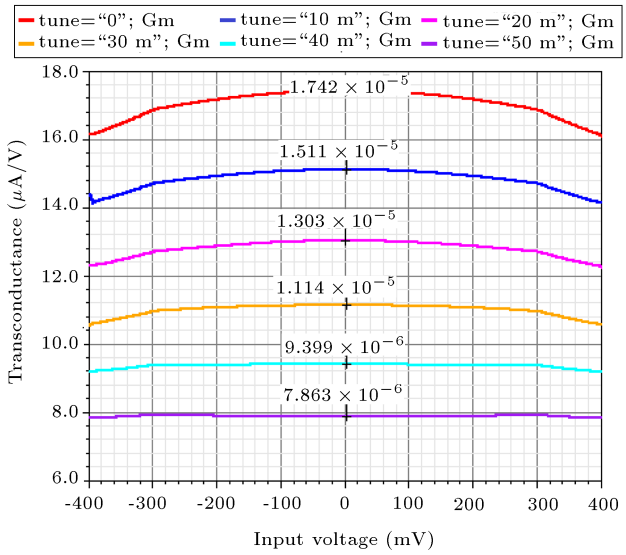

Figure 7. Post-layout simulation of transconductance versus differential input voltage.

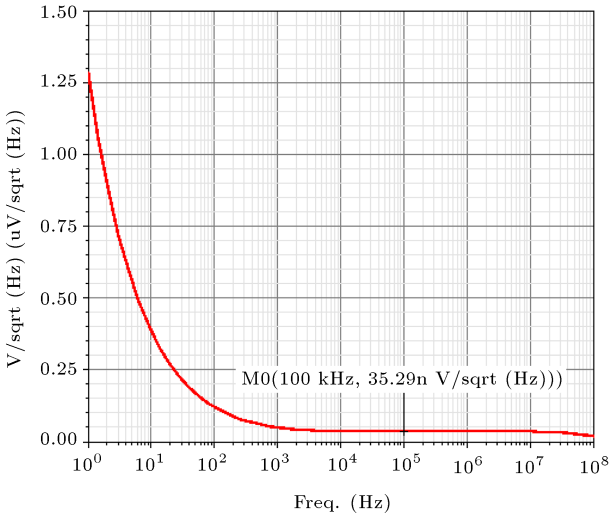

Figure 9. Post-layout simulation of input referred voltage noise.

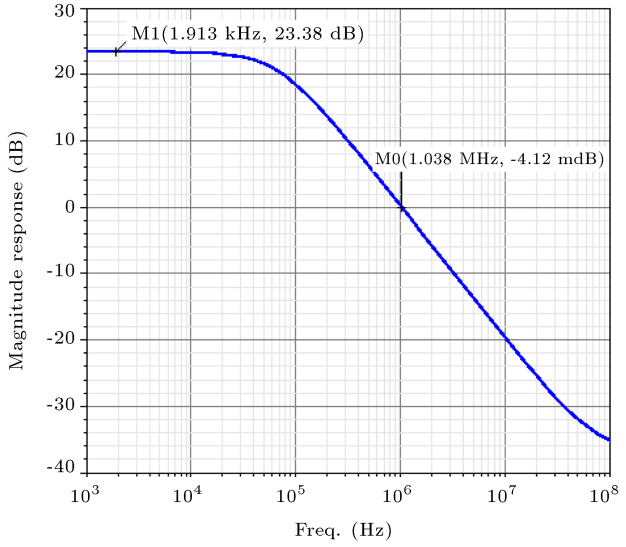

Figure 8. Post-layout simulation of magnitude of differential output voltage.

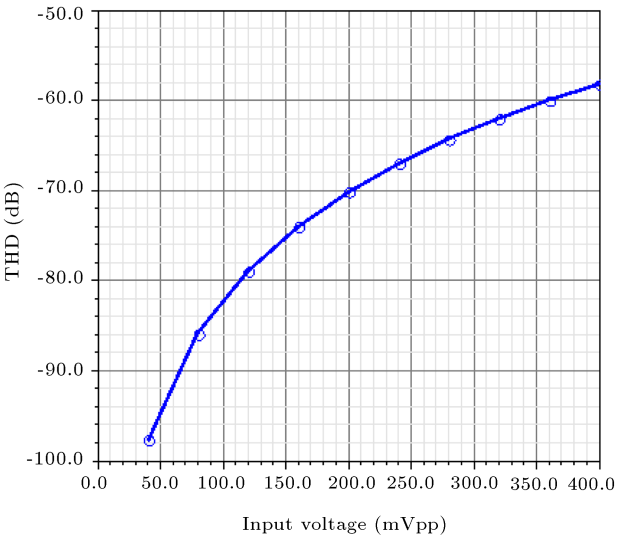

Figure 10. Post-layout simulation of Total Harmonic Distortion (THD) of OTA's output current.

Table 2. Simulation results of proposed Operational Transconductance Amplifier (OTA).

Characteristic	Post-layout simulation results
Supply voltage (V)	0.3
Power consumption (μW)	17.9
Transconductance ($\mu A/V$)	7.9-17.4
DC gain (dB)	23.4
Unity gain bandwidth (MHz)	1.04
Phase margin (degree)	97.4
Load capacitance (pF)	5
CMRR (dB)	47.4
Input referred voltage noise ($nV/\sqrt{(Hz)}$) @100 kHz	35.3
THD (dB) for 0.2 Vpp input voltage @ 100 kHz	–70.1

Table 3. Monte Carlo simulation results for 100 runs.

Characteristic	Mean	Standard deviation
DC differential gain	19.8 dB	5.7 dB
Unity gain bandwidth	1.04 MHz	173 kHz
DC common mode gain	–23.9 dB	4.47 dB
CMRR	40.7 dB	7.68 dB

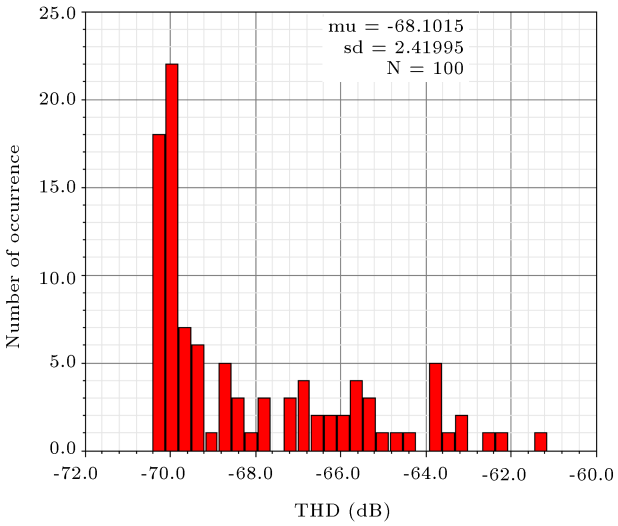

Figure 11. Monte Carlo simulation results of OTA's Total Harmonic Distortion (THD).

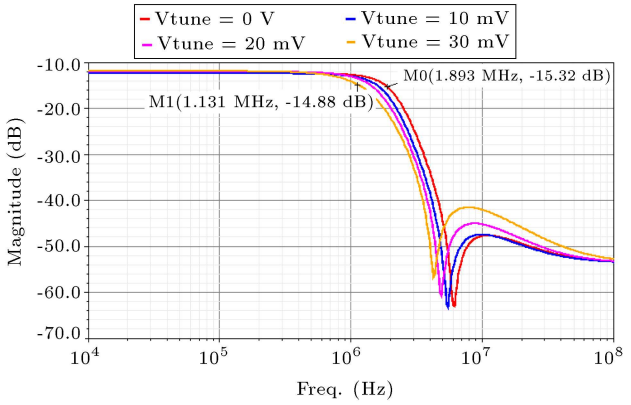

Figure 12. Post-layout simulation of magnitude response of Gm-C filter.

The mean and the standard deviation of samples are –68 and 2.4 dB, respectively, showing the robustness of the circuit against the fabrication errors. The results of Monte Carlo simulation for DC gain, UGBW, common-mode gain, and CMRR are given in Table 3.

5.2. Gm-C filter simulation results

The results of the post-layout simulation of the magnitude response of Gm-C filter are shown in Figure 12. The tune voltage varied from 0 to 30 mV through which the cutoff frequency was tuned from 1.13 to 1.9 MHz. Due to the parasitic resistance effects, the pass-band gain was reduced in post-layout simulation. The main properties of the proposed filter are summarized in Table 4. The result of post-layout IIP3 simulation is shown in Figure 13. The IIP3 is simulated by applying a 100 kHz two-tone input voltage. For the cutoff frequency of 1.9 MHz, the IIP3 is as high as 8.5 dBm, which shows the high linearity of the filter.

5.3. Comparison with similar works

Table 5 compares the post-layout simulation results of the proposed OTA and several previously presented low-voltage designs. At a 0.3 V supply voltage, the proposed OTA achieves tuning capability, which makes it applicable to tunable circuits. Other advantages of the proposed OTA are low-power operation, high linearity, low noise performance, and high phase margin. As a compromise between the DC gain and linearity, DC gain is lessened to make OTA suitable for Gm-

Table 4. Main properties of the proposed Gm-C filter.

Characteristic	Post-layout simulation results
Supply voltage (V)	0.3
Power consumption (μW)	111.3
Cutoff frequency (MHz)	1.13–1.9
Input referred voltage noise (nV/$\sqrt{(\text{Hz})}$) @100 kHz	168.7
IIP3 (dBm) @ 100 kHz	8.5, Vtune=0 V, f_C=1.9 MHz –7.4, Vtune=30 mV, f_C=1.1 MHz

Table 5. The proposed Operational Transconductance Amplifier (OTA) post-layout simulation results compared with similar works in literatures.

Characteristic	This work	[12]	[12]	[14]	[6]	[3]
CMOS technology	0.13 μm	65 nm	65 nm	0.13 μm	0.18 μm	0.18 μm
Supply voltage (V)	0.3	0.35	0.5	0.25	0.5	0.5
Power consumption (μW)	17.9	17	182	0.018	110	60
Transconductance (μA/V)	7.9–17.4	-	-	-	Not tunable	-
DC gain (dB)	23.4	43	46	60	52	47.7
Unity gain bandwidth (MHz)	1.04	3.6	38	1.88 kHz	2.5	17.8
Phase margin (degree)	97.4	56	57	53	-	60
Load capacitance (pF)	5 (between output nodes)	3	3	15	20	20
CMRR (dB)	47.4	–	–	–	78	138
Input referred voltage noise (nV/$\sqrt{(\text{Hz})}$) @100 kHz	35.3	926	938	3.3 μV/$\sqrt{(\text{Hz})}$	80 @ 1 MHz	80 @ 1 MHz
THD	–70.1 dB for 0.2 Vpp input voltage @ 100 kHz	0.6%	0.4%	0.2%	1% at 0.4 Vpp output voltage	HD3=-42.4 dB for 820 mVpp diff. output voltage @2 MHz
Area usage (mm^2)	0.0036	0.005	0.005	0.083	0.026	–
FOM	24	0.26	0.27	0.46	0.35	26.4*

Note.* Area considered to be 0.0036 mm^2.

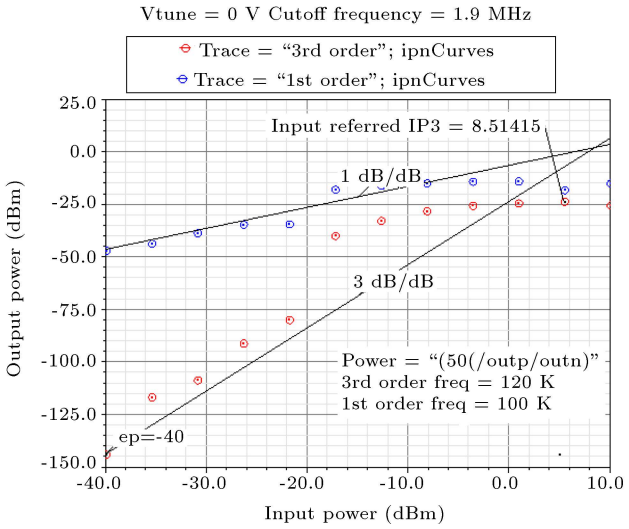

Figure 13. Post-layout simulation of filter's IIP3.

C filter applications. To consider the main features for comparison, a Figure Of Merit (FOM) was defined which comprised the dc gain, unity gain bandwidth, capacitance load at the numerator, the square of supply voltage, power consumption, distortion, noise, and area usage in the denominator. FOM values listed in Table 5 indicate that the proposed OTA exhibits state-of-the-art performance.

$$FOM = \frac{DC gain \times UGBW \times C_L}{V_{Supply}^2 \times Power \times \%distortion \times noise \times area}. \quad (12)$$

6. Conclusion

The present study aimed to propose a novel ultra-low-voltage OTA with 0.13 μm CMOS technology. According to the post-layout simulation results, the OTA operated at a 0.3 V supply voltage and consumed 17.9 μW. The core of the utilized transconductor was based on the body-driven pseudo-differential structure in which the transconductance could be tuned through the gate terminal of input PMOS transistors. Although the common mode rejection was a challenging task in such a low-voltage condition, the common mode feedback was efficiently applied in two directions such that the dc CMRR would increase up to 47.4 dB. By

changing the tune voltage from 0 to 50 mV, the OTA transconductance varied from 17.4 to 7.9 μA/V. By setting the input voltages to 0.36 Vpp, the rate of THD still remained below -60 dB. A third-order low-pass Gm-C filter was designed using the proposed OTA, consuming 111.3 μW at a 0.3 V supply voltage. The cutoff frequency of the filter was tunable from 1.13 to 1.9 MHz which made it suitable for multi-standard direct conversion receivers. The IIP3 of the filter was simulated to be 8.5 dBm at 1.9 MHz cut-off frequency.

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Biography

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