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A new boost converter-based soft switched active snubber cell for power factor correction

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KEYWORDS

Power factor correction; Hard switching; Soft switching; Active snubber cell; Zero voltage transition. **Abstract.** This paper introduces a new boost converter-based soft switched active snubber cell for power factor correction. In this particular converter, the main switch is turned on through Zero Voltage Transition (ZVT) and is turned off with the aid of Zero Voltage Switching (ZVS). The main diode is turned on using ZVS and is turned off using Zero Current Switching (ZCS). In the active snubber cell, the auxiliary switch is turned on by means of ZCS and is turned off using Zero Current Transition (ZCT). No semiconductor device is exposed to additional voltage stress. In this paper, theoretical analysis of the proposed converter is exhibited and validated by both simulation and experimental studies while operating at 100 kHz switching frequency and 600 W output power. It is demonstrated that the proposed converter is of 95.7% efficiency and 0.99 unit power factor in the soft-switching operation.

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1. Introduction

The use of electrical devices is gradually increasing and more energy is required with the developing technology. However, the available energy resources are dissipated rapidly. Hence, energy use should be more optimized in terms of efficiency and cost. It is widely known that national and international constraints and standards are being developed with an emphasis on Power Factor (PF) and harmonics for energy efficiency and quality. Diverse techniques including the so-called Power Factor Correction (PFC) are employed to provide the required efficiency and quality. Power factor can be corrected with a highly costly passive filter or an unduly costly and complex active filter. However, literature on this

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particular issue mainly focuses on high-frequency AC-DC converter-based PFC circuits that provide more advantages [1–4].

The aim of PFC is to bring near-zero reactive power and harmonic currents. These harmonic currents cause undesirable issues such as greater harmonic distortion, poor PF at AC input voltage and current. To achieve PFC, boost converters are usually beneficial in industrial applications [5–7]. This is mainly because ease of control and high power density are the desired attributes of AC-DC boost converters. To maintain these desired attributes, in principle, an AC-DC boost converter ought to be working with the highest possible frequency. However, increase in frequency induces a large number of switching losses and Electromagnetic Interface (EMI), exorbitant current and voltage stresses, declined efficiency, and impractical application scenarios [8–11]. To circumvent these problems, Soft Switching (SS) techniques are developed and replaced Hard Switching (HS) [12–25]. SS is realized using active or passive snubber cells that are added to the converter. Generally, if SS is achieved by passive snub-

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ber cells, this is called Zero Current Switching (ZCS) in the turning-on mode and Zero Voltage Switching (ZVS) in the turning-off mode. Besides, active snubber cells facilitating the development of SS represent Zero Voltage Transition (ZVT) in the turning-on mode and Zero Current Transition (ZCT) in the turning-off mode.

The SS converters can be categorized as magnetic and non-magnetic conductors according to the structure of the snubber cell. The converters containing non-magnetic snubber cell were proposed in [12–17]. A basic ZVT converter was presented in [12] and it achieved SS in the turning-on mode for the main switch. However, the main switch is turned off using HS in this unique converter. Therefore, the power switching losses cannot be prevented in this converter. In [13], the main switch was switched using SS, but there was additional current stress across the main switch and additional voltage stress across the auxiliary In [14], the entire semiconductors operated diode. using SS, where additional current stress occurred on both the main and auxiliary switches. Furthermore, an additional voltage stress occurred across the auxiliary diode. In [15], the main switch was turned on using ZVT and turned off by means of ZVS, whereas the auxiliary switch was turned on and off with the aid of ZCS. However, both switches were exposed to additional current stress and the main switch and diode were also exposed to additional voltage stresses. All semiconductors discussed in [16] operated based on SS techniques and it was confirmed that there was no additional stress in current or voltage across the main components. However, the operational conditions of SS are dependent on the amount of load and the performance of SS deteriorates at light loads. In [17], the main switch was turned on employing ZVT and turned on with the help of ZVS. The auxiliary switch was turned on and off using ZCS, but high current stress occurred in the auxiliary switch. An active power switch rather than the main diode was utilized in [18], where SS was achieved in the turning-on mode for all semiconductors. However, the main switch was turned off by HS. Hence, the power loss of the main switch could not be reduced in the turning-off mode. In [19], SS was achieved for switches, but there were extra elements in the main current path. This case led to additional conduction losses. In [20,21], SS was strictly dependent on the duty cycle and SS could not be achieved in the 0.5 duty cycle and additional current stress was exposed across the main switch in [21].

In [22], all semiconductors operated using SS techniques, in which there was no additional stress in current or voltage across the main elements. A converter with a magnetic snubber cell was proposed in [23–25]. A coupled inductor was used in the snubber cell in [23,24], which ensured ZVT turning-on, but parasitic oscillations arose due to leakage inductance.

In [25], the auxiliary transformer increased the cost of converter and the application of this converter was impractical.

In this treatise, a new boost converter-based active snubber cell for PFC was introduced in order to overcome the drawbacks of the above-mentioned soft switched converter. In this particular converter, the main switch and diode are turned on using ZVT and ZVS, respectively. Similarly, the turning off of the main switch and diode is attained by ZVS and ZCS, respectively. The auxiliary switch is turned on using ZCS, while its turning-off operation is attained by ZCT. Of note, semiconductor devices never experience voltage stress. The converter introduced can function with a wide range of voltage values and reduce EMI. Therefore, the proposed converter outperforms the conventional ZVT boost converter in terms of overall efficiency. Consequently, this new converter is capable of achieving less total harmonic distortion and a unit PF.

2. Operational principle and analysis

The converter suggested is delineated in Figure 1, where V_i defines the AC voltage source, V_O the output voltage, L_m the filter inductor, and C_m the filter capacitor, while D_m represents the main diode, S_m the main switch, and D_{Sm} the body diode, and R_L the output load. In this active snubber cell, S_a stands for the auxiliary switch, D_{Sa} its body diode, and D_a the auxiliary diode while C_S denotes the snubber capacitance. Finally, C_r and L_r represent the resonance capacitance and inductance, respectively.

To conduct a theoretical analysis, eight operational stages occur over one switching duration. Figure 2 shows the corresponding circuits of these operational stages, whereas the key wave shapes of the converter are portrayed in Figure 3.

Stage 1 $[t_0 < t < t_1: Figure 2(a)]$

When $t < t_0$, the voltage of C_S capacitor is identical to the output voltage and the input current flows through the main diode D_m . At $t = t_0$, a control signal is applied to the gate of S_a . Then, the current of D_m is reduced and the current of S_a concurrently increases. At $t = t_1$, the current of the main diode reduces to zero



Figure 1. The circuit design of the introduced Power Factor Correction (PFC) boost converter.



Figure 2. Corresponding circuit designs of the operational phases in the converter introduced: (a) Stage 1, (b) Stage 2, (c) Stage 3, (d) Stage 4, (e) Stage 5, (f) Stage 6, (g) Stage 7, and (h) Stage 8 [26].

and the current of S_a arrives at the input current. S_a is turned on and D_m is turned off using ZCS due to serially connected L_r . Thus, the reverse recovery current of the main diode is significantly reduced. The following equations can be derived for this particular case:

$$i_{Lr}(t) = \frac{V_o}{Z_1} \sin(\omega_1(t - t_0)),$$
(1)

$$v_{Cr}(t) = V_o - V_o \cos(\omega_1(t - t_0)),$$
(2)

$$Z_1 = \sqrt{\frac{L_r}{C_r}},\tag{3}$$

$$\omega_1 = \frac{1}{\sqrt{L_r C_r}}.\tag{4}$$

Stage 2 $[t_1 < t < t_2: Figure 2(b)]$

At $t = t_1$, a resonance initiates through $C_S - L_r - C_r$. The voltage of C_S is reduced while the current of L_r is increased in the sinusoidal form. If the voltage of C_S reaches zero, then this stage terminates. The equations derived for this stage are as follows:

$$i_{Lr}(t) = \frac{V_1}{Z_2} \sin(\omega_2(t - t_1)) + I_1 \cos(\omega_2(t - t_1)) - I_1 + I_{Lr}(t_1),$$
(5)



Figure 3. Corresponding key wave shapes for the operational stages in the converter introduced [26].

$$v_{Cr}(t) = \frac{I_{Lm}}{C_r + C_s} (t - t_1) + V_{Cr}(t_1)$$
 where $I_{Cr}(t_1) = \frac{C_{eq}}{C_r} [V_1 \cos(\omega_2(t - t_1)) - V_{Cr}(t_1)]$ where $V_{Cr}(t_1) = V_{Cr}(t_1) = V_{Cr}(t_1) + V_{Cr}(t_1) + V_{Cr}(t_1) = V_{Cr}(t_1) + V_{Cr}(t_1) = V_{Cr}(t_1) + V_{Cr}(t_1) + V_{Cr}(t_1) = V_{Cr}(t_1) + V_{Cr}(t_1) = V_{Cr}(t_1) + V_{Cr}(t_1) + V_{Cr}(t_1) = V_{Cr}(t_1) + V_{Cr}(t_1) + V_{Cr}(t_1) + V_{Cr}(t_1) = V_{Cr}(t_1) + V_{Cr}(t_1) +$

$$-I_1 Z_2 \sin(\omega_2(t-t_1)) - V_1], \qquad (6)$$

$$v_{Cs}(t) = \frac{I_{Lm}}{C_r + C_s} (t - t_1) + V_o$$

+ $\frac{C_{eq}}{C_s} [V_1 \cos(\omega_2 (t - t_1)))$
- $I_1 Z_2 \sin(\omega_2 (t - t_1)) - V_1],$ (7)

where:

$$I_1 = I_{Lr}(t_1) - \frac{C_{eq}}{C_s} I_{Lm},$$
(8)

$$V_1 = V_o - V_{Cr}(t_1), (9)$$

$$C_{eq} = \frac{C_r C_s}{C_r + C_s},\tag{10}$$

$$Z_2 = \sqrt{\frac{L_r}{C_{eq}}},\tag{11}$$

$$\omega_2 = \frac{1}{\sqrt{L_r}C_{eq}}.\tag{12}$$

Stage 3 $[t_2 < t < t_3: Figure 2(c)]$

At $t = t_2$, with the help of ZVS, the internal diode of D_{Sm} is turned on and this operation initiates this particular stage. If the body diode D_{Sm} is in the on-state, a gate signal provides the switch S_1 and, thus, the main switch is turned on using ZVT. Hence, the switching losses during the turning-on process are entirely diminished. If V_{Cr} reaches its affordable level, D_{Sm} is turned off and this stage terminates.

$$i_{Lr}(t) = I_2 \cos(\omega_1(t - t_2)) - \frac{V_2}{Z_1} \sin(\omega_1(t - t_2)), \quad (13)$$

$$v_{Cr}(t) = I_2 Z_1 \sin(\omega_1(t - t_2)) + V_2 \cos(\omega_1(t - t_2)),$$
(14)

where:

$$I_2 = \sqrt{\frac{L_r I_{L_r}^2(t_2) - C_r V_2^2}{L_r}},$$
(15)

$$V_2 = \frac{I_{Lm}}{C_r} (t_2 - t_1) + \frac{C_s}{C_r} V_o + V_{Cr}(t_1),$$
(16)

$$I_{Lr}(t_2) = \frac{\sqrt{V_1^2 + (I_1 Z_2^2)}}{Z_2} + \frac{C_{eq}}{C_s} I_{Lm}.$$
 (17)

Stage 4 $[t_3 < t < t_4: Figure 2(d)]$

At $t = t_3$, a resonance is commenced between L_r and C_r . The current of L_r increases immediately after the voltage of C_r is reduced in sinusoidal form. In this stage, the control signal of S_a is cut off and it is turned off by means of ZCT, while D_{Sa} is in its onstate. Hence, the power losses of S_a are fully eliminated during the turning-off process. V_{Cr} falls to zero, at which this stage terminates.

$$i_{Lr}(t) = -\frac{V_{Crpeak}}{Z_1}\sin(\omega_1(t-t_3)),$$
 (18)

$$i_{Lr}(t) = V_{Cr\text{peak}}\cos(\omega_1(t-t_3)), \tag{19}$$

$$i_{Sm} = I_{Lm} - i_{Lr}(t),$$
 (20)

where

$$V_{Cr\text{peak}} = \sqrt{\frac{L_r I_2^2(t_2) + C_r V_2^2(t_2)}{C_r}}.$$
 (21)

Stage 5 $[t_4 < t < t_5: Figure 2(e)]$

This particular stage is on-interval of the classical boost converter and the following equations can be derived for this stage:

$$i_{Lr}(t) = I_{Lr\text{peak}} = \frac{V_{Cr\text{peak}}}{Z_1},\tag{22}$$

$$i_{Sm} = I_{Lm} + I_{Lrpeak}.$$
(23)

Stage 6 $[t_5 < t < t_6: Figure 2(f)]$

At $t = t_5$, the gate signal of the main switch is cut off. So, it is turned off through ZVS owing to its parallel capacitor of C_S , which is recharged by $I_{Lm} + I_{Lrpeak}$. At $t = t_6$, V_{Cs} reaches V_O , which terminates this stage.

$$i_{Lr}(t) = i_{Lm} - (i_{Lm} + i_{Lrpeak})\cos(\omega_1(t - t_5)).$$
 (24)

Stage 7 $[t_6 < t < t_7: Figure 2(g)]$

At $t = t_6$, D_m is turned on using ZVS; therefore, this stage is initiated. The current of L_r inductance is linearly declined during this stage. At $t = t_7$, the current of L_r reaches zero and this stage terminates. For this stage, the following equations can be derived:

$$i_{Lr}(t) = I_{Lr\,\max} - \frac{V_o}{L_r}(t - t_6),$$
(25)

$$i_{Dm} = I_{Lm} + i_{Lr}(t).$$
 (26)

Stage 8 $[t_7 < t < t_8: Figure 2(h)]$

This stage is off-interval of the classical boost converter. At $t = t_8$, it returns to the beginning of the period immediately after a gate signal is provided for the auxiliary switch. The resulting equation can be obtained in this stage as follows:

$$i_{Dm} = I_{Lm}.$$
(27)

3. Design methods and soft SS

According to the assumptions made in the state-of-theart literature, the following design criteria are outlined in the converter introduced:

(a) The choice of snubber capacitor C_r : The duration of ZVT, depicted as t_{ZVT} , is crucial for SS at the time instant of the turning-on process. Hence, t_{ZVT} must be larger than t_r , namely rise time of S_m . The relationship between t_{ZVT} and snubber inductance L_r for various snubber capacitance C_r values is given in Figure 4.



Figure 4. The relationship between t_{ZVT} and snubber inductance L_r at various values of snubber capacitance C_r .

(b) The choice of snubber inductor L_r : The reverse recovery duration (t_{rr}) of D_m to select the L_r is important. The current of the switch should reach the level of input current at most within the duration of $3t_{rr}$ after the auxiliary switch is turned on. Duration t_{rr} of the main diode for the application is chosen as 50 ns. To determine L_r , the following equation can be leveraged:

$$\frac{1}{\omega_1}\sin^{-1}\left(\frac{I_{Lm}Z_1}{V_o}\right) \ge 3t_{rr}.$$
(28)

4. Simulation application and converter features

4.1. Simulation application

The proposed converter is simulated using PSIM electronics simulation software. The simulated circuit is presented in Figure 5, while the current and voltage simulation waveforms of S_m , S_a as well as D_m are portrayed in Figure 6. The simulation waveforms are suitable for both theoretical analysis and experimental results.

4.2. Converter features

The fundamental features of the proposed active snubber cell for soft switched PFC boost converters can be compiled as follows:

- 1. ZVT facilitates turning on the main switch, which is turned back off by means of ZVS. The energy recovery of the parasitic capacitance of S_m is realized;
- 2. ZVS facilitates turning on the main diode and turning it back off with ZCS;
- 3. The main diode reverse recovery losses are significantly reduced;
- 4. ZCS helps in turning on the auxiliary switch, which is turned back off with the aid of ZCT;
- 5. SS can aid in turning on and off the entire elements of semiconductors;
- 6. The proposed converter can work without hinging on the load current;
- Main devices are not exposed to additional voltage stress;



Figure 5. Simulated circuit of the proposed converter.



Figure 6. The simulation waveforms of the voltage and current for S_m , D_m as well as S_a from top to bottom, respectively.

- 8. Auxiliary semiconductor devices never experience voltage stress;
- 9. The switching period experiences very low transient intervals;
- 10. Ease of converter handling due to the common ground that switches have;
- 11. The overall architecture of the snubber cell is straightforward;
- 12. The presented snubber cell could be readily adopted for other basic converters;
- 13. Additional passive snubber cell is not required for the proposed converter;
- 14. The proposed converter exhibits a large PF performance.

5. Experimental results

A prototype of the presented PFC converter is realized operating at 600 W and 100 kHz. It is also verified with the aid of the predicted analysis of the converter. In this experimental study, the value of filter capacitance is set to 470 μ F, while the value of the main inductor is set to 1 mH and the value of the resonant inductor is set to 2 μ H. Additionally, 33 nF is chosen for the value of the resonant capacitor is set to 3.3 nF. To obtain the gate signals of the switches, the control circuit associated with the UC3854 integrated circuit is devised in the PFC converter. The control circuit is illustrated in Figure 7. The image of the experimental prototype is provided in Figure 8.



Figure 7. Control circuit of the proposed converter.



Figure 8. The image of the experimental prototype.

UC3854A connected converter produces a gate signal for the main switch. The gate signal of the auxiliary switch is gathered by using the gate signal of the main switch through the instrument of the analog card. Additionally, the semiconductor components utilized in the converter are given in Table 1.

Figure 9 represents the experimental outcomes of the proposed converter. The gate signals of the switches, the voltage and current wave shapes of the main switch are illustrated in Figure 9(a). According to Figure 9(a), the control signal is applied to the gate of S_m immediately after the voltage of S_m falls to zero. Hence, S_m is turned on by means of ZVT without the intersection of its current and voltage. Besides, S_m is turned off with the aid of ZVS. Hence, the power losses induced by S_m during the turning-on process are significantly diminished and the power losses induced by S_m during the turning off process are considerably reduced. Additionally, the main switch is not exposed to any voltage stress.

The current, the voltage and the control signal wave shapes of S_a are exhibited in Figure 9(b). As depicted in Figure 9(b), the auxiliary switch is turned on using ZCS and is turned off with the help of ZCT. Therefore, switching power losses during the turningon operation are reduced and switching power losses during the process of turning off are eliminated for the auxiliary switch. Additionally, the auxiliary switch does not experience any voltage stress.

The current, voltage, and control signal wave shapes of D_m are given in Figure 9(c). The main diode is turned on utilizing ZVS and turned off with the help of ZCS. Therefore, its power losses in switching and

Table 1. Semiconductor components and specifications utilized for the prototype.

Components	Part number	$V(\mathbf{V})$	$I(\mathbf{A})$	$t_r \ (ns)$	t_f (ns)	t_{rr} (ns)
S_m	IXFH15N60P	600	15	43	40	250
S_a	FCP190N60E	600	20	14	15	308
D_m	MUR860	600	8		—	60
D_a	DES18-06	600	8			50



Figure 9. Experimental outcomes of the current and voltage wave shapes of (a) S_m , (b) D_m , (c) S_a (200 V/div, 10 A/div, 1 μ s/div), and (d) AC input voltage and current wave shapes (100 V/div, 2 A/div, 5 ms/div).



Figure 10. Power factor for different input voltages and output power.



Figure 11. Efficiency comparison considering various converter topologies.

reverse recovery processes are considerably diminished. Moreover, the main diode is not exposed to any voltage/current stress.

The input voltage and current operating with 220 V input voltage and with 50 Hz frequency are given in Figure 9(d). Based on Figure 9(d), the current and voltage wave of AC input are of sinusoidal shape. Consequently, the power factor of 0.99 for 220 V AC input voltage at fully load is achieved during the experimental measurements. Additionally, the variance of PF depends on different line voltages, as given in Figure 10.

Figure 11 compares the efficiency of the proposed converter with the conventional converter topologies. It can be readily observed that the proposed converter is much more efficient than other converter topologies considering different ranges of load conditions. For the converter introduced, the efficiency is 91% considering HS operation and it is measured to be about 95.7% considering the SS operation at 600 W.

6. Conclusions

In this treatise, a new boost converter-based soft switched active snubber cell for Power Factor Correc-

tion (PFC) was suggested. The introduced converter facilitated the turning-on and turning-off processes for the main switch using Zero Voltage Transition (ZVT) and Zero Voltage Switching (ZVS), respectively. Therefore, ZVS and Zero Current Switching (ZCS) were utilized for turning on and turning off the main diode, respectively, while soft switching was applied to the entire auxiliary semiconductor components. The structure of the introduced converter was straightforward and characterized by ease of use and affordability. Moreover, the theoretical findings and simulation results of this research were validated with an experimental prototype considering the parameters of 600 W and 100 kHz. Consequently, the PF of about 0.99 was achieved for the proposed converter and the efficacy of the converter reached 95.7% at nominal output power.

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Biographies

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