Scientia Iranica D (2020) 27(3), 1494–1505

Sharif University of Technology
Scientia Iranica
Transactions D: Computer Science & Engineering and Electrical Engineering
http://scientiairanica.sharif.edu

Research Note

Modified quasi-Y-source converter for increasing boost factor

F. Zohrabi, E. Abiri*, A. Rajaei, and A. Nabinezhad

Department of Electronics and Electrical Engineering, Shiraz University of Technology, Shiraz, Iran.

Received 10 June 2017; received in revised form 9 May 2018; accepted 21 July 2018

KEYWORDS
Impedance source network;
Quasi-Y-source converter;
Renewable energy resource.

Abstract. In this paper, a new topology of quasi-Y-source impedance networks is presented. This converter utilizes the factor of change of winding and shoot through state in order to improve the gain of network. The proposed impedance network employs low turns ratio compared to quasi-Y-source and Y-source networks to achieve high voltage gain. The continuous input current of the proposed converter is an advantage, particularly for the applications related to the renewable energy sources such as Fuel Cell (FC) and photovoltaic (PV) systems. Furthermore, there are dc-current-blocking capacitors in the proposed network, which help to avoid the saturation of the coupled inductor. Operation principles of the converter are discussed and the steady-state relations as well as voltage gain and voltage stress across the dc-blocking capacitors are derived. The proposed converter is compared with the conventional quasi-Y-source network to show the advantages of the converter. Several simulations are performed and the results are shown to indicate the performance of the proposed network. In this paper, an experimental prototype of a converter is presented. To prove the validity and consistency of the proposed network, several tests are carried out. This plan can have a negative gain, similar to the quasi-Y-source network.

1. Introduction

Recently, renewable resources have attracted great attention due to the shortage of fossil fuels as well as oil and greenhouse pollution. The output voltage of fuel cells and photovoltaic systems is mostly low, while high voltage gain is needed [1,2]. Thus, the boost dc-dc converter is required, which leads to low efficiency and security of many converters. In addition, in some investigations, it has been proved that the Voltage Source Inverters (VSIs) and Current Source Inverters (CSIs) face several limitations and problems, which can be expressed as follows:

1. Conventional VSI is unable to increase the output voltage, because it is a buck converter; thus, a dc-dc boost converter is needed [3];
2. Current source converter is a boost converter in the conversion from dc to ac and is a buck converter in the conversion from ac to dc. In the applications that a vast range of voltages is needed, a dc-dc boost or buck converter is required. Thus, there will be an additional power conversion stage that causes an increase in the costs and a decrease in the efficiency [3].

*. *Corresponding author. Tel.: +98 7137354501; Fax: +98 7137353502*
E-mail addresses: fa_zohrabi@yahoo.com (F. Zohrabi); abiri@sutech.ac.ir (E. Abiri); a.rajaei@sutech.ac.ir (A. Rajaei); a.nabinezhad.68@gmail.com (A. Nabinezhad)

doi: 10.24200/sci.2018.20788

In order to overcome the limitations of voltage-source inverter and current-source inverter topologies, impedance-source networks have been proposed. Electric power conversion can take advantage of the suggested networks and provide voltage enhancement without any extra power stage. Peng introduced the Z-source converter as the first impedance network in 2003 [3], which could provide a new single-stage topology. The most significant feature of the Z-source network is being both open and short-circuit, unlike the VS or CS. The mentioned feature enables this converter with a mechanism for the main converter circuit to step up and down the voltage as desired in a single-stage power conversion [4,5]. On the other hand, there are some disadvantages to Z-Source Inverters (ZSIs). The main drawback of the voltage-fed ZSI appears in the boost mode, where the input current is discontinuous and the capacitors must sustain a high voltage. On the other hand, the main drawback of the current-fed ZSI is that the inductors must sustain high currents. To further improve traditional ZSIs, the quasi-Z-source inverters were suggested in [6].

Besides the benefits of the ZSIs, the quasi-Z-source inverters have their own advantages, such as continuous input current and reduced passive component ratings. Voltage gain of the Z-source inverters is limited. In order to increase voltage gain, several magnetically coupled impedance networks have been suggested [7]; some examples for such networks are trans-Z-source [8], Y-source [9], quasi-Y-source [10], and quasi-T-source [7]. After comparing the trans-Z-source and the Z-source inverters, it was shown that the trans-Z-source inverter could improve the voltage gain by its transformer [8]. Another important type of inverters is Y-source inverter, which uses three winding transformers. The main difference between this network and the classical impedance network can be expressed by the method of calculating the voltage gain. Since it is undesirable for most renewable sources to have discontinuous input current, bulk dc-bus capacitors are needed. Therefore, the quasi-Y-source network is proposed [10].

This paper proposes a new Y-source converter with the purpose of increasing the voltage gain of conventional quasi-Y-source converter considering the same winding factor. The suggested converter, due to continuous input current, uses a dc blocking capacitor. Therefore, it is able to eliminate the saturation problem.

In this paper, we investigate the relations among the converter parameters such as voltage gain, voltage stress on blocking capacitors, average value of the output voltage, and input inductor. First, a brief description of the performance of the converter is provided. It is then followed by simulation and experimental results.

2. Performance of the proposed Y-source

Figure 1 and Figure 2 show the quasi-Y-source and the proposed Y-source networks considering a three-winding transformer. The demonstrated networks contain an inductor L; two capacitors C_1 and C_2; a controlled switch and diode D_1; and a three-winding transformer with N_1, N_2, and N_3 turns, which present the primary, the secondary, and the third turns, respectively. Furthermore, the mentioned converter is in line with other types of the impedance-source converters in many aspects, such as two operating modes named shoot-through and non-shoot-through states [10]. The shoot-through state is forbidden in the traditional VSI, since it can cause damage to the device by a short circuit in the voltage source. In the quasi-Y-source converter, the impedance source network, which is connected to the inverter bridge, can alter the circuit operation and this situation allows for reaching the shoot-through states. Additionally, via the shoot-through state, the dc-link voltage could be enhanced by the quasi-Y-source network [11]. This can guarantee the protection of the circuit from damage besides improving the system reliability. The suggested Y-source network can be used for both the dc-dc converter and the dc-ac inverter.

Regarding the proposed Y-source network, the implementation of a dc-dc converter, which consists of an additional diode D_2, capacitor C_O, and load

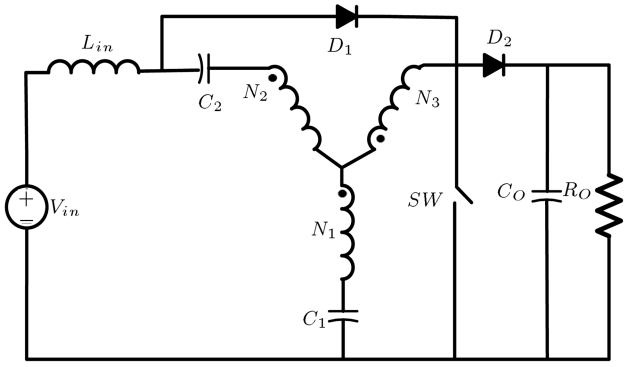

Figure 1. Quasi-Y-source converter.

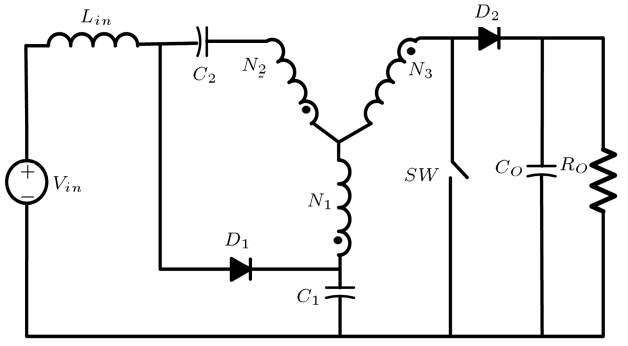

Figure 2. Proposed Y-source converter.

resistance R_L, is shown in Figure 2. When the switch SW is turned on, the shoot-through state is reached. In this state, diodes D_1 and D_2 are turned off. Simultaneously, the capacitors C_1 and C_2 charge the magnetizing inductance of the transformer. Besides, the load is supplied by the buffer capacitor C_O. The shoot-through state is shown in Figure 3 and formulated in Eqs. (1) to (4):

$$\frac{N_3}{N_1}V_{L1} - V_{L1} + V_{C1} = 0, \tag{1}$$

$$V_{Lin} = V_{in} - V_{C1} + V_{L1} + \frac{N_2}{N_1}V_{L1} + V_{C2}, \tag{2}$$

$$\Rightarrow V_{Lin} = V_{in} - V_{C1} + \left(1 + \frac{N_2}{N_1}\right)\left(\frac{V_{C1}}{1 - \frac{N_3}{N_1}}\right) + V_{C2}, \tag{3}$$

$$V_O = 0. \tag{4}$$

The non-shoot-through state is shown in Figure 4. This state is reached when the switch SW is turned off; therefore, diode D_1 is switched to the ON mode and the input voltage V_{in} recharges C_1 and C_2. Meanwhile, the filter capacitor C_O and the power load are recharged by the input voltage with the magnetizing inductance. This state is formulated in Eqs. (5) to (9):

$$V_{L1} + \frac{N_2}{N_1}V_{L1} + V_{C2} = 0 \Rightarrow V_{L1} = \frac{-V_{C2}}{\left(1 + \frac{N_2}{N_1}\right)}, \tag{5}$$

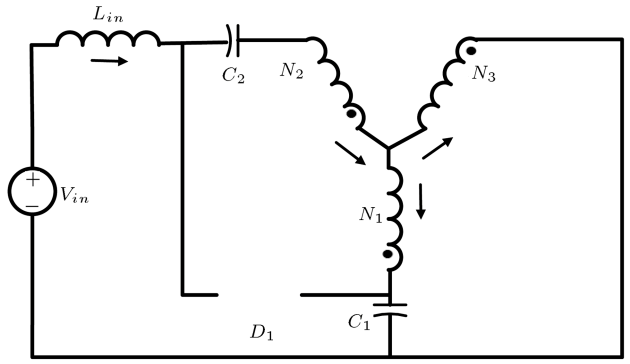

Figure 3. Proposed Y-source in shoot-through state.

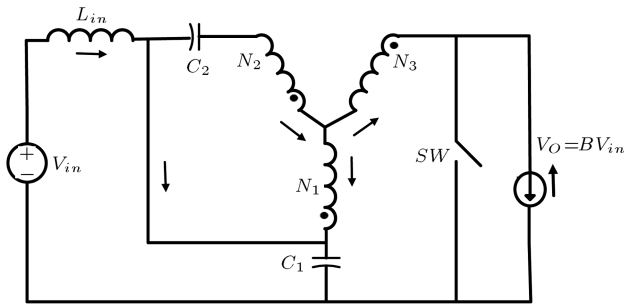

Figure 4. Proposed Y-source in non-shoot-through state.

$$V_{Lin} = (V_{in} - V_{C1}), \tag{6}$$

$$V_o = \frac{N_3}{N_1}V_{L1} - V_{L1} + V_{C1}. \tag{7}$$

The steady state causes the average voltage of the inductors to be zero over one switching cycle. From Eqs. (1) and (5), the following relation can be obtained:

$$\left(\frac{V_{C1}}{1 - \frac{N_3}{N_1}}\right)D_{st} + \left(\frac{-V_{C2}}{1 + \frac{N_2}{N_1}}\right)(1 - D_{st}) = 0, \tag{8}$$

$$\Rightarrow \frac{V_{C1}}{V_{C2}} = \frac{(N_1 - N_3)(1 - D_{st})}{D_{st}(N_1 + N_2)}, \tag{9}$$

where D_{st} denotes the shoot-through duty cycle.

Applying the volt-second balance principle to the inductor L_{in} yields:

$$\left(V_{in} - V_{C1} + \left(1 + \frac{N_2}{N_1}\right)\left(\frac{V_{C1}}{1 - \frac{N_3}{N_1}}\right) + V_{C2}\right)D_{st} + (V_{in} - V_{C1})(1 - D_{st}) = 0, \tag{10}$$

$$\Rightarrow \frac{D_{st}V_{C1}}{\left(\frac{N_1 - N_3}{N_1}\right)}\left(\frac{N_1 + N_2}{N_1}\right) + D_{st}V_{C2} + V_{in} - V_{C1} = 0. \tag{11}$$

Following Eqs. (9) and (11), the voltages across the capacitors C_1 and C_2 can be calculated by:

$$V_{C1} = \frac{(1 - D_{st})}{1 - D_{st}\left(1 + \frac{N_1 + N_2}{N_1 - N_3}\right)}V_{in}, \tag{12}$$

$$V_{C2} = \frac{D_{st}\left(\frac{N_1 + N_2}{N_1 - N_3}\right)}{1 - D_{st}\left(1 + \frac{N_1 + N_2}{N_1 - N_3}\right)}V_{in}. \tag{13}$$

From Eqs. (5), (7), (9), and (12), the maximum output voltage can be given by Eq. (14) during the non-shoot-through state.

$$V_{om} = \frac{V_{in}}{1 - D_{st}\left(1 + \frac{N_2 + N_1}{N_1 - N_3}\right)}. \tag{14}$$

Therefore, the converter voltage gain is as follows:

$$G_v = \frac{V_{om}}{V_{in}} == \frac{1}{1 - (1 + K')D_{st}} = B. \tag{15}$$

According to Eq. (15), the voltage gain G_v is proportional to winding factor K' and the boost factor B of the proposed-Y-source impedance network, where

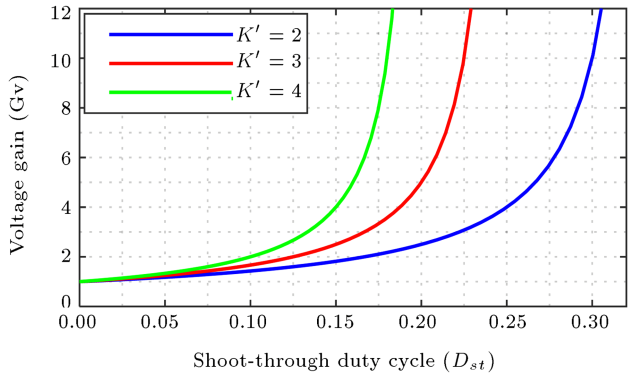

Figure 5. Theoretical voltage gain of the proposed Y-source network versus D_{st} and winding factor K'.

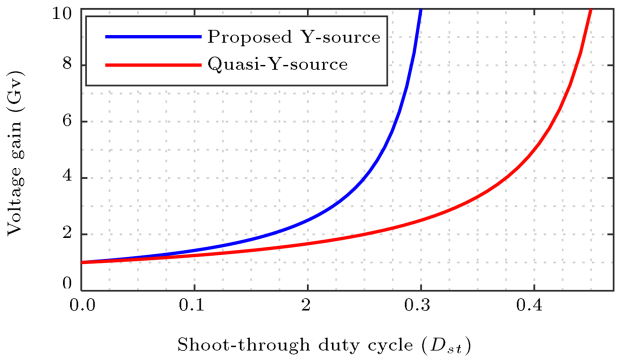

Figure 6. Comparison of voltage gains of the proposed Y-source network ($K' = 2$) and quasi-Y-source network ($\delta = 2$).

K' and B are defined as $K' = (N_1 + N_2)/(N_1 - N_3)$ and $B = 1/(1 - (1 + K')D_{st})$.

$$V_{om} = \frac{1}{1 - \left(1 + \frac{N_1+N_2}{N_1-N_3}\right) D_{st}},$$

$$V_{in} = \frac{1}{1 - (1 + K') D_{st}} V_{in}. \tag{16}$$

The range of variation for D_{st} in the proposed-Y-source network can be determined as:

$$0 \le D_{st} \le D_{st,\max} = \frac{1}{1 + K'}. \tag{17}$$

The voltage gain gets a negative value when the shoot-through time is greater than $1/(1 + K')$. It can be seen in Figure 5 that the voltage gain for the proposed-Y-source network is a function of the shoot-through duty cycle D_{st} with a different winding factor K', where $K' > 1$. The gain of the proposed-Y-source network, which is obtained considering a different winding factor K' and turns ratio $(N_1 : N_2 : N_3)$, is given in Table 1. According to Eq. (16), it should be noted that the winding factor of the proposed-Y-source is in contrast to that of the quasi-Y-source impedance network ($\delta = (N_1 + N_2)/(N_1 - N_3)$) shown in Figure 1 [10]. Following the analysis in [10], the maximum output voltage of the quasi-Y-source impedance network is given by:

$$V_{om} = \frac{V_{in}}{1 - D_{st}\left(\frac{N_2+N_1}{N_1-N_3}\right)} = \frac{V_{in}}{1 - \delta D_{st}}. \tag{18}$$

We can determine the variation range for D_{st} as follows:

$$0 \le D_{st} \le D_{st,\max} = \frac{1}{\delta}. \tag{19}$$

Therefore, with the same winding factor, it can be seen that the voltage gain of the proposed Y-source network is greater than that of the quasi-Y-source network, as shown in Figure 6. Based on [10], the voltages across the capacitors C_1 and C_2 of the quasi-Y-source network can be written as:

$$V_{C1} = \frac{(1 - D_{st})}{1 - D_{st}\left(\frac{N_1+N_2}{N_2-N_3}\right)} V_{in}, \tag{20}$$

$$V_{C2} = \frac{D_{st}\left(\frac{N_3+N_2}{N_1-N_3}\right)}{1 - D_{st}\left(\frac{N_1+N_2}{N_1-N_3}\right)} V_{in}. \tag{21}$$

3. Capacitor voltage stress

The voltage stresses across C_1 and C_2 are defined

Table 1. Gain of the proposed Y-source impedance network achieved with a different winding factor, K', and turns ratio, $(N_1 : N_2 : N_3)$.

$K' = (N_1 + N_2)/(N_1 - N_3)$	$D_{st,\max}$	Gain G_v	$N_1 : N_2 : N_3$
2	1/3	$(1 - 3D_{st})^{-1}$	(5:3:1) (3:1:1) (4:2:1)
3	1/4	$(1 - 4D_{st})^{-1}$	(2:1:1) (3:3:1) (4:2:2)
4	1/5	$(1 - 5D_{st})^{-1}$	(2:2:1) (3:1:2) (3:5:1)
5	1/6	$(1 - 6D_{st})^{-1}$	(3:2:2) (4:1:3) (2:3:1)
6	1/7	$(1 - 7D_{st})^{-1}$	(2:4:1) (4:2:3) (3:3:2)

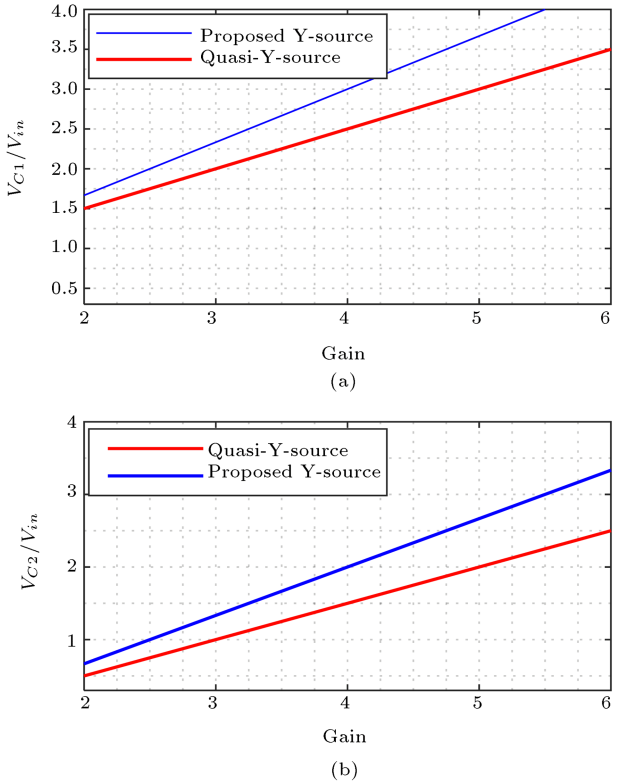

Figure 7. (a) Voltage stress across capacitor C_1 ($\delta = 2, K' = 2$). (b) Voltage stress across capacitor C_2 ($\delta = 2, K' = 2$).

according to Eqs. (12) and (13). Note that the voltage stresses of the capacitors C_1 and C_2 are higher than those of the quasi-Y-source network [10], as shown in Figure 7(a) and 7(b).

4. Average output voltage

The average output voltage [12] can be found as follows:

$$\overline{V_o} = \frac{1}{T}\int_{D_{st}T}^{T} \frac{V_{in}}{1-(1+K')\,D_{st}} = \frac{V_{in}\,(1-D_{st})}{1-(1+K')\,D_{st}}. \quad (22)$$

The denominator of Eq. (18) indicates that the voltage gain will be negative when the shoot-through time becomes greater than $1/(1+K')$. The average output voltage gain of the proposed-Y-source network with a different duty ratio D_{st} and winding factor K' is shown in Figure 8. Here, it is assumed that $K' = 2$.

5. Calculating the value of input inductor

The inductance of the dc-dc boost converter can be expressed through the current ripple factor K_L. If the losses are ignored, the output power P_{out} is equal to the input power. Therefore, the input voltage and the

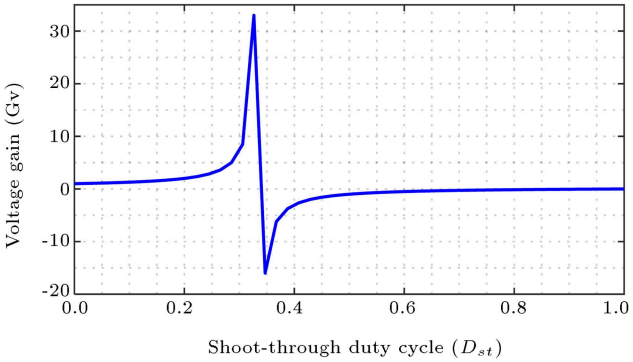

Figure 8. Average output voltage gain of the proposed Y-source network.

input power are used to calculate the input current [12].

$$I_L = \frac{P_{out}}{V_{in}}. \quad (23)$$

Inductor current ripple can be calculated as follows:

$$\Delta I_L = \int_{D_{st}T}^{T} \frac{di_L}{dt}dt = \int_{D_{st}T}^{T} \frac{V_L}{L}dt = \frac{V_L}{L}T\,(1-D_{st})\,. \quad (24)$$

The voltage across the inductor L during the non-shoot-through state is:

$$V_L = (V_{in} - V_{C1})\,. \quad (25)$$

Substituting Eq. (25) into Eq. (24) gives:

$$\Delta I_L = \frac{(1-D_{st})\,T\,(V_{in}-V_{C1})}{L}. \quad (26)$$

The current ripple factor K_L can be expressed as:

$$K_L = \frac{\Delta I_L}{I_L}. \quad (27)$$

The inductance of the dc-dc boost converter is stated through the current ripple factor K_L based on Eqs. (26) and (27), as follows:

$$L = \frac{(1-D_{st})\,T\,(V_{in}-V_{C1})}{K_L}\left(\frac{V_{in}}{P_{out}}\right). \quad (28)$$

In Eq. (28), the voltage across capacitor C_1 can be evaluated by:

$$V_{C1} = \frac{V_{in}\,(1-D_{st})}{1-D_{st}\left(1+\left(\frac{N_1+N_2}{N_1-N_3}\right)\right)}. \quad (29)$$

6. Simulation results

In this section, we provide computer simulations to analyze the theoretical and experimental results. Figure 2 shows the design of the converter. Tables 2 and

Table 2. General specifications of the proposed Y-source converter.

Symbols	Definitions	Values
V_{in}	Input voltage	50 (V)
V_O	Output voltage	200 (V)
C_1	Capacitance of capacitor C_1	330 (μF)
C_2	Capacitance of capacitor C_2	330 (μF)
C_O	Capacitance of output capacitor	47 (μF)
L	Inductance of inductor	2 (mH)
$N_1 : N_2 : N_3$	Turns ratio	3:1:1
K'	Winding factor	2
D_{st}	Duty cycle	0.25
f_s	Switching frequency	22 (kHZ)
R_L	Load	200 (Ω)

Table 3. General specifications of the proposed Y-source converter.

Symbols	Definitions	Values
V_{in}	Input voltage	50 (V)
V_O	Output voltage	125 (V)
C_1	Capacitance of capacitor C_1	330 (μF)
C_2	Capacitance of capacitor C_2	330 (μF)
C_O	Capacitance of output capacitor	47 (μF)
L	Inductance of inductor	2 (mH)
$N_1 : N_2 : N_3$	Turns ratio	2:1:1
K'	Winding factor	3
D_{st}	Duty cycle	0.15
f_s	Switching frequency	22 (kHZ)
R_L	Load	200 (Ω)

3 list the parameters of the proposed converter. Using Eq. (17) and assuming $K' = 2$, the shoot-through range can be $0 < D_{st} < 1/3$. According to Eq. (15), if the value of D_{st} in Table 2 is set to 0.25, the amount of gain will be 4. The achieved gain here is higher than the gain of quasi-Y-source converter and can be boosted to $V_{om} = 200$ V at an input voltage of $V_{in} = 50$ V.

The output voltage of the proposed Y-source is shown in Figure 9(b). As shown in this figure, the output voltage increases to 200 V, which is close to the theoretical values. The voltage stresses across capacitors C_1 and C_2 are shown in Figure 9(c) and (d). According to Figure 9(c) and (d), V_{C1} and V_{C2} are boosted to 150 V and 100 V, respectively. It can be seen that these values are close to the theoretical ones. The input current drawn by the network is continuous, as shown in Figure 9(e). In order to achieve a constant output voltage, the shoot-through duty cycle is changed from 0.1 to 0.246.

For a wide range of input voltages (52 V–100 V), the output voltage is adjusted to 200 V. Considering $K' = 2$ and $D_{st} = 0.25$, the experimental waveforms of the proposed Y-source dc-dc converter are depicted in Figure 10. It should be noted that the simulation results follow the experimental results. Figure 1 shows the quasi-Y-source network based on the listed parameters in Tables 4 and 5. For $\delta = 2$ and $D_{st} = 0.25$, the experimental and simulation waveforms of the quasi-Y-source network are shown in Figures 11 and 12. Eq. (18) reveals that the output voltage increases to $V_{om} = 100$ V. Both practical and simulation results confirm that the output voltage is

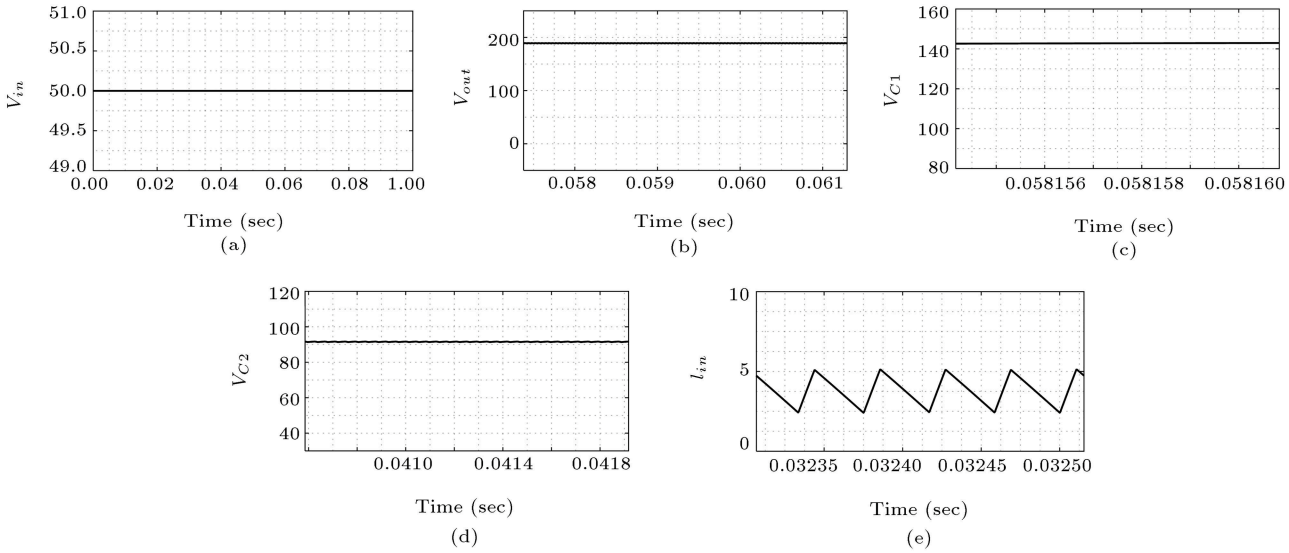

Figure 9. Waveforms obtained by the simulation of the proposed Y-source boost dc-dc converter with $D_{st} = 0.25$, winding factor $K' = 2$, and $f_s = 22$ kHZ: (a) Input voltage, (b) output voltage, (c) voltage of capacitor C_1, (d) voltage of capacitor C_2, and (e) input current.

Table 4. General specifications of the quasi-Y-source converter.

Symbols	Definitions	Values
V_{in}	Input voltage	50 (V)
V_O	Output voltage	100 (V)
C_1	Capacitance of capacitor C_1	330 (μF)
C_2	Capacitance of capacitor C_2	330 (μF)
C_O	Capacitance of output capacitor	47 (μF)
L	Inductance of inductor	2 (mH)
$N_1 : N_2 : N_3$	Turns ratio	3:1:1
δ	Winding factor	2
D_{st}	Duty cycle	0.25
f_s	Switching frequency	22 (kHZ)
R_L	Load	200 (Ω)

approximately 100 V. Besides, the output voltages of the capacitors C_1 and C_2, according to Eqs. (20) and (21), are set to 75 and 25 V.

Given $K' = 3$ and $D_{st} = 0.15$ in the formulation, the experimental and simulation waveforms of the proposed Y-source network are shown in Figures 13 and 14. Based on Eq. (14), the output voltage can be given as $V_{om} = 125$ V. Likewise, in the simulation and practical results, output voltage is approximately 125 V. The output voltages of the capacitors C_1 and C_2 are 105 and 56 V, according to Eqs. (12) and (13).

Denoting $\delta = 3$ and $D_{st} = 0.15$, Figures 15 and 16 show the simulation and experimental waveforms of the quasi-Y-source network, based on Eq. (18). For the quasi-Y-source dc-dc converter, the output voltage will be boosted to $V_{om} = 90$ V; similarly, its value in both practical and simulation results is around 90 V. Following Eqs. (20) and (21), the output voltages of the capacitors C_1 and C_2 are 77 and 27 V. It can be observed that the approximate values of V_{C1} and V_{C2} are boosted to 77 V and 27 V in experimental and simulation waveforms. In the presented figures, the practical results have the same behavior as that of the simulation results. Furthermore, in equal conditions,

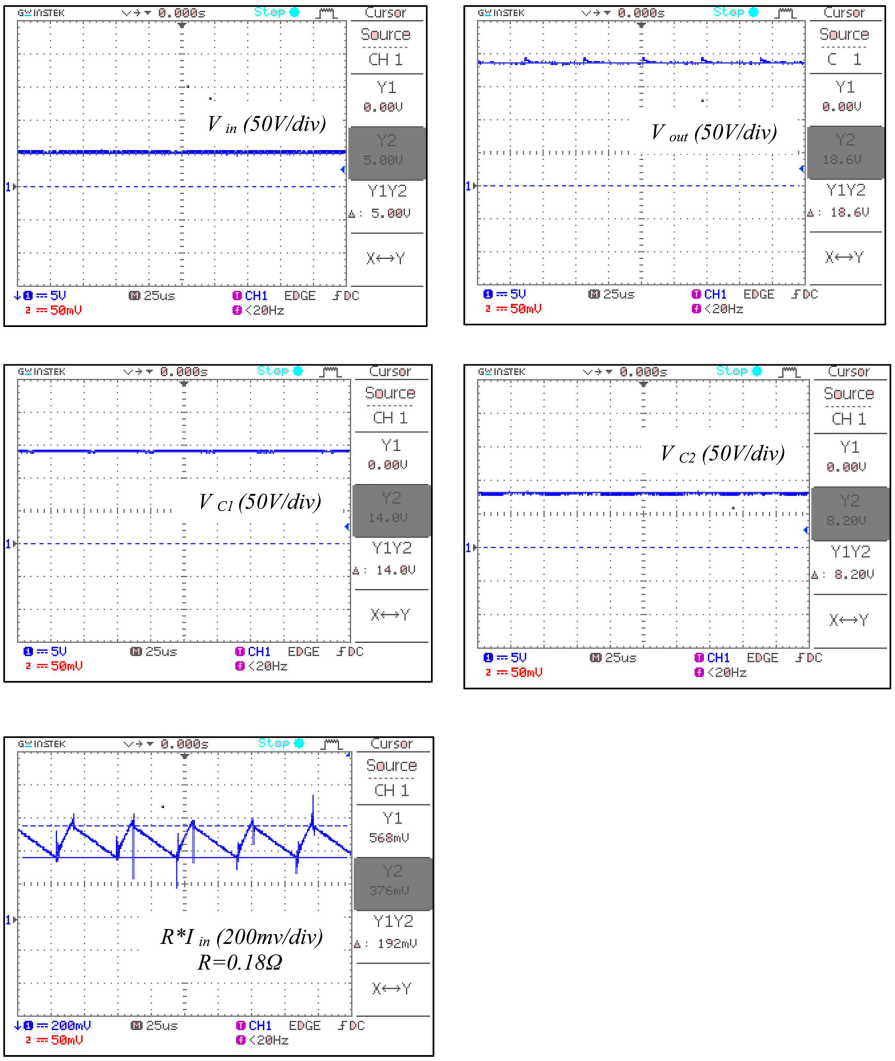

Figure 10. Experimental waveform of the proposed single-switch Y-source dc-dc converter with turns ratio of (3:1:1) and $D_{st} = 0.25$.

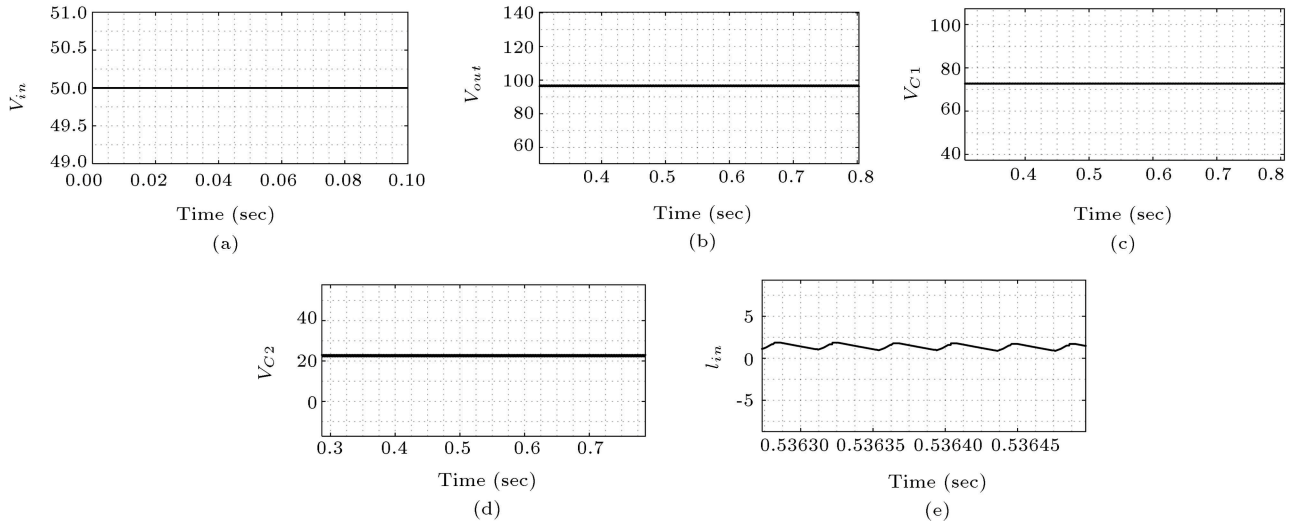

Figure 11. Waveforms obtained by the simulation of the quasi-Y-source boost dc-dc converter with $D_{st} = 0.25$, winding factor $\delta = 2$, and $f_s = 22$ kHZ: (a) input voltage, (b) output voltage, (c) voltage of capacitor C_1, (d) voltage of capacitor C_2, and (e) input current.

Table 5. General specifications of the quasi-Y-source converter.

Symbols	Definitions	Values
V_{in}	Input voltage	50 (V)
V_O	Output voltage	90 (V)
C_1	Capacitance of capacitor C_1	330 (μF)
C_2	Capacitance of capacitor C_2	330 (μF)
C_O	Capacitance of output capacitor	47 (μF)
L	Inductance of inductor	2 (mH)
$N_1 : N_2 : N_3$	Turns ratio	2:1:1
δ	Winding factor	3
D_{st}	Duty cycle	0.15
f_s	Switching frequency	22 (kHZ)
R_L	Load	200 (Ω)

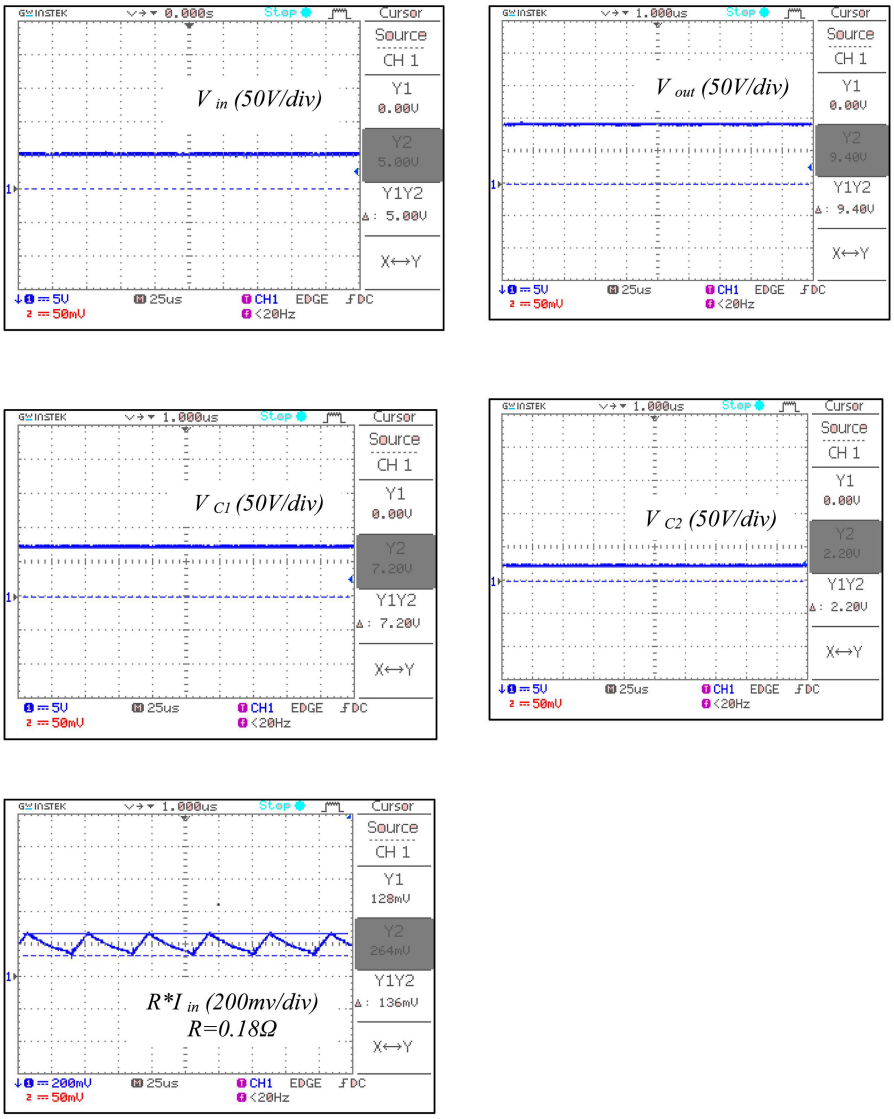

Figure 12. Experimental waveform of the single-switch quasi-Y-source dc-dc converter with turns ratio of (3:1:1) and $D_{st} = 0.25$.

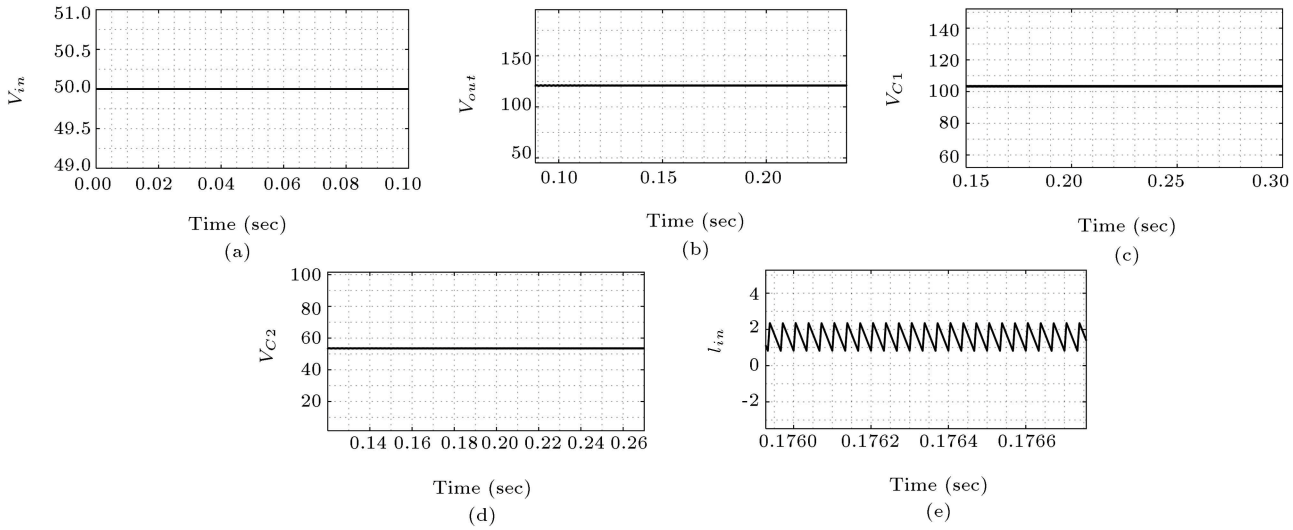

Figure 13. Waveforms obtained by the simulation of the proposed Y-source boost dc-dc converter with $D_{st} = 0.15$, winding factor $K' = 3$, and $f_s = 22$ kHZ: (a) Input voltage, (b) output voltage, (c) voltage of capacitor C_1, (d) voltage of capacitor C_2, and (e) input current.

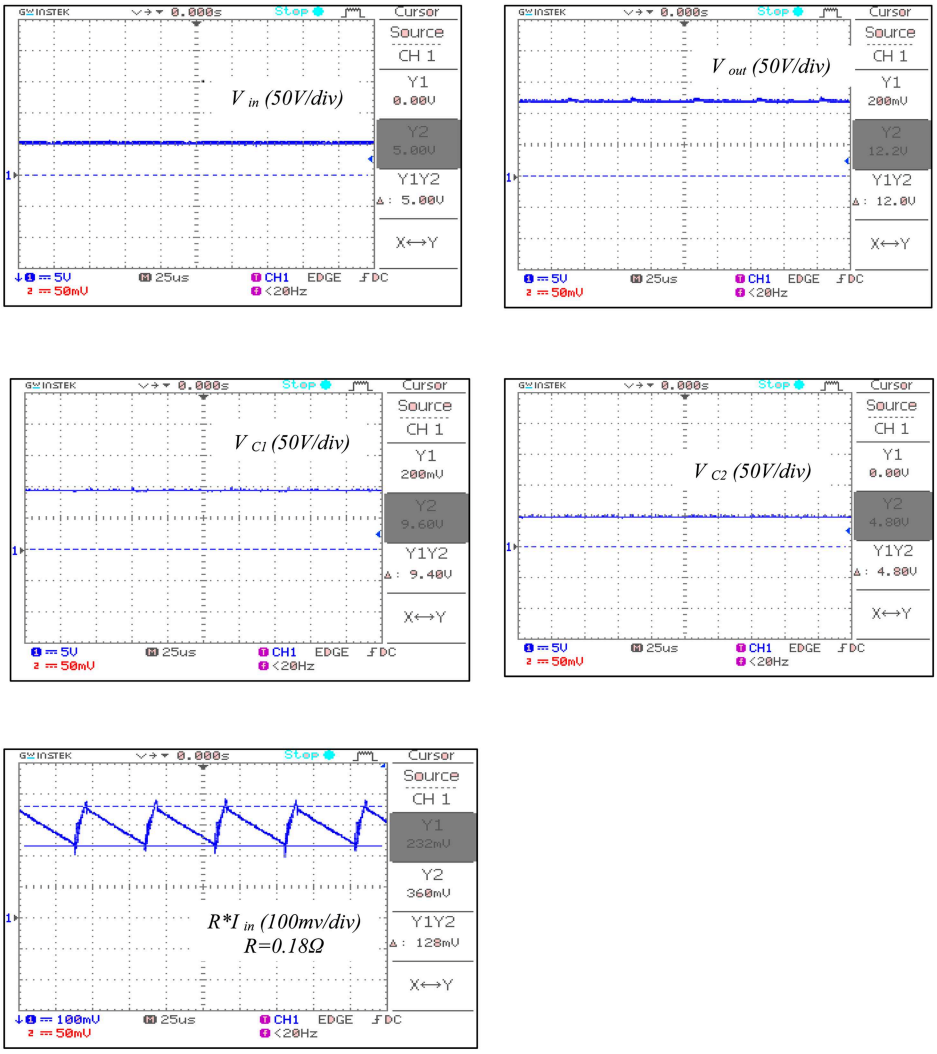

Figure 14. Experimental waveform of the proposed single-switch Y-source dc-dc converter with turns ratio of (2:1:1) and $D_{st} = 0.15$.

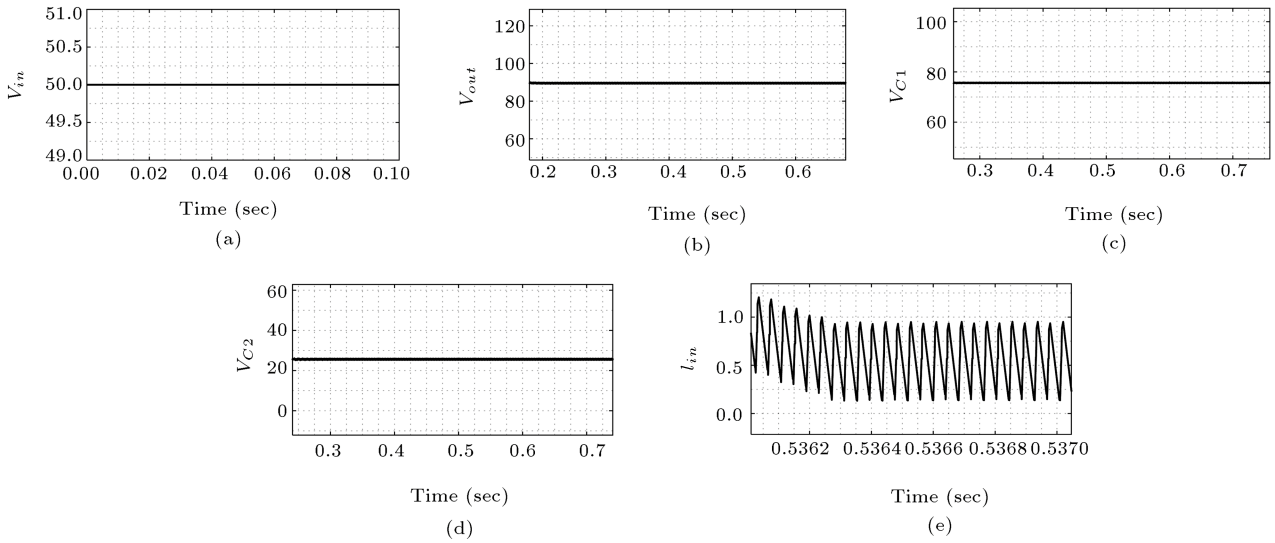

Figure 15. Waveforms obtained by the simulation of the quasi-Y-source boost dc-dc converter with $D_{st} = 0.15$, winding factor $\delta = 3$, and $f_s = 22$ kHZ: (a) input voltage, (b) output voltage, (c) voltage of capacitor C_1, (d) voltage of capacitor C_2, and (e) input current.

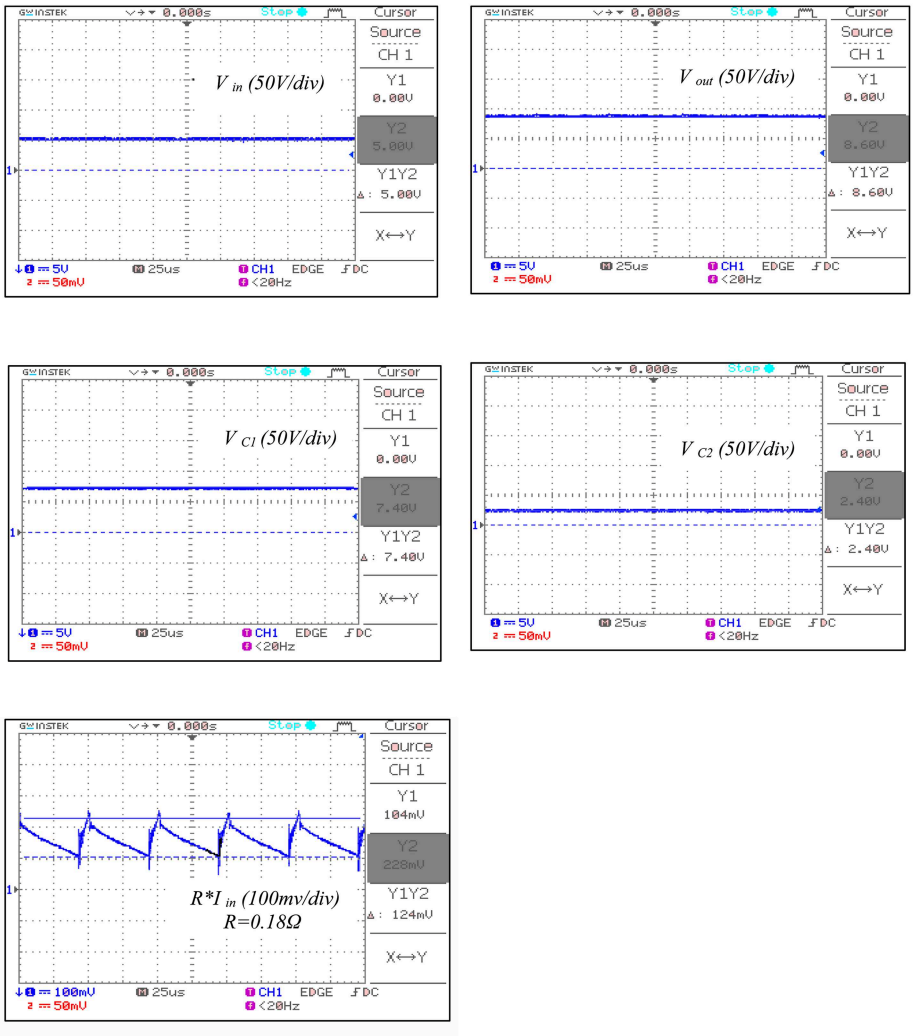

Figure 16. Experimental waveform of the single-switch quasi-Y-source dc-dc converter with turns ratio of (2:1:1) and $D_{st} = 0.15$.

the voltage gain in the proposed converter is greater than that in the quasi-Y-source converter.

7. Conclusion

In this paper, we proposed a new impedance source network, which was able to maintain small duty ratio and turns ratio of the coupled magnetics. It suitably performed in converters operating in high voltage gain. In comparison to the conventional quasi-Y-source and Y-source networks, the new topology utilized low turns ratio and provided a continuous input current to achieve high voltage gain. This is a suitable feature of this topology, which can be applied to new energy sources. The expected performance and the functionality of the proposed dc-dc converter were confirmed by both mathematical and experimental results.

References

1. Blaabjerg, F. "Power electronics as efficient interface in dispersed power generation systems", *IEEE Transactions on Power Electronics*, **19**(5), pp. 1184–1194 (2004).
2. Forouzesh, M. and Baghramian, A. "Analysis and development of an improved Y-source boost DC-DC converter", *International Journal on Electrical Engineering and Informatics*, **8**(1), pp. 200–219 (2016).
3. Peng, F.Z. "Z-source inverter", *IEEE Transactions on Power Electronics*, **39**(2), pp. 504–510 (2003).
4. Liu, Y., Abu-Rub, H., and Ge, B. "Z-source/quasi-Z-source inverters derived networks, modulations, controls, and emerging applications to photovoltaic conversion", *IEEE Ind. Electron. Mag.*, **8**(2), pp. 32–44 (2014).
5. Siwakoti, Y.P., Peng, F.Z., Blaabjerg, F., Loh, P.C., Town, G.E. "Impedance-source networks for electric power conversion. Part I: A topological review", *IEEE Trans. Power Electron*, **30**(2), pp. 699–716 (2015).
6. Joel Aderson, and F.Z. Peng "Four Quasi-Z-Source inverter", In *Proc. IEEE Power Electron. Spec. Conf.*, pp. 2743–2749 (2008).
7. Siwakoti, Y.P., Blaabjerg, F., and Chiang Loh, P. "New magnetically coupled impedance (Z-) source networks", *IEEE Transactions on Power Electronics*, **31**(11), pp. 7419–7435 (2016).
8. Qian, W., Peng, F.Z., and Cha, H. "Trans-Z-source inverters", *IEEE Transactions on Power Electronics*, **26**(12), pp. 3453–3463 (2011).
9. Siwakoti, Y.P., Loh, P.C., Blaabjerg, F., and Town, G.E. "Y-source impedance network", *IEEE Transactions on Power Electronics*, **29**(7), pp. 3250–3254 (2014).
10. Siwakoti, Y.P., Blaabjerg, F., and Chiang Loh, P. "Quasi-Y-source boost DC-DC converter", *IEEE Transactions on Power Electronics*, **30**(12), pp. 6514–6519 (2015).
11. Li, Y., Anderson, J., Peng, F.Z., Liu, D. "Quasi-Z-source inverter for photovoltaic power generation systems", In *Proc. Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, pp. 918–924 (2009).
12. Husev, O., Blaabjerg, F., and Clemente, C. "Comparison of impedance-source networks for two and multilevel buck-boost inverter applications", *IEEE Transactions on Power Electronics*, **31**(11), pp. 7564–7579 (2016).

Biographies

Fatemeh Zohrabi received her BSc in Electrical Engineering from Shahid Chamran University of Ahvaz in 2005 and MSc from Bushehr University in 2010. She is currently pursuing the PhD degree in Electronics and Electrical Engineering at Shiraz University of Technology, Shiraz, Iran. Her research interests include power converters, power system operation and economics, renewable energy systems, and evolutionary optimization algorithms.

Ebrahim Abiri received his BSc in Electronics Engineering from Iran University of Science and Technology in 1992, MSc from Shiraz University in 1996, and PhD in Electronic from Iran University of Science and Technology in 2007. He has authored more than 80 published technical papers in electronics and power electronics and 4 books. He has been with the Department of Electrical Engineering at Shiraz University of Technology since 2007.

Amirhossein Rajaei was born in Jahrom, Iran. He received MS and PhD degrees in Electrical Engineering from Tarbiat Modares University, Tehran, Iran, in 2009 and 2013, respectively. He is currently Assistant Professor at Shiraz University of Technology, Shiraz, Iran. His main research interests include renewable energy resources, power converters, electric vehicles, and motor drive systems.

Ali Nabinezhad received his BSc in Power Engineering from Kashan University in 2012 and MSc from Shiraz University of Technology in 2018. His research interests include power converters, power system operation and economics, and renewable energy systems.